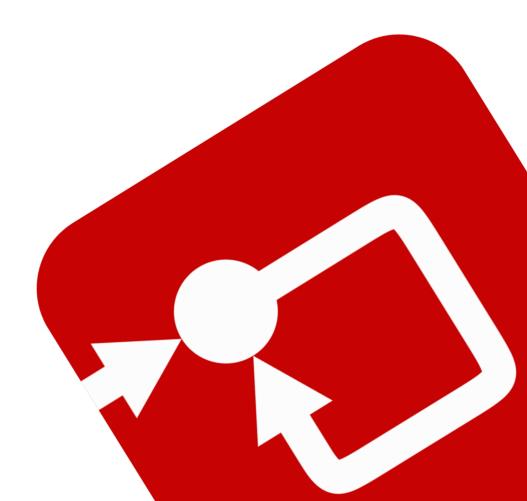


Peak Current Mode Control

Tutorial –December 2018-



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General Index

1. Introduction	3
2. Brief operating principle explanation of the Peak Current Mode Control	3
3. Design a Peak Current Mode Control with SmartCtrl.	4
4. Bibliography	. 12

Figure Index

Figure 1: Buck converter with Peak Current Mode Control	3
Figure 2: Buck converter with Peak Current Mode Control and artificial ramp	4
Figure 3: SmartCtrl initial menu	5
Figure 4: Selecting the topology	5
Figure 5: buck converter parametrization	6
Figure 6: current sensor definition	6
Figure 7: modulator parameters	7
Figure 8: Voltage sensor parameters	8
Figure 9: Type 3 compensator parameters	8
Figure 10: Solution map with the point selected	8
Figure 11: SmartCtrl analysis view	9
Figure 12: Exporting to Psim button	9
Figure 13:Exporting to Psim options	10
Figure 14: Psim exported schematics	10
Figure 15:Psim simulation result	11



1. Introduction

SmartCtrl is a software specifically designed to aid in the design of the control loop used in power electronics applications. With this aim, SmartCtrl provides many predefined topologies, compensators and control types which allow an easy and straightforward way of designing the control loop.

This tutorial is intended to guide you, step by step, along the design of a peakcurrent mode control of a DC/DC converter using the pre-defined topologies of the SmartCtrl Software.

The peak current mode control (PCMC) was proposed in the 80's by Bob Mammano, and it became fashionable with the appearance of UC1842 device [1]. It is based on controlling the output voltage of the DC/DC converter through the control of the inductance maximum peak current.

2. Brief operating principle explanation of the Peak Current Mode Control

Figure 1 shows the circuit of a buck converter with peak current mode control. When the switching period starts, the transistor is switched on and the voltage drop across the inductance is positive; therefore, its current will increase accordingly. This current is compared to the control current (Ic) provided by the voltage loop regulator, and when the inductance current reaches Ic the transistor is switched off, and so the inductance current slope becomes negative.

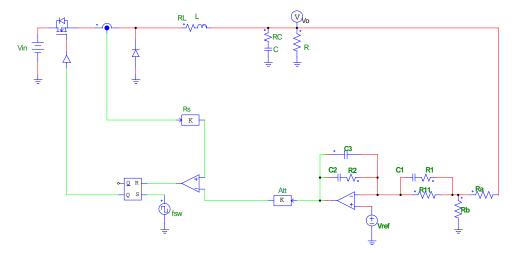


Figure 1: Buck converter with Peak Current Mode Control

The main drawback of this control technique is its noise susceptibility, which may cause a premature reset of the latch and consequently, the appearance of subharmonic oscillations that may lead to instabilities [1]. Instability due to



subharmonic oscillations appears only in continuous conduction mode when duty cycles are above 50%, as demonstrated in [1]; and it can be eliminated by adding an artificial ramp to the sensed current waveform (see Figure 2)).

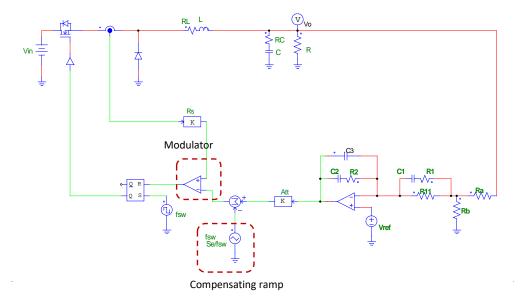


Figure 2: Buck converter with Peak Current Mode Control and artificial ramp

3. Design a Peak Current Mode Control with SmartCtrl.

Within the pre-defined control strategies provided by SmartCtrl, you can find the Peak Current Mode Control. This control strategy can be applied to any of the predefined DC/DC converters included in SmartCtrl: Buck, Boost, Buck-Boost, Flyback and Forward. Along this tutorial, the peak current mode control is going to be applied to a buck converter. Let's start a step by step configuration of this system.

To access the configuration window of the Peak Current Mode Control, there are three possible paths:

1. Click on DC-DC converter peak-current mode control as shown in Figure 3.



SmartCtrl	×
Design a predefined topology	Open a
DC-DC power stage and control circuit design	default file
DC-DC converter - Single loop Voltage Mode Control or ACMC	recently saved file
DC-DC converter Peak current mode control	previously saved file
DC-DC converter Average Current Mode Control	sample design
PFC Boost converter	
Design a generic topology	Design a generic control system
s-domain model editor	Equation editor
Import frequency response data from txt file	Help

Figure 3: SmartCtrl initial menu

2. Select one of the pre-defined DC/DC converters. In this tutorial a buck converter has been chosen and configured. See Figure 4 and Figure 5.

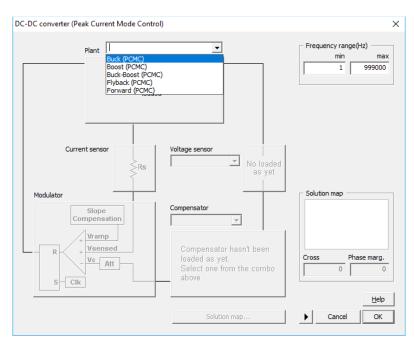


Figure 4: Selecting the topology



Buck (PCMC)	×
Steady-state dc operating point Conduction mode Duty cycle IL avg (A) Steady-state dc operating point Conduction mode Duty cycle IL avg (A) Steady-state dc operating point Continuous Duty cycle 275 m IL avg (A) 917.076 m IL max (A) 917.076 m IL min (A) 598.076 m Vo (V) 3.3	Vin(V) 12 RL(Dhms) 1 n L(H) 30 u Rc(Dhms) 50 m C(F) 160 u R(Dhms) 4.356 Po(W) 2.5 Fsw(Hz) 250 k
Set <u>d</u> efaults	Update read only boxes Help Cancel DK

Figure 5: buck converter parametrization

3. Define the current sensor as shown in Figure 6.

Ri sensor		×
Rs	Rs (Ohms) 0.2	
Set <u>d</u> efaults		<u>H</u> elp <u>C</u> ancel <u>D</u> K

Figure 6: current sensor definition

4. Define the modulator parameters as shown in Figure 7.



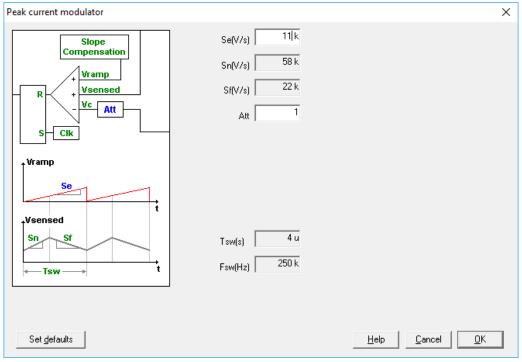


Figure 7: modulator parameters

From top to bottom, the modulator input signals are de following:

- **Vramp** is the characteristic compensation slope used with this type of control technique. This compensation slope is added to the inductance current in order to ensure the system stability when duty cycles are above 50%.
- **Vsensed** is the equivalent voltage of the sensed inductance current.
- **Vc** is the sensed regulator output voltage

Regarding the modulator design criteria, they are defined below:

- **Sn** The inductance charge slope.
- **Sf** The inductance discharge slope.
- **Se** The slope of the compensation ramp, it is computed as function of Sn and Sf.
- Att Is the attenuation applied to the regulator output voltage
- 5. Once the modulator has been defined, the voltage sensor must be selected among the available pre-defined voltage sensors. In this tutorial, a voltage divider has been selected. See Figure 8.



Voltage divider		×
VolRa	Gain 757.576 m	Calculate Gain=Vref/Vo from Vref
Vref Rb	Vo(V) 3.3	
<u> </u>	Vref(V)	
Set <u>d</u> efaults		Help Cancel OK

Figure 8: Voltage sensor parameters

6. In order to complete the configuration of the controlled system, the compensator topology has to be selected. Choose a Type 3 and parametrize it as shown in Figure 9.

Туре 3		×
C2 R2 Vref	R11(ohms) 10K	
Set <u>d</u> efaults		<u>H</u> elp <u>C</u> ancel <u>O</u> K

Figure 9: Type 3 compensator parameters

7. Select the phase margin and the crossover frequency of the open loop. SmartCtrl provides the solutions map in order to ease the selection of these parameters.

Select a fc of 1.5kHz and a PM of 90 degrees and click OK to validate the selection. See Figure 10.

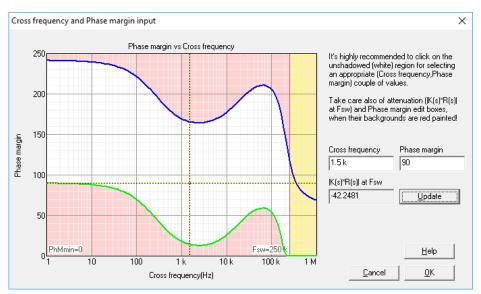


Figure 10: Solution map with the point selected



The graphic panels will show the Bode plots, Nyquist, transient response and steady state waveforms of the DC/DC converter with a peak current mode control, as shown in Figure 11.

At any time, the user can change the parameterization of the system and the results will be updated accordingly. To change the parameterization, just click on any of the graphics.

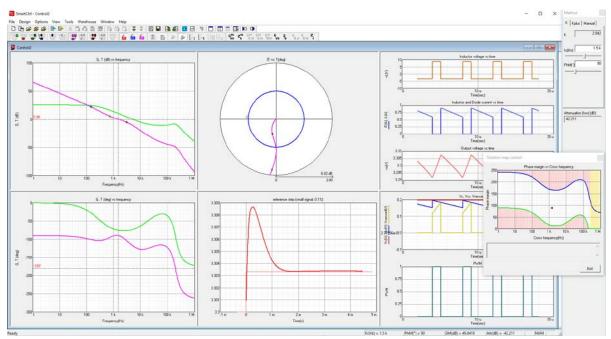


Figure 11: SmartCtrl analysis view

The design can be fully exported to Psim in case the user wants to simulate the design. To do this, just click in SmartCtrl exporting to Psim icon and configure the exportation. See Figures 12 to 15.

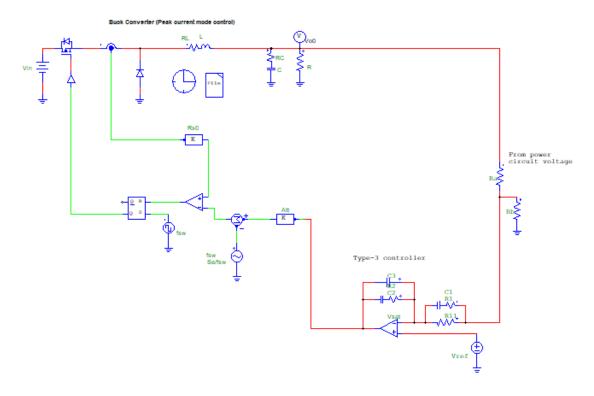
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B B #	ß	Ε÷	$[\![\frac{L}{T}_R$	[]]]]]]

Figure 12: Exporting to Psim button



Exporting options	×
Regulator exporting way Components (R1, C1, are given) Source of the statements (R1, C1, are given)	
C z domain coefficients	
 Power stage and sensors Initial conditions 	
Show files to be exported	
<u>H</u> elp <u>C</u> ancel <u>D</u> K	

Figure 13:Exporting to Psim options







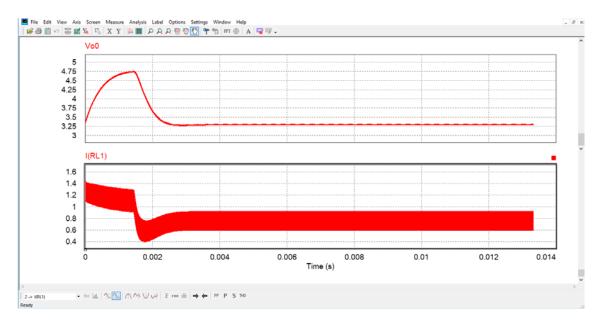


Figure 15:Psim simulation result



4. Bibliography

- [1] "Voltage-Mode, Current-Mode (and Hysteretic Control)", Microsemi Technical Note TN-203, Sanjaya Maniktala, 2012
- [2] "Fundamentals of Power Electronics", Robert W. Erickson and Dragan Maksimovic, Kluwer academic publishers, ISBN 0-7923-72-70-0.