

Boost PFC Converter Control Loop Design

Tutorial –December 2018-



How to Contact:

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1. Introduction

SmartCtrl is a general-purpose software specifically designed for power electronics applications. This tutorial is intended to guide you, step by step, to design the control loops of a PFC (power factor correction) boost converter with the SmartCtrl Software.

The example used in this tutorial is the PFC boost converter circuit that comes with the PSIM example set. The PSIM schematic is shown in Figure 1.

Figure 1: PFC required system

The circuit includes the inner current loop and the outer voltage loop. The current loop regulator parameters are the resistance R11, R2_i and the capacitances C2_i, C3_i; and the voltage regulator parameters are the resistance Rset and the capacitance Css and Ct, highlighted in the red boxes of Figure 1.

The objective of this tutorial is to design the current and voltage regulators using the SmartCtrl software. The design procedure is described below.

2. Open SmartCtrl

To begin the design process, in SmartCtrl, click on the icon highlighted in top part of Figure 2 or click on the icon of tool bar shown in bottom part of Figure 2.

SmartCtrl	×
Design a predefined topology	Open a
DC-DC power stage and control circuit design	default file
DC-DC converter - Single loop Voltage Mode Control or ACMC	recently saved file
DC-DC converter Peak current mode control	previously saved file
DC-DC converter Average Current Mode Control	sample design
PFC Boost converter	
Design a generic topology	Design a generic control system
s-domain model editor	Equation editor
Import frequency response data from txt file	Help <u>C</u> lose
	ost converter

Figure 2: Ways of accessing PFC design wizard

It can also be accessed with the **Design** menu, **Predefined topologies** ->**AC/DC converters** ->**PFC Boost converter**. Whatever the access selected, the window of Figure 3 will appear.

In Figure 3 it has been grouped all the fields depending if they are for inner or outer control loop.

Figure 3: PFC template structure

As it can be seen from Figure 3, the PFC boost converter is controlled by a double loop control scheme. The inner loop is a current loop, and the outer loop is a voltage loop. Note that the PFC boost converter design must be carried out sequentially. SmartCtrl program will guide you through this process.

3. Inner Loop Design

Before designing the inner loop, select the type of the multiplier.

1. Select the Multiplier UC3854A as shown in Figure 4.

Figure 4: Inner loop multiplier

Attending to the schematic in Figure 1, the parameters of the multiplier for this particular example are the ones shown in Figure 5.

Notice that KFF, the feed-forward gain, is the ratio between the rms input voltage and the average input voltage to the multiplier. It has been calculated applying [1].

$$KFF = \sqrt{2} \cdot \frac{2}{\pi} \cdot \frac{RFF3}{RFF1 + RFF2 + RFF3}$$
[1]

Where RFF1, RFF2 and RFF3 are the resistances with the same name which can be observed in the schematic of Figure 1.

The configuration of the UC3854A multiplier can be found in Figure 5.

UC3854A Multiplier		×
C KFF	KFF 0.01763	
AB C ² A Vea	Km 1.0	
	Rac(ohms) 910 K	
	Rmo(ohms) 10 K	
Set gefaults		Help Cancel QK

Figure 5: UC3854 multiplier

2. Select the gain of the inner loop current sensor. See Figure 6.

Select the value of the resistor which will act as the current sensor (Rs). This resistor is represented in the picture of the power plant.

Resistive sensor			\times
	Ri (Ohms) 0.25	(included in Plant schema)	x
Set defaults		Help Cancel QK	

Figure 6: inner loop current sensor

3. At this point, the inner current loop is almost defined as it can be seen in Figure 7. To finish this loop, it is necessary to define the plant topology. To do so, select a boost PFC (resistive load) plant.

Figure 7: Inner current loop almost defined

4. Configure the plant and the inner loop compensator

1. Select the Boost PFC (Resistive load) plant for boost PFC converter. Complete the parameters in the input data window as shown in Figure 8. <u>Note that the input voltage is in rms value</u>.

Boost PFC (Resistive load)		×
	Vin(rms)(V)	
	RL(Ohms) 10 m	
	L(H) 1.1 m	
	Rc(Ohms) 10 m	
	C(F) 450 u	
	Vo(V) 400	
	R(Ohms) 533.333	
	Po(W) 300	
	wta(*) 90	
	Fsw(Hz) 100 k	Line frequency (Hz) 50 💌
Set <u>d</u> efaults	Update read only boxes	<u>H</u> elp <u>C</u> ancel <u>O</u> K

Figure 8: Power plant parameters

Note that wta(°) is the line angle in degrees at which the plant operation point is calculated. The current loop is designed considering the plant calculated for this operating point. This line angle is indicated as a red dot in the output panel that represents the Rectified voltage and external compensator output.

When finished, click OK to continue.

2. Select a Type 2 as the current regulator as done in Figure 9 and configure it as it has been done in Figure 10.

Figure 9: Select a Type 2 for inner loop regulation

Figure 10: Type 2 parameters

It is necessary to know the ramp waveform (Figure 10) in order to specify the parameters Vp (maximum voltage), Vv (minimum voltage) and tr (rise time). These parameters configure the converter modulator whose gain is important in the inner loop calculation.

3. Select the crossover frequency and the phase margin with the help of the solution map. See Figure 11 and Figure 12.

Figure 11: Inner loop solution map accessing button

SmartCtrl provides a guideline and an easy way of selecting the crossover frequency and the phase margin through the Solution Map. See Figure 12.

Figure 12: inner loop solution map

In the Solution Map, each point within the white area corresponds to a combination of the crossover frequency and the phase margin that leads to a stable solution. In addition, when a point is selected, the attenuation given by the sensor and the regulator at the switching frequency is provided.

To carry out the selection, click a point within the white area, or it can be done manually by entering the crossover frequency and the phase margin and clicking in update.

In this design it has been selected a cross frequency of 1kHz and a Phase Margin of 50 degrees. This parameter pair will generate a -39dB of attenuation at switching frequency.

Once the crossover frequency and the phase margin are selected, the Solution Map will be shown on the right side of the converter input window. If, at any time, the user wants to modify the crossover frequency or the phase margin, just click on the white area of the Solution Map, as shown in Figure 13.

Figure 13: Inner loop solution map shortcut access

5. Outer Loop Design

The process of designing the outer loop is quite similar to the inner loop one.

1. Select the voltage sensor. In this particular example, the option which has been chosen is "Regulator embedded voltage divider". See Figure 14.

There is no need to define any other parameter in this sensor.

Figure 14: Outer loop sensor choice

2. Select the voltage regulator. See Figure 15.

Figure 15: Outer loop compensator choice

In this example, the regulator type is a "Single pole_unatt", with the parameters specified in Figure 16.

Single pole_unatt		×
Vref Par	R11(ohms) 10K Vref(V) 7.5	
	Vsat(V) 6.0	
Set gefaults		Help Cancel QK

Figure 16: Outer loop single pole compensator parameters

In this case three different compensator can be used:

- a) PI unattenuated it has an infinite gain at DC so it will reach the steady-state value. However, it will introduce a small distortion in the current waveform that will reduce the Power Factor coefficient.
- b) Type 2 unattenuated it is quite similar to the unattenuated PI; it has the almost same characteristics.
- c) Single pole it has a finite gain at DC so it will not reach the steady-state output voltage (it will be a few volts below the 400V reference); however, it will not distort the current waveform so it is used when unitary Power Factor coefficients are required.
- 3. Determine the crossover frequency and the phase margin.

The crossover frequency and the phase margin of the outer loop must be selected. A Solution Map is also provided to help select a stable solution. Press the Solution map (outer loop) button (Figure 17) and the solution map will appear (Figure 18).

Figure 17: Accessing the outer loop solution map

Figure 18: Outer loop solution map

Select a point by clicking within the white area, and click OK to continue. In this tutorial a cross frequency of 10Hz and a Phase Margin of 60 degrees have been selected.

Once the crossover frequency and the phase margin are selected, the Solution Map will appear on the right side of the converter input window. If, at any time, these two parameters need to be changed, just click in the white area of the Solution Map, as shown in Figure 19.

Figure 19: outer loop solution map shortcut access

4. Accept the selected design by clicking on OK.

The program will automatically show calculated control system. By means of Bode plots, Nyquist plot, etc. its stability and dynamic response can be checked.

6. Design results and interpretation

When the data input wizard finish, some panels appears so the user can check the dynamic response of the control already designed and adjust it. This window configuration can be seen in Figure 21.

SmartCtrl provides several analysis options:

- a) Check the steady state waveforms they are shown in the right part. They are quite useful to identify possible oscillations, noises or waveform distortions.
 For example, if PI compensator would have been chosen for the outer loop, a current distortion will appear in these traces. See Figure 21.
- b) Check the response to a small signal step It gives information about the response of the system, if it is underdammed or overdamped. See Figure 21.
- c) Check the bandwidth with the bode plots The crossover frequency in open loop is pretty close with the closed loop bandwidth. See Figure 21.
- d) Check the stability with the Nyquist plot it provides quick-understanding info about the stability of the system. See Figure 21.
- e) View the input and output reports. See Figure 20 and Figure 22.
- f) Perform a parametric sweep. See Figure 20 and Figure 23.
- g) Modify input data for inner loop, outer loop and plant. See Figure 20.
- h) Visualize data from input or output loop. See Figure 20.
- i) Export to Psim. This functionality has been covered in point 5.

Figure 20: SmartCtrl main utilities

Note that the solution map window is always enabled so the user is always capable of changing the pair Phase Margin – crossover frequency.

Figure 21: SmartCtrl main window for inner loop

ut data	×	Output data
UT DATA DC PFC double loop (inner loop)	^	RESULTS Compensator (Analog):
Frequency range (Hz) : (1, 999 k)	-	
Cross frequency (Hz) = 1 k Phase margin (°) = 50		R21 (Ohms) = 4.90067 k
Plant	_	C2i (F) = 88.9699 n C3i (F) = 13.6769 n
Boost (LCS_VMC) PFC	-	fzl (Hz) = 365.024
R (Ohms) = 533.333		fz2 (Hz) = 365.024
L (H) = 1.1 m		fpl (Hz) = 2.73955 k
RL(Ohms) = 10 m		fp2 (Hz) = 2.73955 k
C (F) = 450 u		fi (Hz) = 155.051
RC(Ohms) = 10 m		
Vin (V) = 230		
Wta () = 90		$b_2 = (5 2) = 0$ $b_1 = 0.000426012$
$VO_{(V)} = 400$		bi (s) = 0.000436013
FSW(HZ) = 100 k		50 - 1
node = Continuous		$-2 (-c^2) = 0$
C		a3 (5 3) = 5 9622e=009
Sensor	_	$a_2 (s_2) = 0.00102647$
		a0 = 0
Compensator		Ct (F) = 1.38709 n
	-	Rset (Ohms) = 8.5 k
Type 2		
Gmod = 0.157204		Loop performance parameters:
R11i(Ohms)= 10000		
Vp(V) = 6.502		
Vv(V) = 1.095		PhF (Hz) = out of frequency range
tr(sec) = 8.5e-006		GM (dB) =
		Atte(dB) = -50.7277
	\lor	Voest(V) = 447.825
	>	< >
	. 1	Evit

Figure 22: input/output data report

	nensalor	
Boost PFC with n	existive load	
Value	Minimum	Masimum
230	115	345
10 m	5 m	15 m
1.1 m	550 u	1.65 m
10 m	5 m	15 m
450 u	225 u	675 u
400	200	600
300	150	450
100 k	50 k	150 k
	Boost PFC with m Value 280 10 m 1.1 m 10 m 400 r 400 r 300 r 100 k	Boost FFC with resultive load Value Minimum 200 1115 100 m 5 m 1.1 m 550 G 100 m 5 m 450 u 225 u 400 200 300 1150 100 k 50 k

Figure 23: Parametric sweep of inner loop plant parameters

The Bode plots and Nyquist plot corresponding to the inner loop are shown in Figure 21, as well as the graphical information regarding the outer loop is shown in Figure 24. In the right panel "Method", three parameters appear:

- Attenuation (fsw)(dB). This is the attenuation in dB achieved by the open loop transfer function at the switching frequency. It should be low enough for the inner loop and the outer loop. Preferably lower than -50dB.
- Loop gain (2fl)(dB). This is the attenuation in dB achieved by the open loop transfer function at twice the line frequency (100 Hz or 120 Hz). It should be high for the inner loop and low for the outer loop.

• Stim. Vo (V). As the outer loop compensator is a single pole, it has not enough low frequency gain to archive the reference value. That is why SmartCtrl provides the output voltage value obtained with this compensator.

By clicking with the right button on the line current panel, a floating menu appears, offering different choices. One of them is the command FFT, which displays a new window with a plot that shows the amplitude of the first and third harmonics of the line current, to provide more information regarding the harmonic distortion. See Figure 25.

Figure 24: SmartCtrl main window for outer loop

Figure 25: line current FFT 1st and 3rd harmonics

The red dot in the rectified line voltage plot of Figure 26 originally corresponds to the line angle wta specified in the plant window (Figure 8). This dot can be moved by clicking and dragging, and the Bode plot and the attenuation parameters will refresh, as the plant is recalculated considering the equivalent DC/DC converter for that particular operating point. An example is depicted in Figure 27, modifying the line angle. Notice how the **open** loop transfer function.

Figure 27: wta parameter sweep and its effect in <u>open</u> loop

The blue dot in the rectified line voltage plot (Figure 26) is placed in the line angle that corresponds to the maximum current ripple through the inductor. Some results obtained by simulating the schematic in Figure 1 are depicted in Figure 28.

To illustrate the meaning of this blue dot. In the left part of Figure 28, the voltage at the output of the rectifier and the current through the inductor are shown, indicating the position of the blue dot.

In the right part of the figure, a detail of the same waveforms is shown, as well as the oscillator ramp and the internal compensator output.

The plot that shows the oscillator ramp and the inner compensator output is useful to determine whether there could be oscillations. If the slopes of both functions are too similar, there could be more than one intersection per period, causing oscillations.

Figure 28: Detail of the blue dot of the rectified line voltage view

When a single-pole is used as the compensator type of the outer loop, there are some advantages regarding the line current distortion. On the other hand, <u>the actual output</u> <u>voltage may not be exactly the specified</u> due to the low gain at low frequency. This causes some differences between the SmartCtrl results and the simulated results. This problem can be easily compensated by the user by increasing the output voltage reference.

However, if the actual output voltage is 10% higher than the specified one, SmartCtrl will provide a warning message, recommending the user to check this point and increase low frequency gain. In this particular example, the actual output voltage is 415 V instead the specified 400 V, and consequently there is not any warning message.

To illustrate this problem related with the low gain of the outer loop at low frequency, a new outer loop has been design, with different phase margin (PM) and cross-over frequency (fc).

The comparison between this design and the original one can be found in Table 1. The new design has a lower gain at low frequency and the measured output voltage is 448V, that is, more than 10% higher than the specified value. See Figure 29.

Original des	ign	New design	
Inner loop (type 2)	fc=15 kHz	Inner loop (type 2)	fc=15 kHz
	$PM=60^{\circ}$		$PM=60^{\circ}$
Outer loop (single-pole)	fc=25 Hz	Outer loop (single-pole)	fc=15 Hz
	$PM = 40^{\circ}$		$PM=60^{\circ}$
Specified output voltage	400 V	Specified output voltage	400 V
Actual output voltage	415 V	Actual output voltage	448 V

Table 1: Original design and new design

Figure 29: Gain at low frequency with two different designs

Regarding the inner control loop, it is very important to consider that it is necessary to have a high enough bandwidth in order to follow the rectified sinusoidal reference. If the cross-frequency of the current loop is not high enough, a zero-crossing distortion in the input current will happen.

In these occasions, the results provided by SmartCtrl may not match the actual results, as the line current waveform is calculated by SmartCtrl assuming that the current loop follows perfectly well the reference generated by the outer loop.

Consequently, when a zero-crossing distortion is expected, the program displays a warning message to inform the user that the actual line current would differ from the one represented. The cross-frequency of the inner loop compensator should be increased to minimize this problem.

To illustrate this problem related with the low cross-over frequency of the inner loop, a comparison between several designs of the inner loop with different phase margin (PM) and cross-over frequency (fc). The input current waveforms achieved with these designs are compared in Figure 30.

Notice the important zero-crossing distortion for cross-over frequency lower than 5 kHz, and how the distortion is minimized as the cross-frequency is increased.

Figure 30: Zero-crossing distortion with different compensators in the current loop

7. Export and simulate with Psim

1. Click in SmartCtrl exporting to Psim button. See Figure 31. And configure the exportation as shown in Figure 32.

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Figure 31: SmartCtrl exporting to Psim button

Expor	ting options	×
Γ	Regulator exporting way	
	Components (R1, C1, are given)	
	C s domain coefficients	
	C z domain coefficients	
L	✓ Power stage and sensors	
	Initial conditions	
	Show files to be exported	
	Help Cancel OK	

Figure 32: SmartCtrl exporting to Psim options

2. In Psim, the schematic of Figure 33 will appear, if simulation is launched, the waveforms of Figure 34 will appear.

Figure 33: Psim schematic created by SmartCtrl

As it can be seen, the schematic of Figure 33 is exactly the objective of this tutorial. In Figure 34, it appears the output voltage and the rectified input current.

As it can be seen, his current has no any distortion or ripple and the output voltage is exactly what was specified in SmartCtrl.

Figure 34: Traces of the Psim simulation