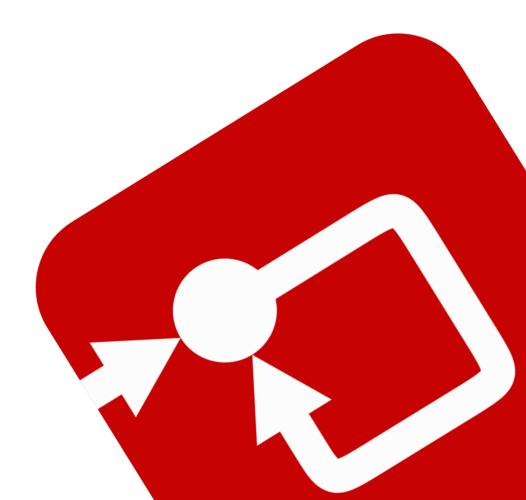


Digital Control Double Loop Design

Tutorial –December 2018-



How to Contact:

 $\mathbf{\Sigma}$

(a)

info@powersmartcontrol.com

www.powersmartcontrol.com

SmartCtrl Copyright © 2015-2018 Power Smart Control S.L.

All Rights Reserved.

No part of this tutorial may be reproduced or modified in any form or by any means without the written permission of Power Smart Control S.L.

Notice

Power Smart Control tutorials or other design advice, services or information, including, but not limited to, reference designs, are intended to assist designers who are developing applications that use SmartCtrl; by downloading, accessing or using any particular Power Smart Control resource in any way, you (individually or, if you are acting on behalf of a company, your company) agree to use it solely for this purpose and subject to the terms of this notice.

Power Smart Control reserves the right to make corrections, enhancements, improvements and other changes to its resources.

You understand and agree that you remain responsible for using your independent analysis, evaluation and judgment in designing your applications and that you have full and exclusive responsibility to assure the safety of your applications and compliance of your applications with all applicable regulations, laws and other applicable requirements.

Disclaimer

Power Smart Control S.L. (PSC) makes no representation or warranty with respect to the adequacy or accuracy of this documentation or the software which it describes. In no event will PSC or its direct or indirect suppliers be liable for any damages whatsoever including, but not limited to, direct, indirect, incidental, or consequential damages of any character including, without limitation, loss of business profits, data, business information, or any and all other commercial damages or losses, or for any damages in excess of the list price for the licence to the software and documentation.







General Index

1. Introduction	3
2. Inner loop design	3
3. Outer loop design	6
4. Discretize the compensators	7

Figure Index

Figure 1: SmartCtrl initial window	. 3
Figure 2: plant parameters	.4
Figure 3: Sensor parameters	.4
Figure 4: compensator parameters	. 4
Figure 5: solution map point	. 5
Figure 6: outer loop sensor	. 6
Figure 7: outer loop compensator	. 6
Figure 8: outer loop solution map	. 6
Figure 9: Discretise tool in SmartCtrl	. 7
Figure 10: discretizing parameters for inner and outer loop	. 7
Figure 11: SmartCtrl export to Psim button	. 7
Figure 12: exporting options	. 8
Figure 13: Psim exported schematic	. 8
Figure 14: Time domain simulation result	. 8
Figure 15: Inner open loop gain measurement	. 9
Figure 16: Inner open loop gain measurement result	. 9
Figure 17: selecting the inner loop in SmartCtrl	. 9
Figure 18: importing data wizard	10
Figure 19: SmartCtrl open loop gain of inner loop comparison	11



1. Introduction

SmartCtrl is a design software specifically designed for power electronics application. This tutorial is intended to guide you, step by step, to design the digital control loop of a buck converter and simulate it with PSIM. This document is the second part of the document "Discrete Digital Control Loop Design".

In this document, a double loop control stage has been designed. To do so, part of the design already done in the tutorial "Discrete Digital Control Loop Design" has been used.

2. Inner loop design

Open SmartCtrl and choose a DC-DC converter averaged current mode control. See Figure 1 and select a buck LCS_VMC topology.

Configure the inner loop with the following parameters:

- a) Plant: select a buck LCS_VMC topology. See Figure 2.
- b) Sensor: select a Hall effect sensor. See Figure 3.
- c) Compensator: select a Type 2. See Figure 4.
- d) Solution map: select fc=2kHz and PM=40 degrees. See Figure 5.

At this point, the inner control loop is fully defined.

SmartCtrl	Х
Design a predefined topology	Open a
DC-DC power stage and control circuit design	default file
DC-DC converter - Single loop Voltage Mode Control or ACMC	recently saved file
DC-DC converter Peak current mode control	previously saved file
DC-DC converter Average Current Mode Control	sample design
PFC Boost converter	
Design a generic topology	Design a generic control system
s-domain model editor	Equation editor
Import frequency response data from txt file	Help <u>C</u> lose

Figure 1: SmartCtrl initial window



Buck (LCS_VMC)	×	
Vin RL C Rc R+ Vo Vin C <td< td=""><td>Vin(V) Image: Constraint of the second s</td><td></td></td<>	Vin(V) Image: Constraint of the second s	
Set defaults	Update read only boxes <u>H</u> elp <u>Cancel</u>	

Figure 2: plant parameters

Hall effect sensor		×
H(s)	Gain (V/A) 250 m fphall (Hz) 10 k	
Set defaults		<u>H</u> elp <u>C</u> ancel <u>O</u> K

Figure 3: Sensor parameters

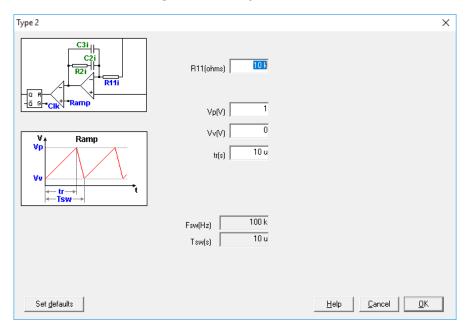


Figure 4: compensator parameters



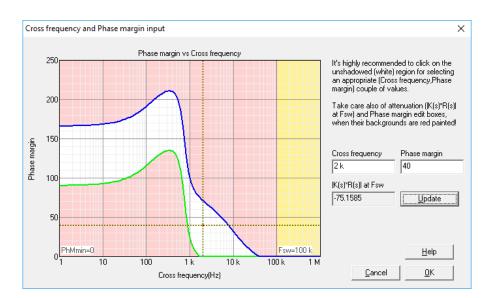


Figure 5: solution map point

It is used a Hall effect sensor as antialiasing filter since the quantity that is sampled (current trough the inductor) has a high ripple, when sampling under the Nyquist frequency (typically the switching frequency), antialiasing filter should be used, or an adequate synchronization with the ripple waveform must be ensured.

In this case, the pole frequency of the Hall effect sensor is 10 kHz as it can be seen in Figure 3.

After selecting plant, sensor and regulator (modulator) parameters, the cross over frequency fc and the phase margin PM desired for the inner control loop are selected using the graphical aid of the Solution Map



3. Outer loop design

This design procedure is quite similar to the one done in tutorial "Discrete Digital Control Loop Design", so the details has not been covered in full depth.

Configure the outer loop with the following parameters:

- a) Sensor: select a voltage divider sensor. See Figure 6.
- b) Compensator: select a Pl. See Figure 7.
- c) Solution map: select fc=1kHz and PM=100 degrees. See Figure 8.

At this point, the outer control loop is fully defined.

Note that the outer loop compensator does not include any information regarding the modulator as the modulator is included in the inner loop.

Voltage divider	×
Ra	Gain 208.333 m Calculate Gain=Vref/Vo from Vref
Vref Rb	Vo(V) 12
<u> </u>	Vref(V)
Set <u>d</u> efaults	<u>H</u> elp <u>Cancel</u> <u>O</u> K

Figure 6: outer loop sensor

PI		×
R2 C2 Vref	R11(ohms)	
Set <u>d</u> efaults		<u>H</u> elp <u>C</u> ancel <u>O</u> K

Figure 7: outer loop compensator

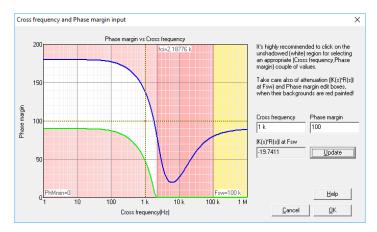


Figure 8: outer loop solution map



4. Discretize the compensators

At this point, analog control loop has been calculated. Then, by clicking in the "Digital settings" icon, the dialog box asking for digital loop parameters (sampling frequency, bits number and accumulated delay) appears. See Figure 9 and Figure 10.



Figure 9: Discretise tool in SmartCtrl

Note that different parameters can be used for the inner loop and the outer loop. In this case, both loops have the same sampling frequency (equal to the switching frequency), the same number of bits (16) and the same accumulated delay. By checking the check-box "Calculate digital compensator" and clicking in the "OK" button, both inner and outer digital regulators are calculated.

Digital control settings	×
Calculate digital compensator	
Outer loop	Inner loop
Sampling frequency (Hz)	Sampling frequency (Hz)
Bits number 16	Bits number 16
Accumulated delay (s) 10 u	Accumulated delay (s) 10 u
Help Cancel	

Figure 10: discretizing parameters for inner and outer loop

The button "export to PSIM (schematic)" allows exporting the entire design to PSIM (see the document "Digital control loop design" for more detail. See Figure 11 and Figure 12. The exported schematic is shown in Figure 13.

-	¥	10 01	. 4	•	Ð	- -	•	
т <mark>бос</mark>	ĪV		8	s	Þ	Etr	$[{}^{\rm L}_{\rm TR}$	[⊥ to

Figure 11: SmartCtrl export to Psim button



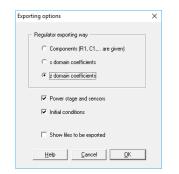


Figure 12: exporting options

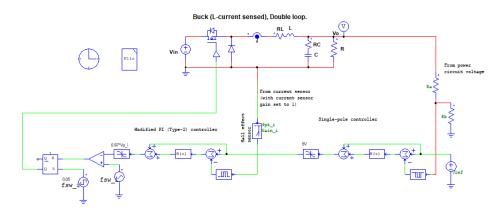


Figure 13: Psim exported schematic

The result of the time domain simulation can be seen in Figure 14. It can be seen how the output voltage is exactly 14V which is the value specified in SmartCtrl.

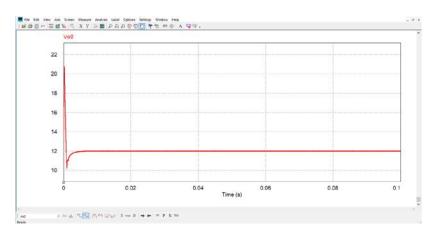


Figure 14: Time domain simulation result

In order to simulate the digital open loop transfer function corresponding to the inner loop, more additional elements are added to the schematic. First, the outer loop is disabled, and then an adder, a sinusoidal voltage source and an AC probe are added to perform the AC sweep and measure the current loop. See Figure 15 and Figure 16.



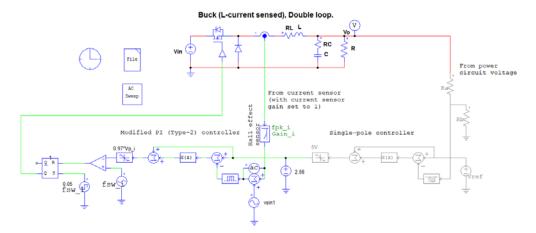


Figure 15: Inner open loop gain measurement

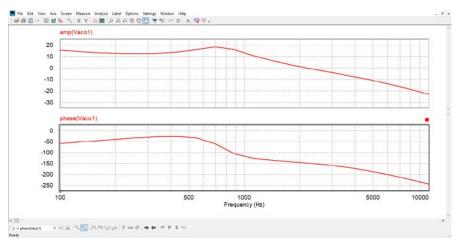


Figure 16: Inner open loop gain measurement result

Save the data with **File** -> **save as** -> Psim_inner_loop_Ac_sweep.**txt**

In the SmartCtrl project select the inner loop (Figure 17) and click in **File** -> **Import** (see Figure 18).

¥		8					
бс.	Ī		Ba	s	Þ	$\left\lfloor \frac{1}{T} \right\rfloor$	Ę

Figure 17: selecting the inner loop in SmartCtrl



dd function						2
Function type -	– Digital C Rz(f)	 file	function from tro file [e; Jsers\Jorge\Desk		Paste	C
C K(f)*R(f) C T(f) C CL(f) C Generic	☞ Tz(f) ○ CLz(f)	# 14 15 16 17 18 19	Freq(Hz) 2.98e+003 3.79e+003 4.83e+003 6.16e+003 7.85e+003 1.00e+004	Mod(dB) -3.99 -7.16 -10.54 -14.27 -18.43 -23.08	Phase(*) -158.81 -170.67 -185.41 -203.01 -223.22 -245.83	
Function color	Select	Commer	nt		>	~

Figure 18: importing data wizard

In Figure 19 it has been compared open loop gain of inner loop:

- a) Analog system -> dark pink trace
- b) Discretized system -> light pink trace
- c) Psim measured -> green trace

It can be seen how all of them are equal at cross frequency and quite similar until half of switching frequency.



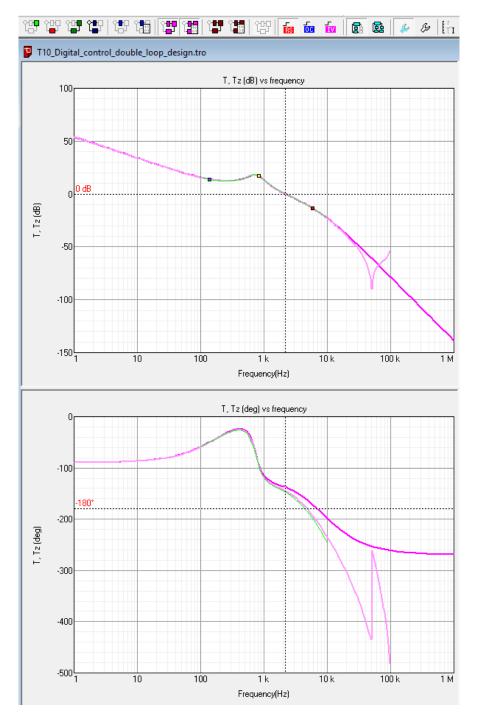


Figure 19: SmartCtrl open loop gain of inner loop comparison