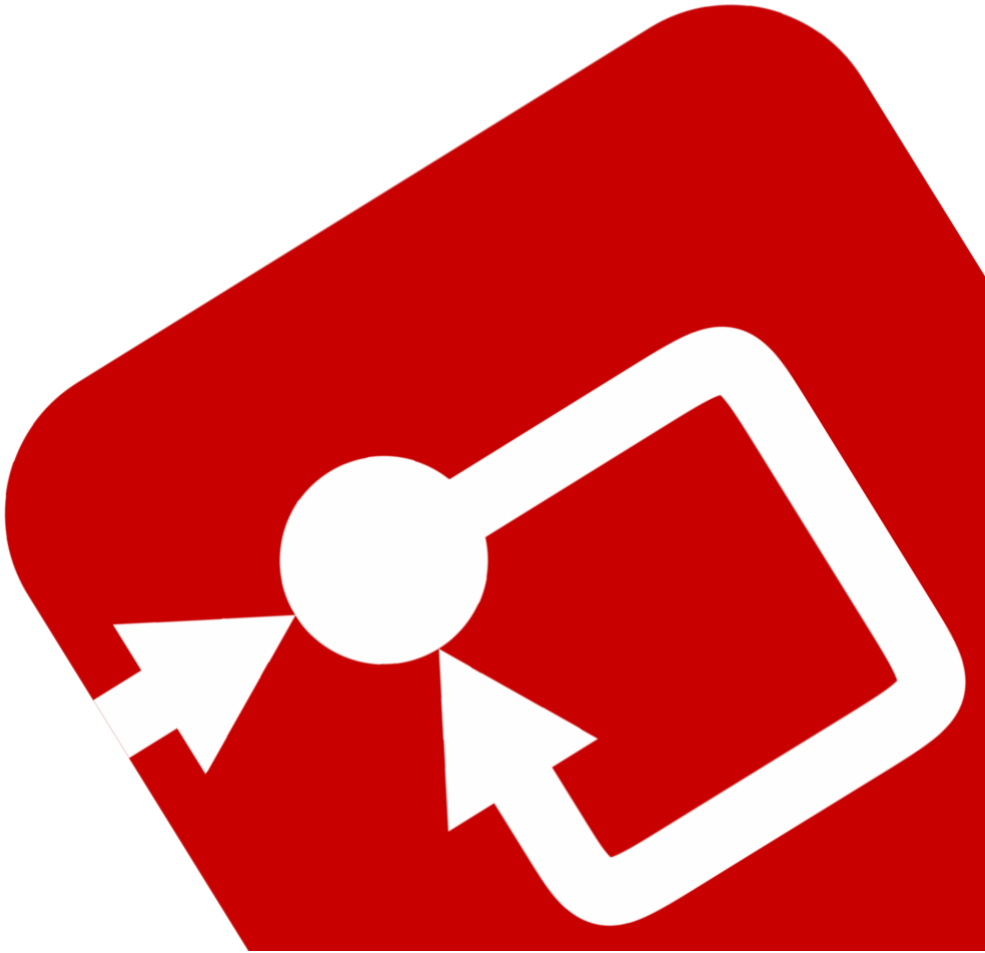
smart ctrl

control design for power electronics

DQ control of Three Phase PFC Boost Converter

Tutorial – February 2025 -



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1. Introduction

This tutorial is intended to guide you, step by step, to design the outer and inner control loop in dq axis of a Three Phase PFC Boost converter.

The selected converter for this example is the Three Phase PFC Boost converter with L filter. See Figure 1.

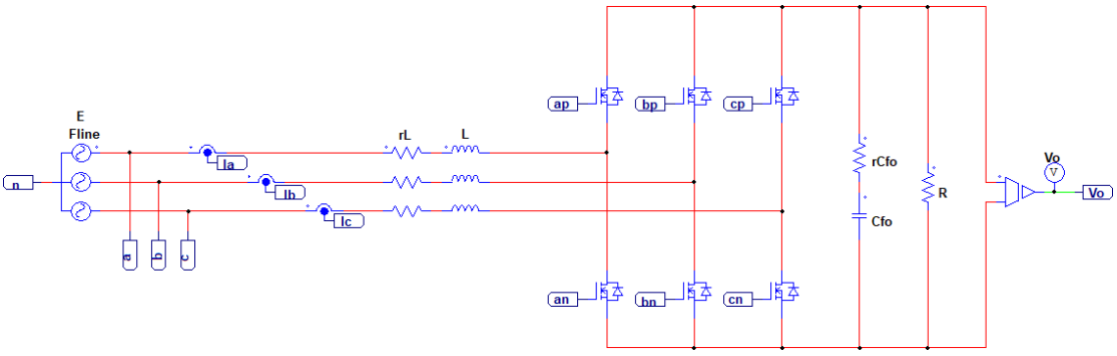

Figure 1: Power Stage

There are a lot of possibilities to design the control loop of the Three Phase PFC Boost converter. One of them is the conventional control using axis decoupling by means of feedforward loops as shown in Figure 2.

The inner loop regulates the current through the inductance and the outer loop regulates the output voltage.

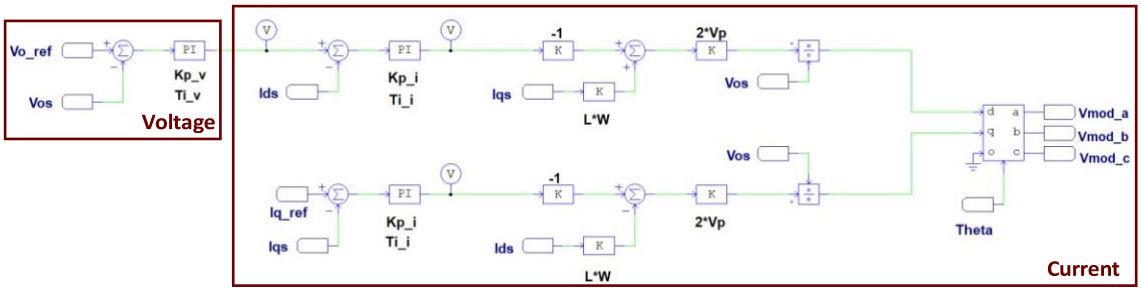

Figure 2: Outer and inner loop with feedforward axis decoupling

The Phase-Locked Loop (PLL) is another stage to be designed in this tutorial. The PLL selected is known as Synchronous Reference Frame Phase-Locked Loop (SRFPLL).

The PLL control structure has a PI compensator and an integrator that works as VCO. See Figure 3.

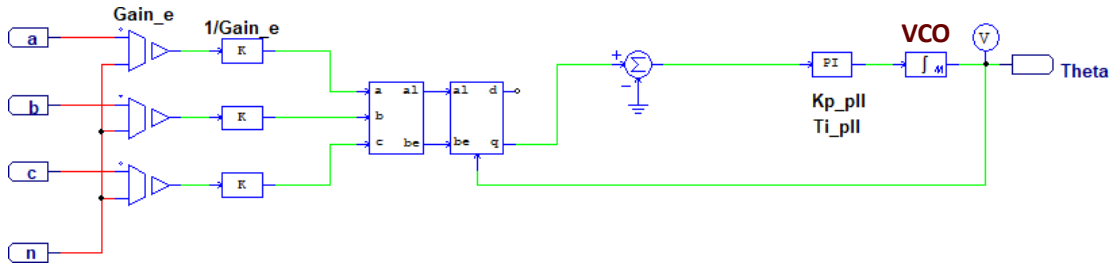

Figure 3: Synchronous Reference Frame Phase-Locked Loop (SRFPLL)

Finally, space vector modulation will be chosen, which consists of generating a zero-sequence signal (ZSS). The result of this modulation is equivalent to an injection of the third harmonic. One of the possible implementations is shown in Figure 4.

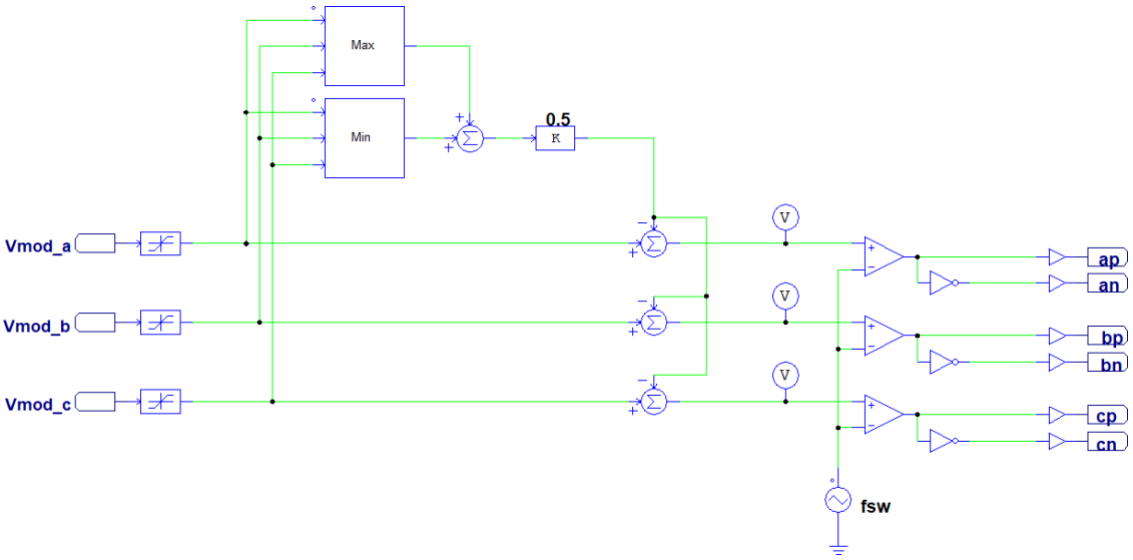

Figure 4: Space Vector modulator (SVPWM)

2. Converter design

1. Open your SmartCtrl Software.
2. To begin the design of a Three Phase PFC Boost converter, click on *Three-Phase PFC Boost converter*. See Figure 5.

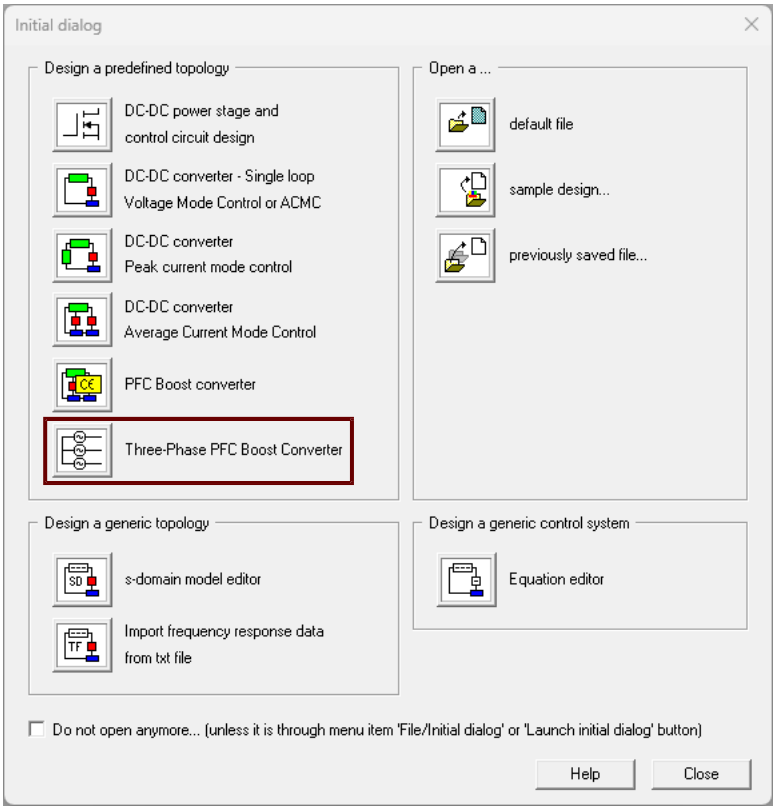

Figure 5: SmartCtrl initial window

3. It can also be accessed with:
   a) Button 
   b) Select the corresponding option within the Design menu. See Figure 6.

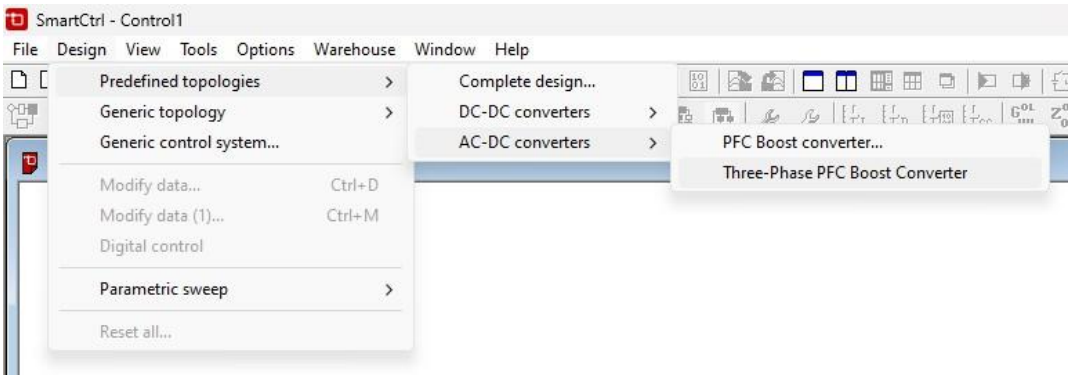

Figure 6: Alternative access to design a Three Phase PFC Boost Converter

4. The first window that appears is the Single-Line diagram (SLD). See Figure 7.
   This window can also be accessed by clicking on button **SLD**.
   The single line diagram allows the user to configure different types of control, modulators, loads and filters.

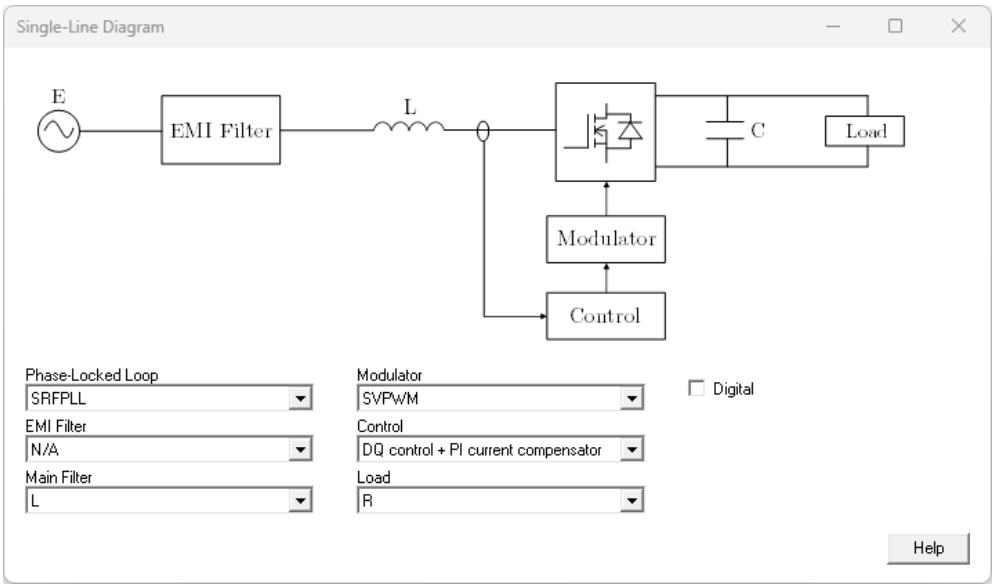

Figure 7: Single-Line diagram window

5. To access the power stage window, click on the button **PS**.
   Complete the parameters of the plant and the click on OK. See Figure 8.

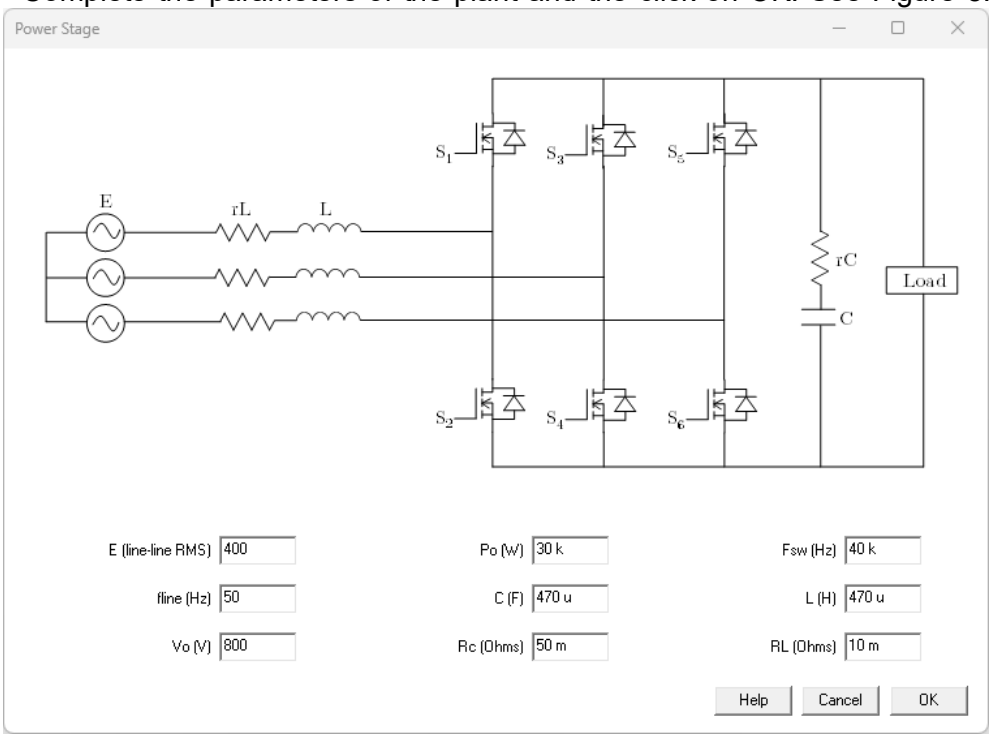

Figure 8: Power Stage window

6. To access the current sensor window, click on the button H_i.
   Enter the gain and bandwidth of the current sensor. See Figure 9.
   The “Unity Gain Feedback” checkbox calculates the inverse gain of the current sensor. Therefore, the control loop operates with actual values.
   Finally, click on button OK.

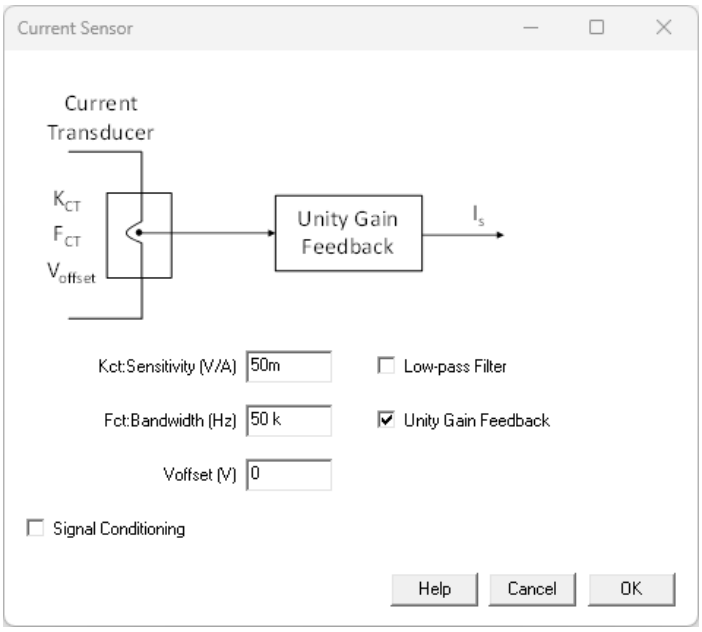

Figure 9: Current sensor window

7. To access the grid voltage sensor window, click on the button H_E.
   Enter the gain of the grid voltage sensor. See Figure 10.
   Finally, click on button OK.

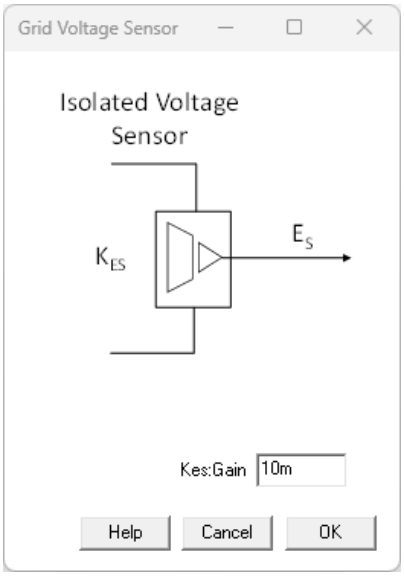

Figure 10: Grid voltage sensor window

8. To access the output voltage sensor window, click on the button H_V. Enter the gain and bandwidth of the output voltage sensor. See Figure 11. The “Unity Gain Feedback” checkbox calculates the inverse gain of the output voltage sensor. Therefore, the control loop operates with actual values. Finally, click on button OK.

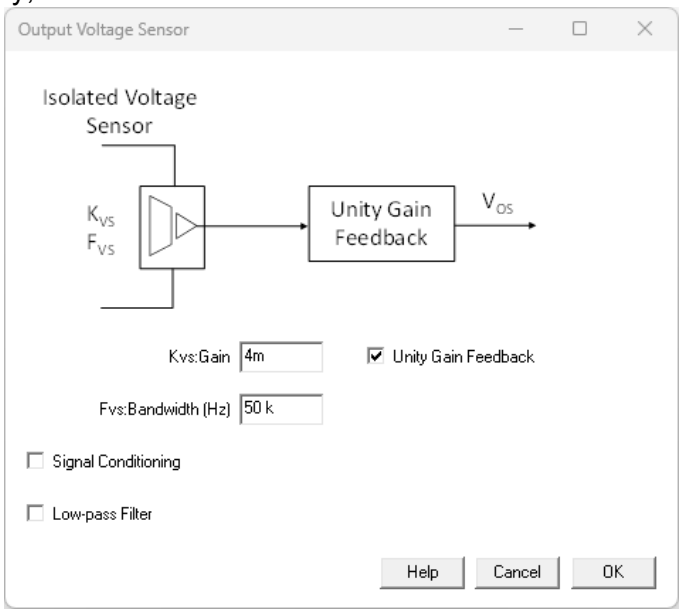

Figure 11: Output voltage sensor window

9. To access the modulator window, click on the button MOD. Enter the peak value of the carrier signal. See Figure 12. Finally, click on button OK.

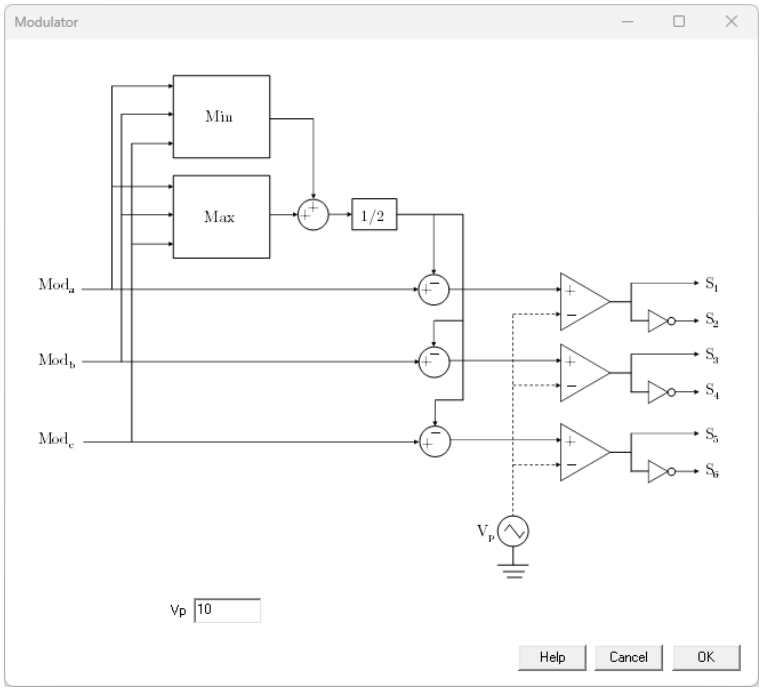

Figure 12: Modulator window

10. To design the inner current loop, it is recommended to open the current compensator window by clicking on the button Ci. Additionally, we open the solution map by clicking on the button SM Ci. Finally, we open the bode diagrams by clicking on the button . See Figure 13.
In the bode plot window, the frequency response of the current plant is displayed by clicking on the Gi button, the frequency response of the open-loop transfer function is displayed by clicking on the Ti button and the frequency response of the closed-loop transfer function is displayed by clicking on the G_i^{CL} button.

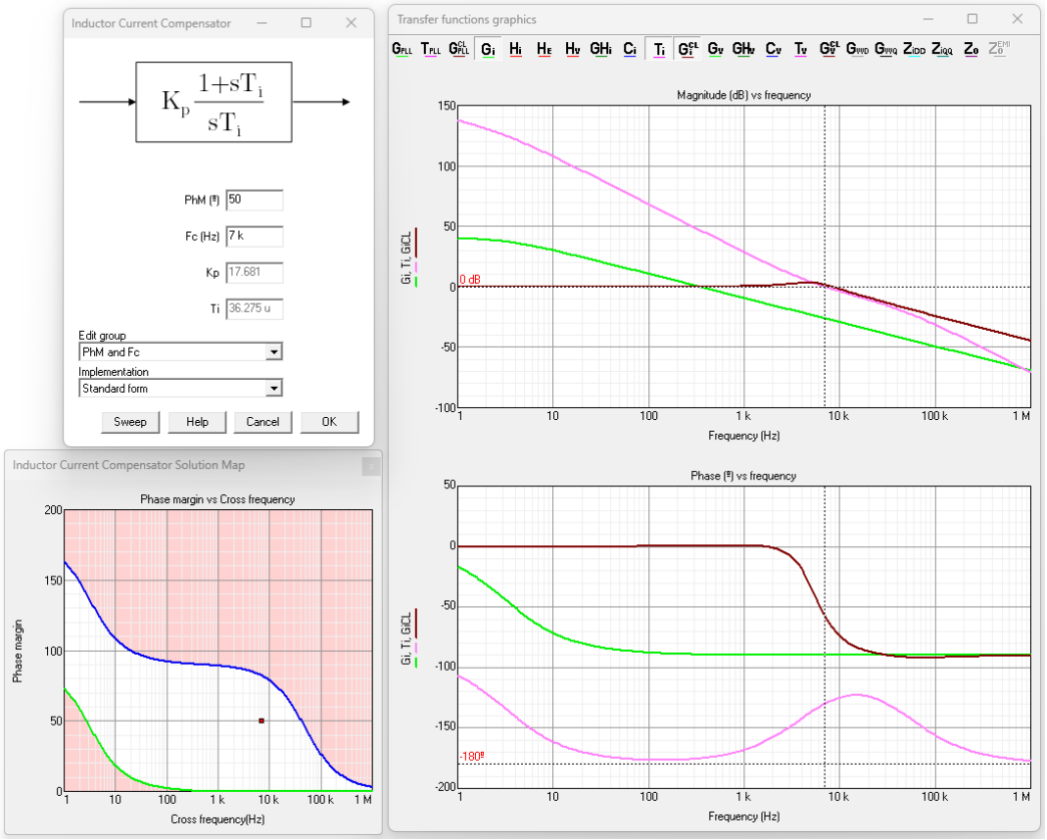

Figure 13: Inner current loop design

The bandwidth of the control loop can be adjusted by directly entering the value of the crossover frequency and phase margin or by using the solution map. In this tutorial, we select a crossover frequency equals to 7kHz and phase margin of 50º.

A remark should be done: the solution map window shows all the pairs Phase Margin – cross Over Frequency. All the ones contained in the white area will

generate a perfectly stable controller. On the contrary, if chosen in the red area the controller will almost for sure be unstable.

11. To design the outer loop, it is recommended to open the voltage compensator window by clicking on the button C_v. Additionally, we open the solution map by clicking on the button SM Cv. See Figure 14.
In the bode plot window, the frequency response of the voltage plant is displayed by clicking on the G_v button, the frequency response of the open-loop transfer function is displayed by clicking on the T_v button and the frequency response of the closed-loop transfer function is displayed by clicking on the G_v^{CL} button.

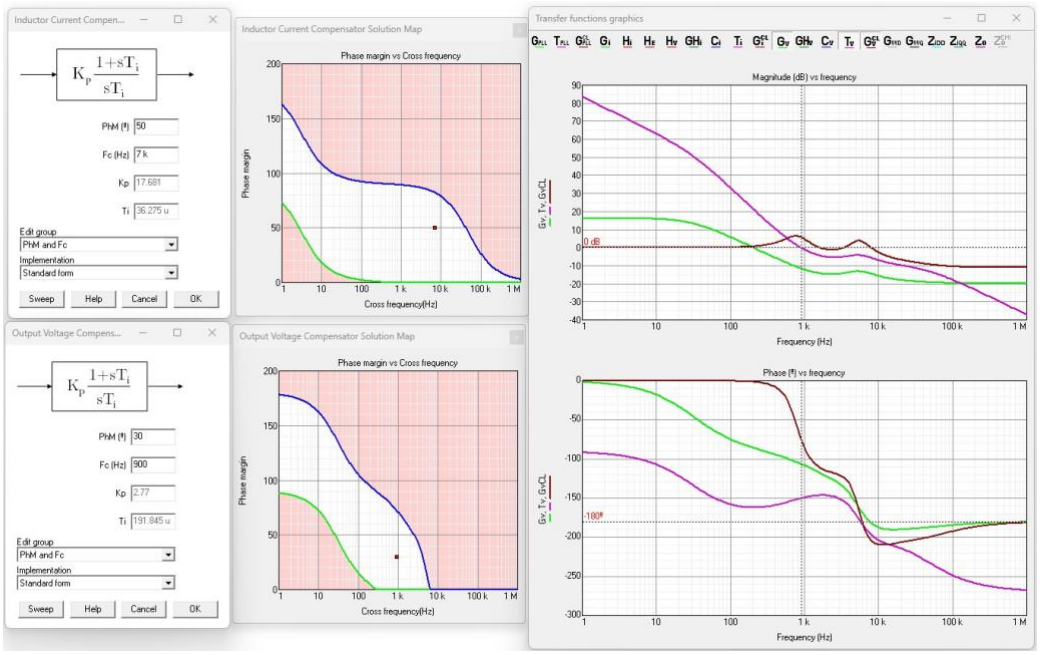

Figure 14: Outer voltage loop design

The bandwidth of the control loop can be adjusted by directly entering the value of the crossover frequency and phase margin or by using the solution map. In this tutorial, we select a crossover frequency equals to 900Hz and phase margin of 30º.

12. To access the phase-locked loop window, click on the button PLL.
The bandwidth of the control loop can be adjusted by directly entering the value of the crossover frequency and phase margin or by defining the stabilization time, t_s, and the damping ratio or by defining the values of K_p and T_i. See Figure 15.

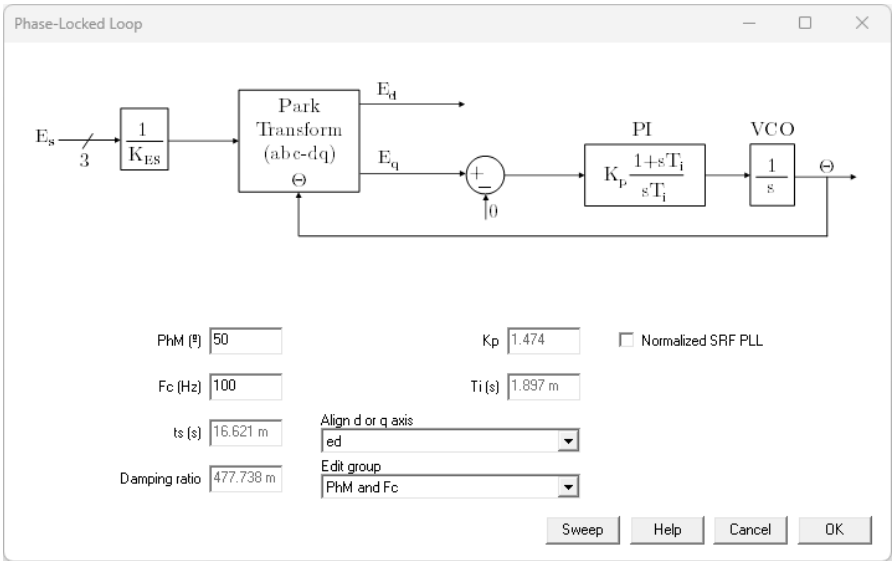

Figure 15: Phase-Locked Loop window

Another option to adjust the control loop of the PLL is to use the solution map  . In this tutorial, we select a crossover frequency equals to 100Hz and phase margin of 50º. See Figure 16.

In the bode plot window, the frequency response of the PLL plant is displayed by clicking on the  button, the frequency response of the open-loop transfer function is displayed by clicking on the  button and the frequency response of the closed-loop transfer function is displayed by clicking on the  button.

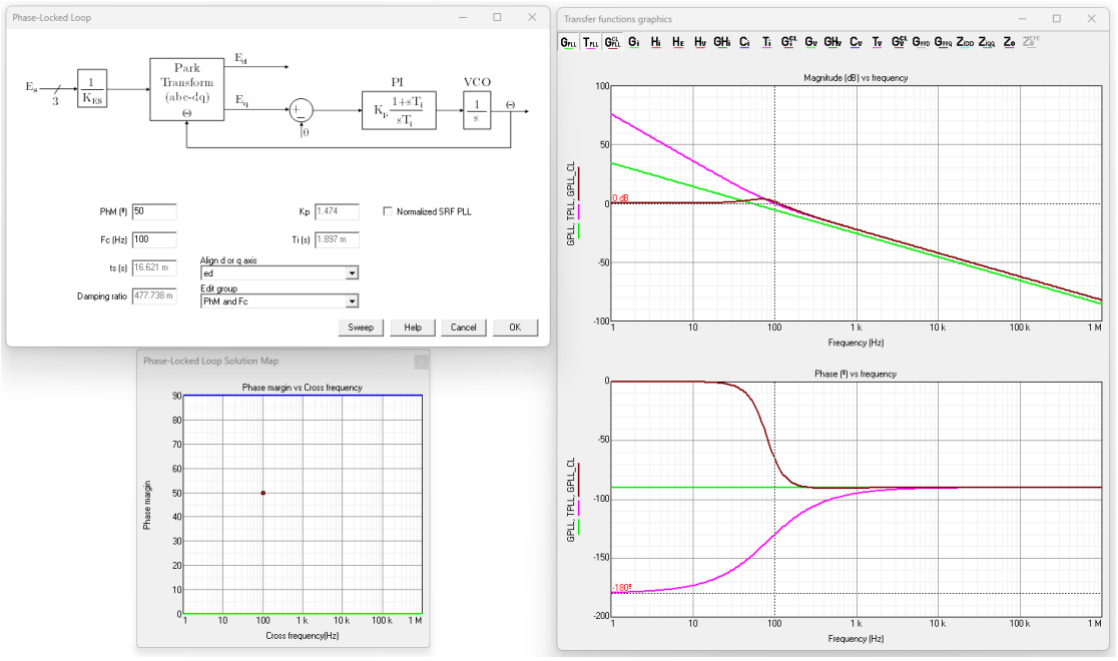

Figure 16: Phase-Locked loop design

By clicking on the PLL button the transient response of the PLL is displayed. See Figure 17.

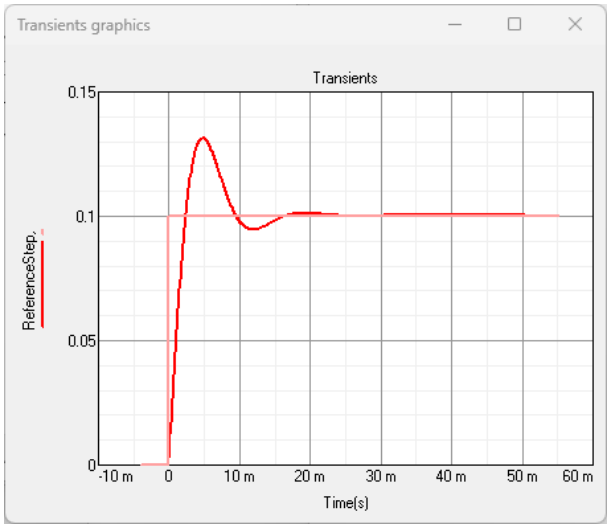

Figure 17: Transient response of PLL

13. Once all the control loops have been designed, the input and output reports can be obtained. See Figure 18.

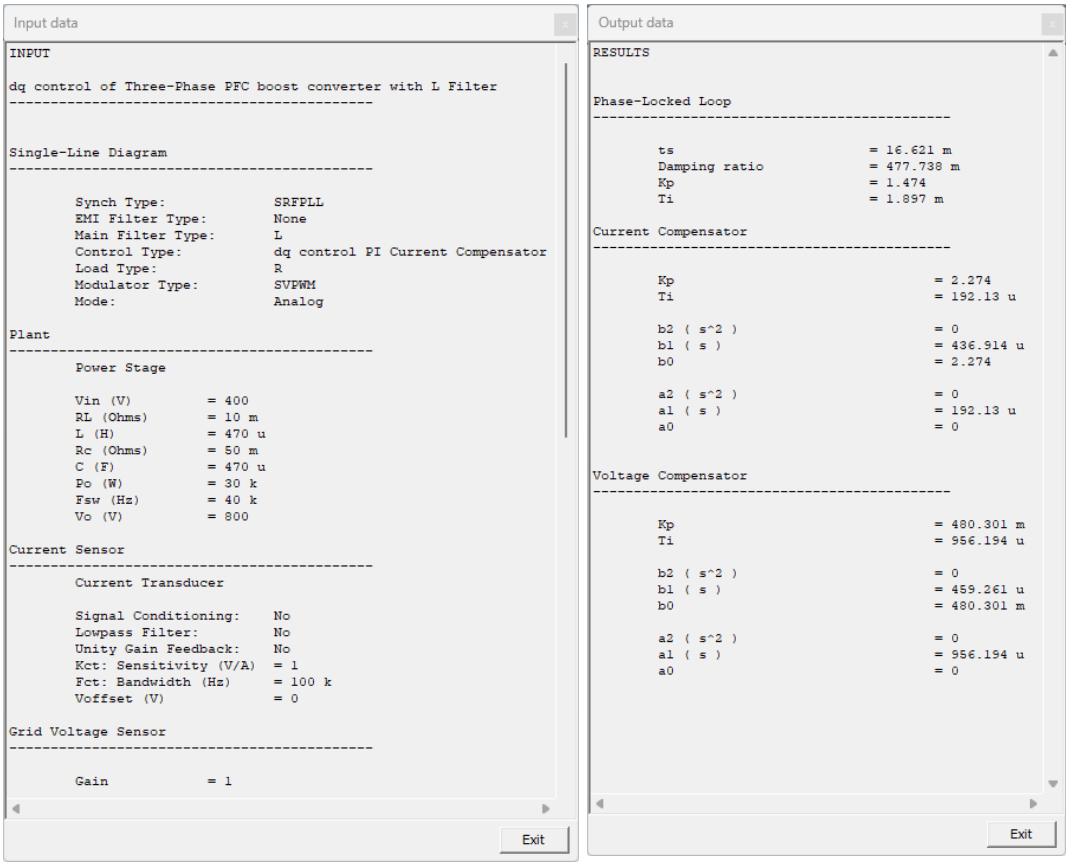

Figure 18: Input and output data reports

3. Design exportation to PSIM

To export to PSIM click on this button. See Figure 19.

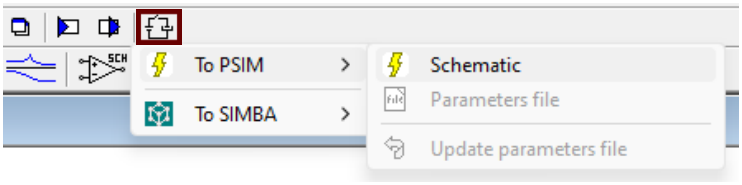

Figure 19: Exportation to PSIM button

And configure the exportation. See Figure 20.

- "s-domain coefficients": the schematic and parameters of the compensator will be exported in the form of PSIM control blocks.
- "C code": the power stage and the sensing stage will be exported in the form of PSIM control blocks. The control stage and modulator will be exported in a DLL.

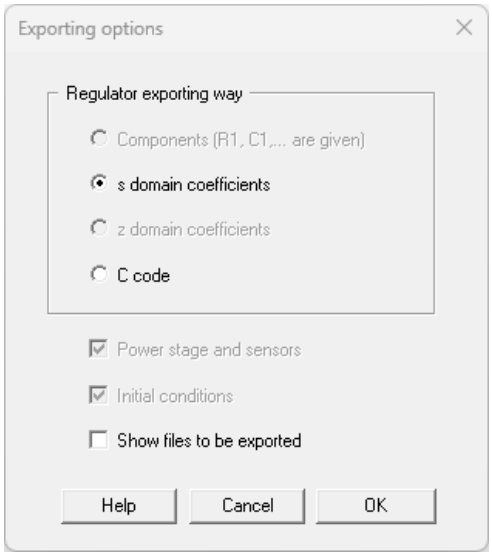

Figure 20: Exportation to PSIM settings

In this tutorial, we select the "s-domain coefficients" option. Then, click OK and PSIM will be automatically opened, and the simulation launched.

4. Design validation

In PSIM, the following system has been automatically created and configured by SmartCtrl. See Figure 21.

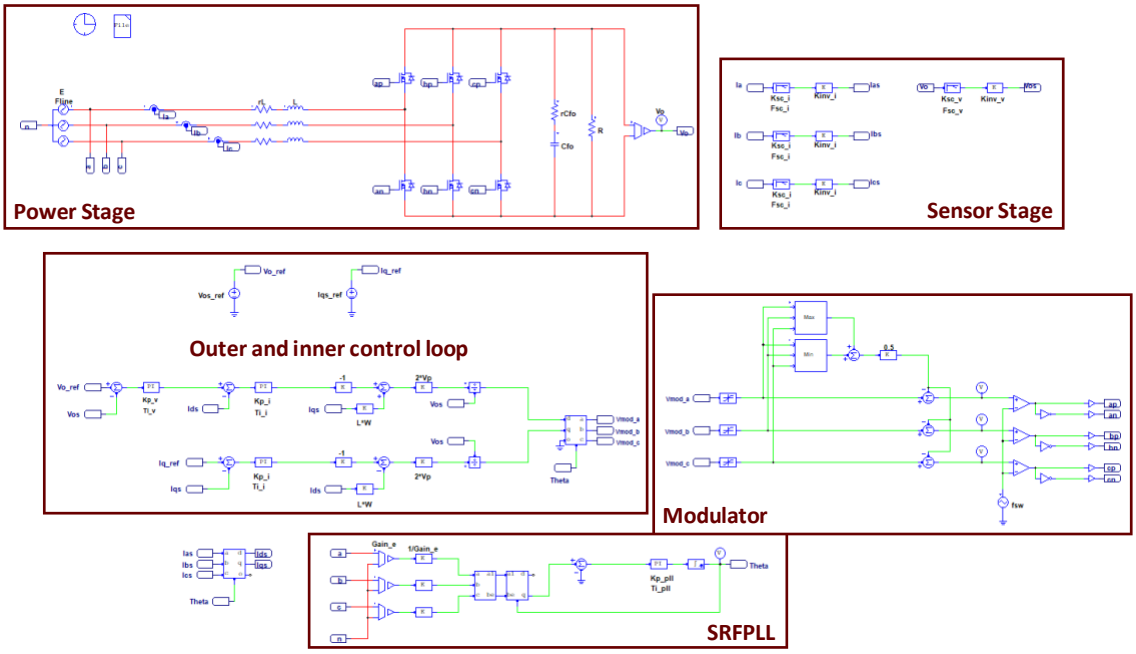

Figure 21: PSIM exported system

In this picture, all the different functional blocks have been highlighted. Ensure to configure the simulation time control as follows. Figure 22.

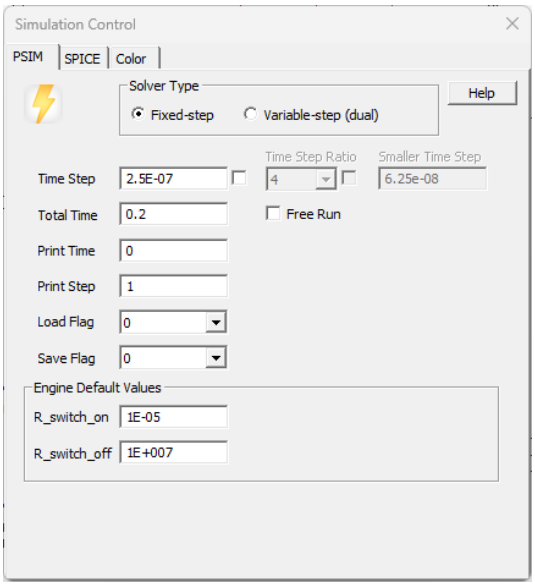

Figure 22: Clock configuration in PSIM

The result of the simulation is shown in Figure 23:

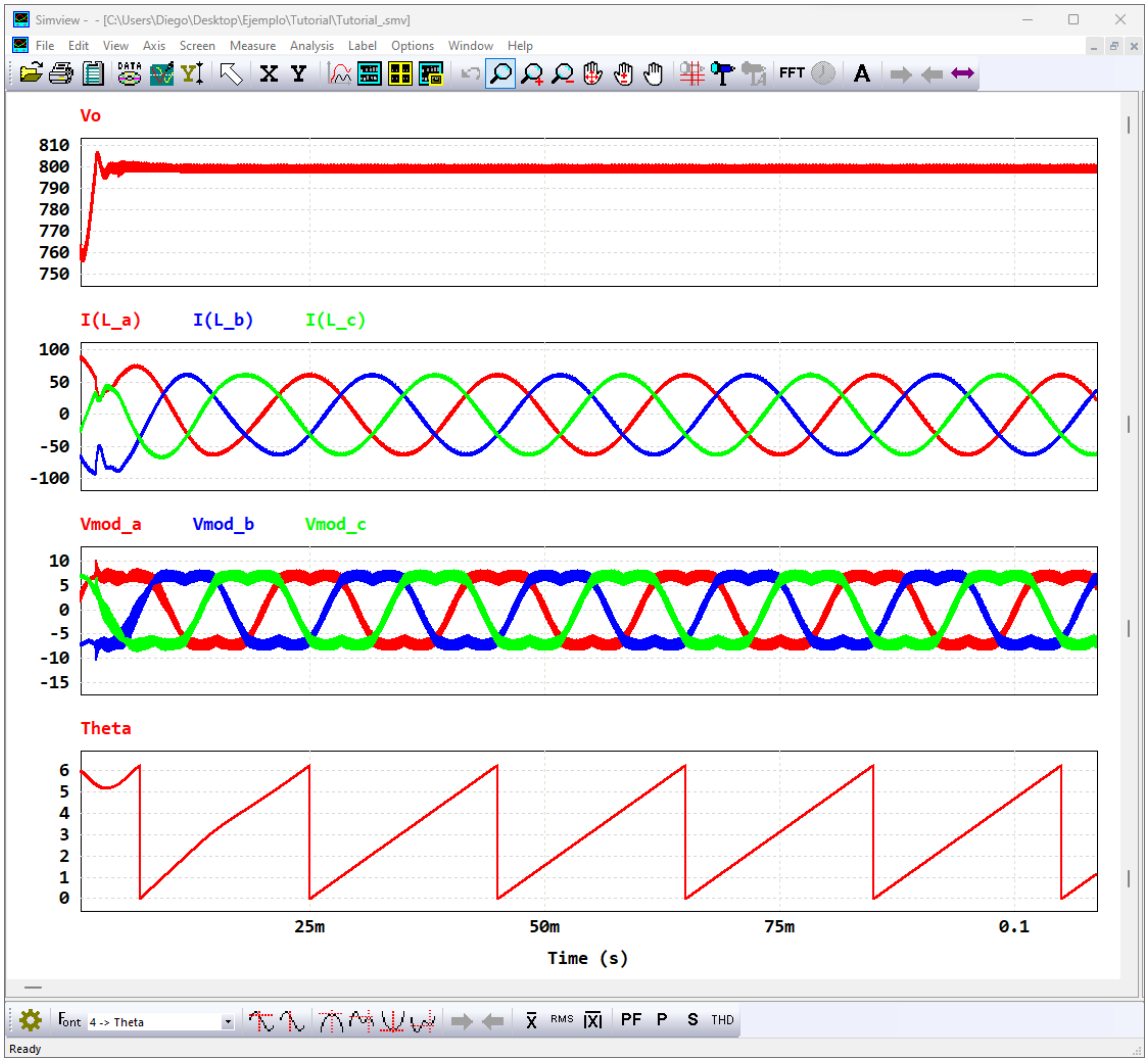

Figure 23: Result of PSIM simulation

As it can be seen, the output voltage is 800V, it is exactly what have been specified in SmartCtrl.

If the dynamic response of the system is to be analyzed, it would be necessary to introduce a step, for example, in the input voltage. See Figure 24.

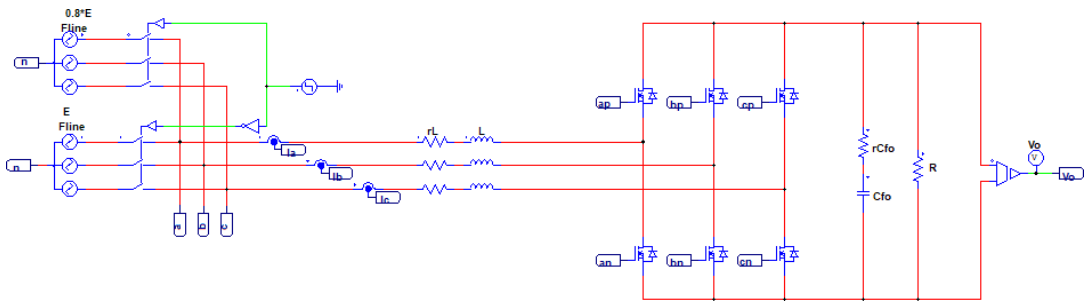

Figure 24: Input voltage step in PSIM

The result of this new system can be seen in Figure 25.

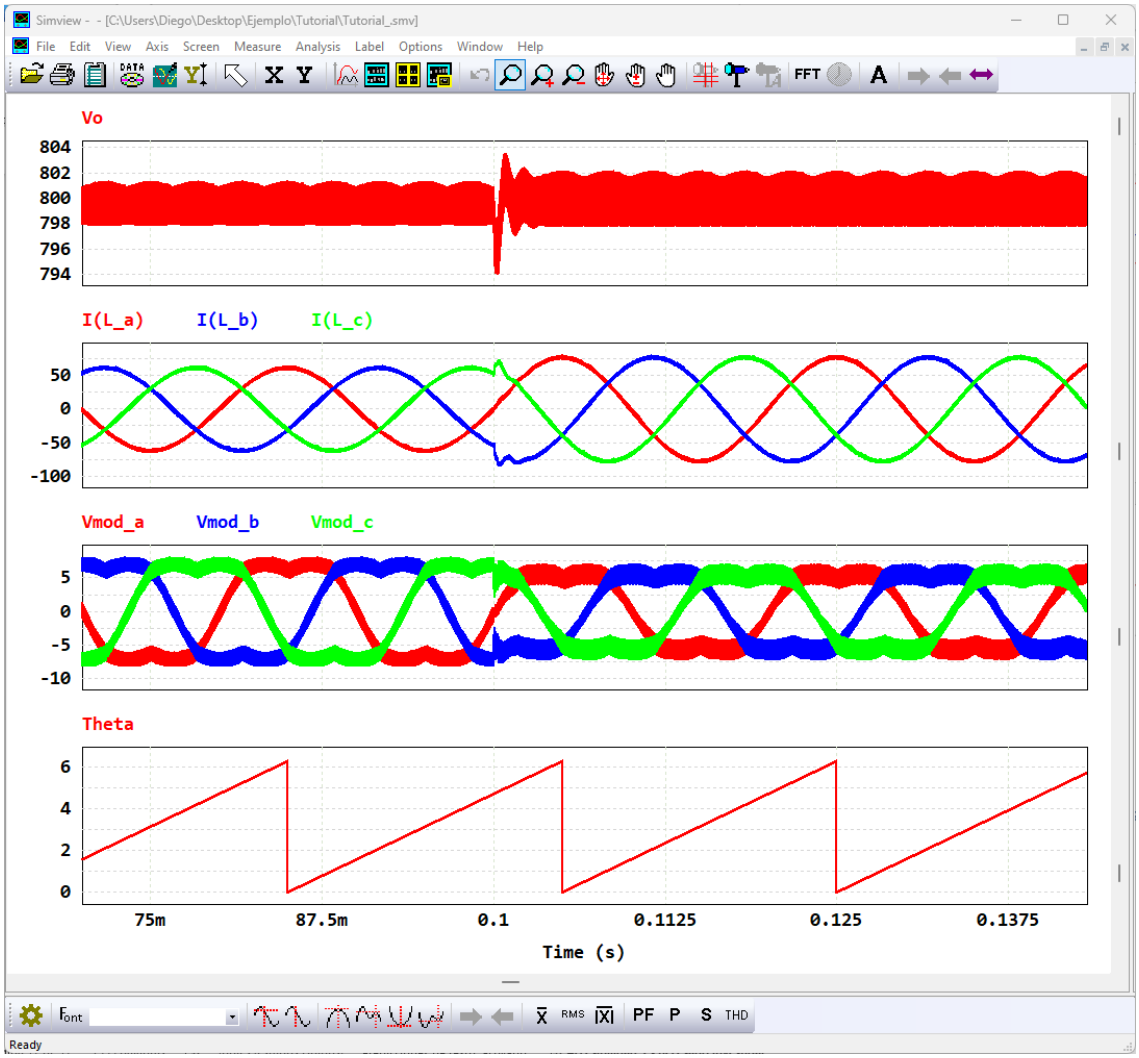

Figure 25: New PSIM simulation where dynamic response can be seen