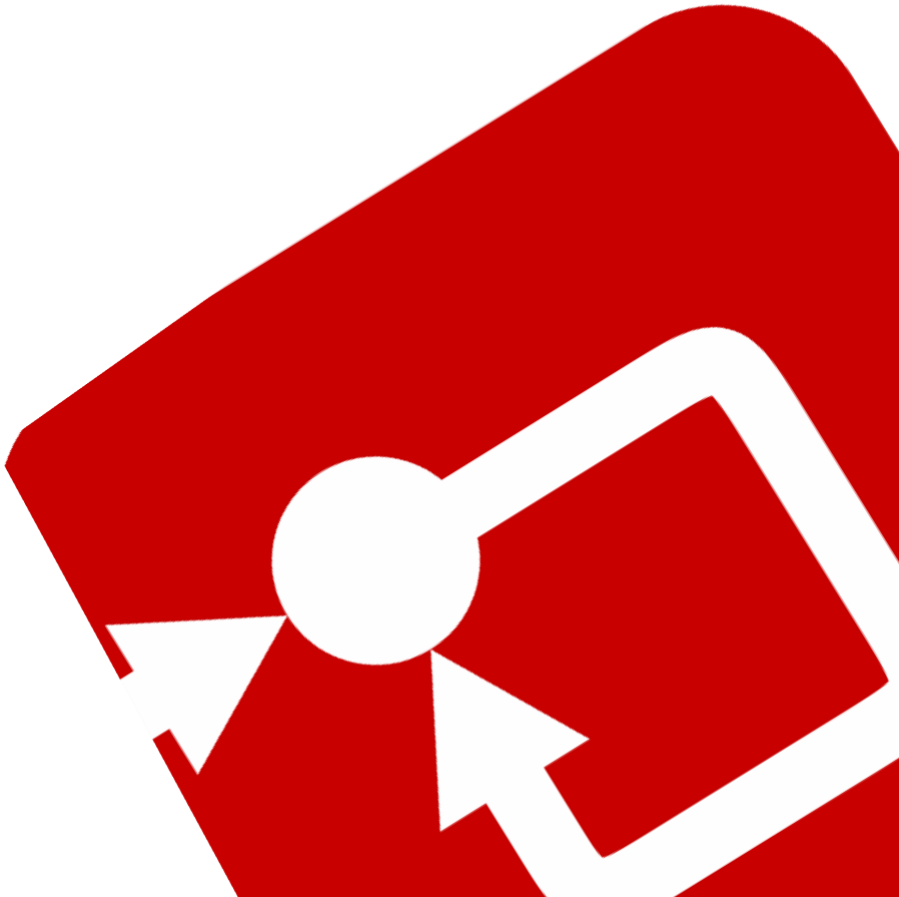
smart ctrl

control design for power electronics

# Digital Control Loop Design: discretization

Tutorial –December 2025-



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Power Smart Control SL

# General Index



# Figure Index

# 1. Introduction

SmartCtrl is a controller design software specifically designed for power electronics application. This tutorial is intended to guide you, step by step, to design the digital control loop of a buck converter and simulate it with PSIM.

SmartCtrl provides three ways of dealing with digital controls:

a) Design the whole system as an analog one and discretize the compensator
b) Design an analog plant with a digital compensator.
c) Design a whole discrete system.

In this tutorial, it has been option a) the one covered.

# 2. Digital Control Design

The design procedure begins with the design of the analog control loop. After that, the analog regulator is discretized taking into account several specific parameters of the digital design.

1. Select the power converter topology and the type of control. In this case, it is a voltage mode controlled Buck converter. To start the design click in DC-DC converter – Single loop design mode control or ACMC, see Figure 1.

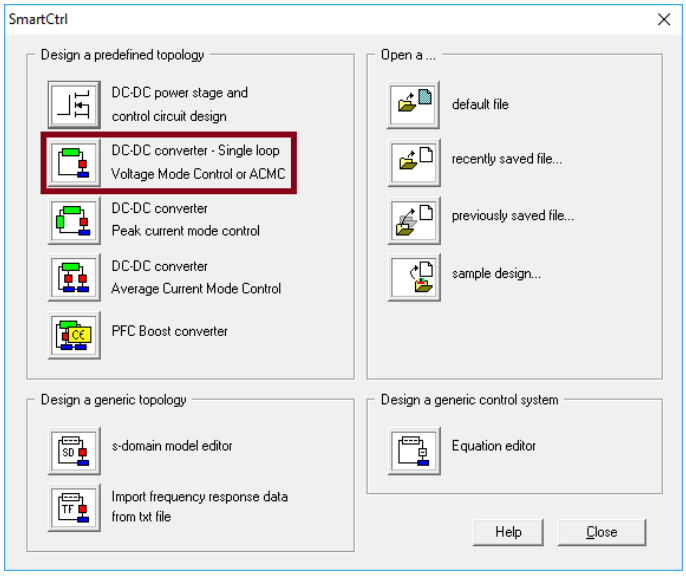


Figure 1: SmartCtrl start menu

2. Select a buck voltage mode controlled plant (See Figure 2) and introduce the plant parameters shown in Figure 3. Notice that Digital checkbox has been left unmarked.

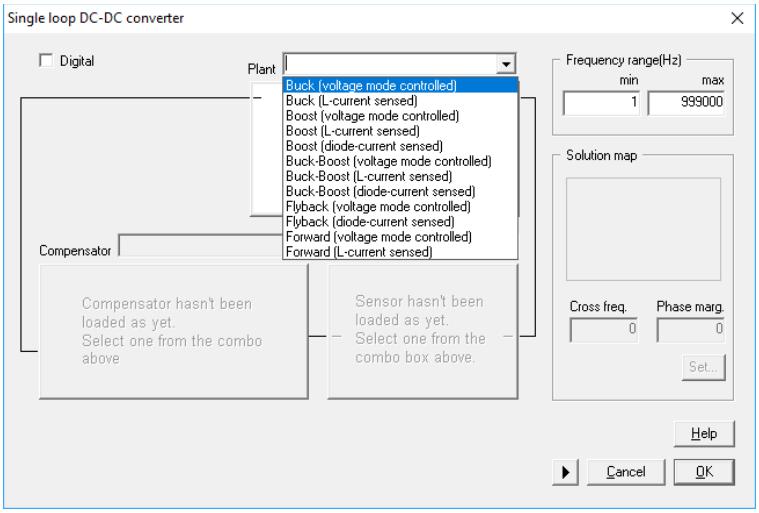


Figure 2: Select the plant topology

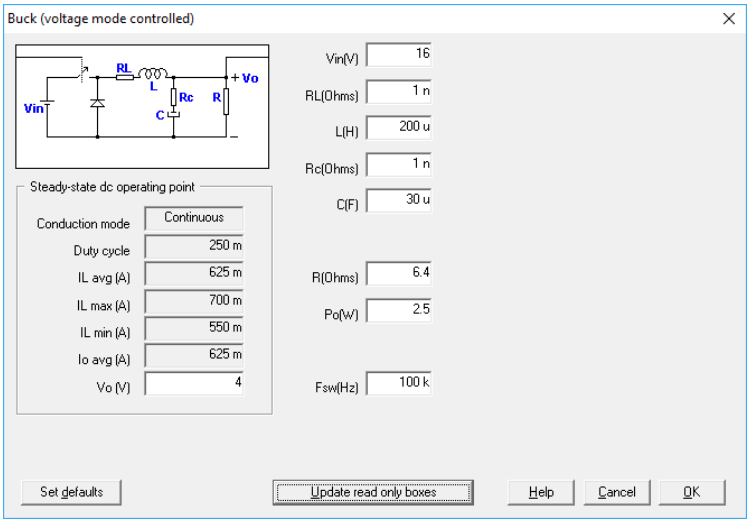


Figure 3: parametrize the plant

3. Sensor parameters are defined in the corresponding dialog box (Figure 4). When a digital control loop is designed, only "Voltage Divider" sensor can be selected.

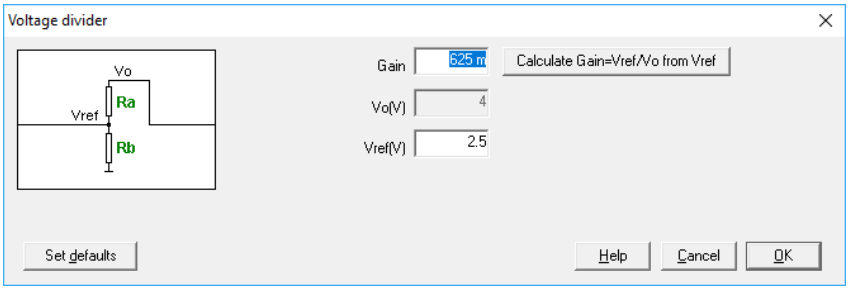


Figure 4: Voltage divider sensor parameters

After selecting the Type 3 compensator, a new dialog box appears as it can be seen in Figure 5.

4. The modulator parameters are defined in this dialog box. In this tutorial, a trailing edge unity gain modulator has been selected, so the parameters have been fixed as: Vp=1, Vv=0, tr=10us.

5. It time to select the requirements of the control loop in terms of cross over frequency of the open loop transfer function (fc) and the phase margin (PM).

In SmartCtrl the user can select graphically a solution inside the stable design space, called Solution Map (Figure 5), whose white area defines the pairs of (fc, PM) that result in a stable design. In this tutorial, the selected cross over frequency is fc=4.5 kHz, and the selected phase margin is PM=50º. See Figure 6.

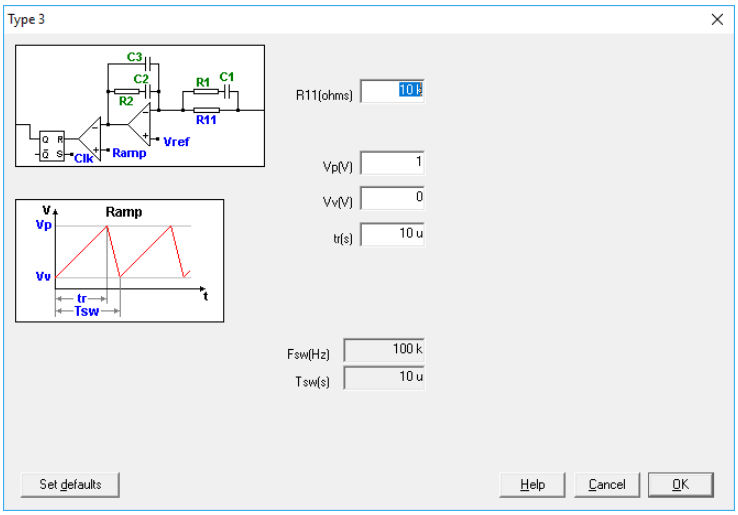


Figure 5: Type 3 compensator parametrization

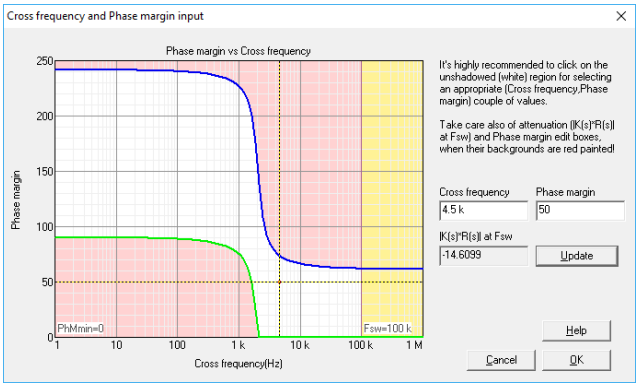


Figure 6: Solution map fully defined

6. The analog loop is already designed as it can be seen in Figure 7. Click OK to finish the wizard. SmartCtrl will launch the analysis view where Bode and Nyquist plots, transient plot and steady state waveforms can be used to analyze the stability and dynamic response of the system designed. See Figure 8.

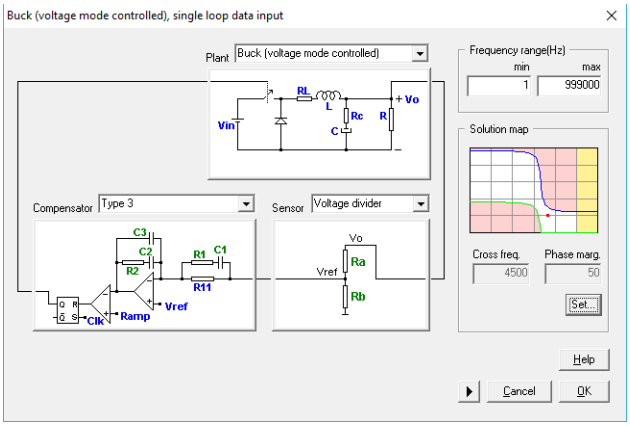


Figure 7: Control loop fully defined

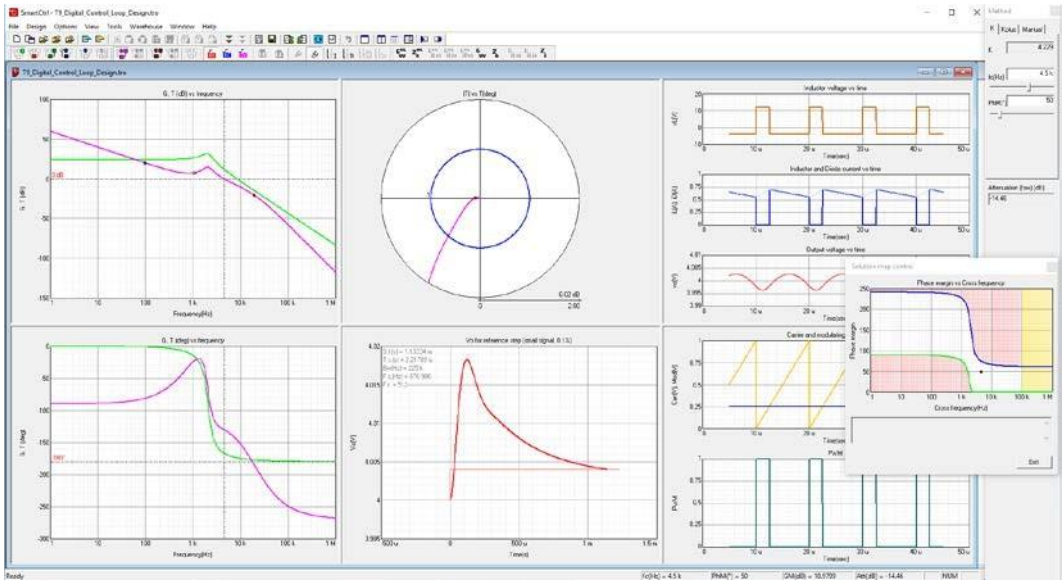

Figure 8: SmartCtrl analysis view

# 3. Digital Control Analysis in SmartCtrl

Once the analog loop has been completed, SmartCtrl provides a tool to discretize the analog compensator and generate an analog one. To do this, it is used the bilinear transformation taking into account some additional aspects.

To access this capability just click in the icon highlighted in Figure 9. Notice it can only be used after completing all the design steps of an analog regulator.

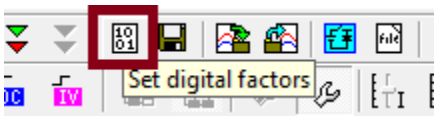


Figure 9: Discretization capability

The digital settings box appears, asking for the specific digital parameters: sampling frequency, bits number and accumulated delay. The sampling frequency is often the same as the switching frequency, but it can be different.

Notice that the sampling frequency must be a multiple or submultiple of the switching frequency. See Figure 10.

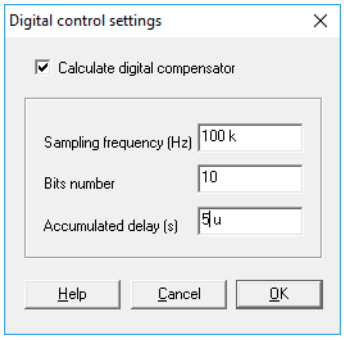


Figure 10: Discretization settings

The number of bits is related with the rounding of coefficients of digital compensator. Depending on each case, a different number of bits can be enough to obtain a digital regulator similar to analog regulator, as it will be detailed later. Note that bits number is referred only to the regulator coefficients calculation.

As shown in Figure 11, Accumulated delay is the time between the sampling instant and the PWM pulse effective updating, which is the falling edge in the trailing edge pulse width modulator. Therefore, accumulated delay includes analog to digital conversion delay, calculations delay and modulator delay being the sum of all delays in the digital control loop.

When digital settings have been completed, the check box "Calculate digital compensator" must be checked. Then the digital regulator is calculated and it appears some icons which allow to represent digital transfer functions, see Figure 12.

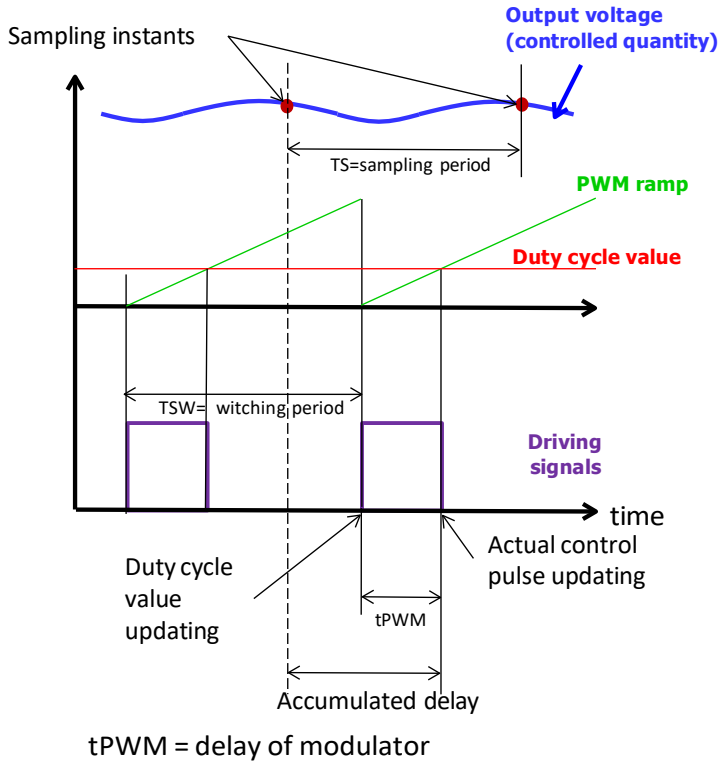


Figure 11: Accumulated delay definition

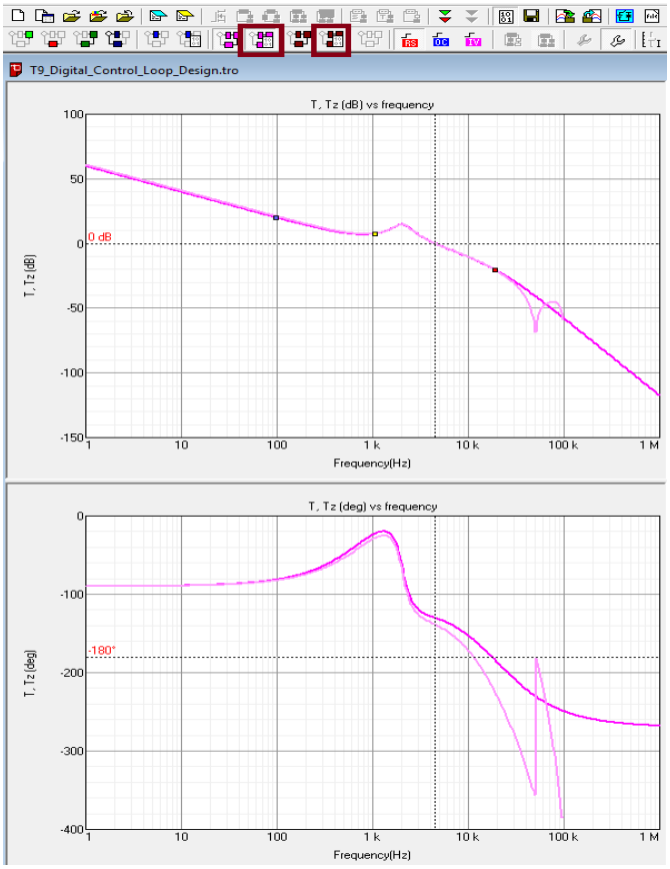


Figure 12: Digital transfer functions

As it can be seen in Figure 12, The analog (dark pink trace) and the digital compensator (clear pink trace) can be plot together making it possible to compare them. This discretization function is exact only at cross frequency (as prewarping has been applied to the function), in any other point, it will exist a small deviation.

In Figure 12 it can also be seen in the bode plots the alteration at high frequencies that generate this discretizing method.

Digital factors sweep utility allows to change dynamically any digital settings and see graphically how it affect the results. See Figure 13.

In the example of Figure 14 the number of bits has been changed, it can be seen that the digital open loop and analog open loop transfer functions are different in magnitude (low frequencies) and in phase (medium and high frequencies).

It means that the selected number of bits is not enough to represent the coefficients of the digital regulator.

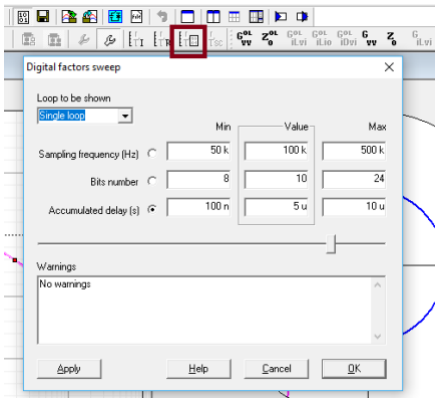


Figure 13: Digital parameter sweep

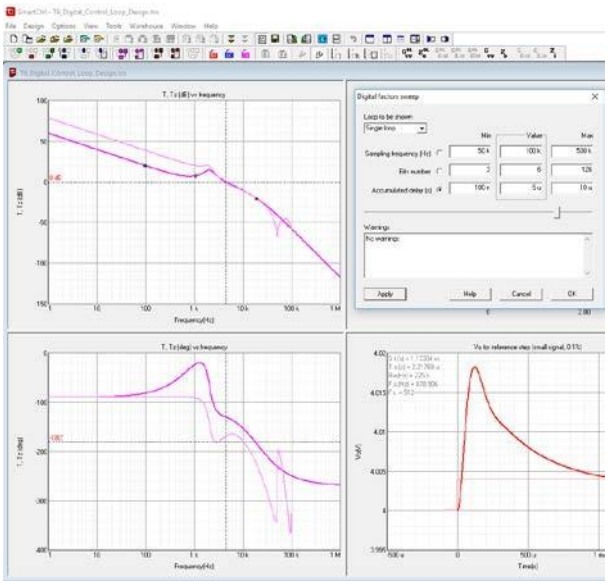

Figure 14: Effect of changing bit number

# 4. Exportation to Psim and simulation

Once the digital regulator has been calculated, the entire design can be exported to PSIM, and then simulated and checked.

To export the whole design to Psim, just click on the icon shown in Figure 15 and configure the exportations as it has been done in Figure 16.

SmartCtrl provides several exporting options. It can be exported both: the original analog compensator or the discretized one. To export the discrete one just select "z domain coefficient" in Figure 16.

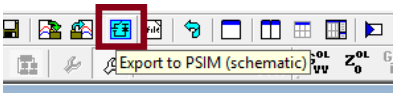


Figure 15: SmartCtrl export to Psim button

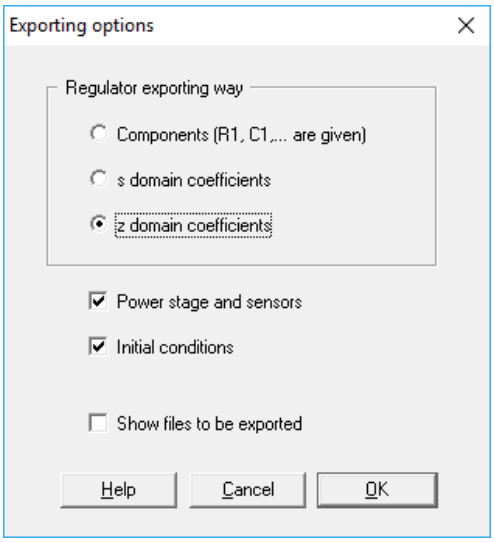


Figure 16: SmartCtrl exporting to Psim options

The design is exported to a PSIM schematic, including a file where a **l** converter and contro **l**er parameters are contained. The system that SmartCtrl creates in Psim is shown in Figure 17.

In the PSIM schematic the power stage and the digital control stage appear. A trailing edge pulse width modulator is included. In this particular implementation, the modulator introduces a time delay equal to D/fsw, there D is duty cycle corresponding to the steady state operating point, and fsw is the switching frequency.

A "time delay" block is added to take into account the additional time delays in the control loop, in such a way that the total time delay in control loop is equal to the value of "accumulated delay" introduced by the user. The value of this "time delay" is automatica **l**y calculated by SmartCtrl.

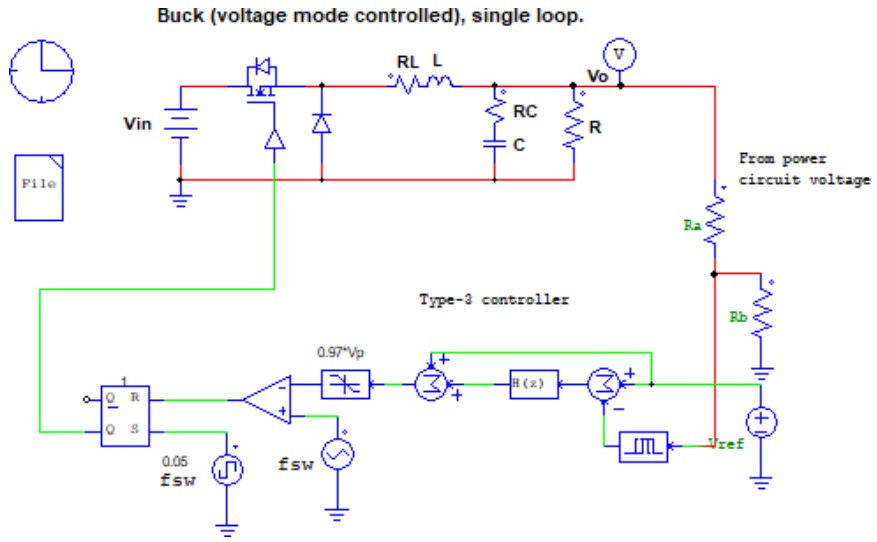


Figure 17: Psim schematics

A time domain simulation can be launched to check that the steady state operating point is achieved. The result of this simulation is shown in Figure 18, it can be seen how the output voltage is equal to 4V, the one that was specified in SmartCtrl.

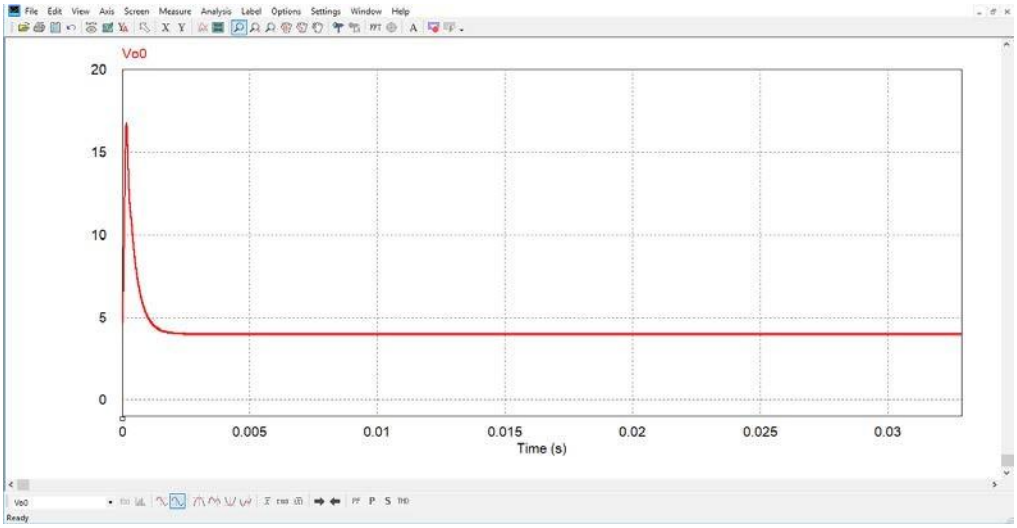


Figure 18: Result of time domain simulation

This time domain simulation is quite interesting to check if the converter works properly. However, a more in depth simulation can be done in which the open loop gain would be the magnitude to measure. This open loop gain can be compared with the one provided by SmartCtrl to see if the final converter matches the dynamic response specification.

To measure this open loop gain, it is necessary to modify the Psim schematic to introduce an AC sweep simulation. See Figure 19.

Please note that open loop gain should be measured with the converter working in closed loop, in other case, the compensator will saturate. To do this measurements, Psim provides a special AC probe with two leads.

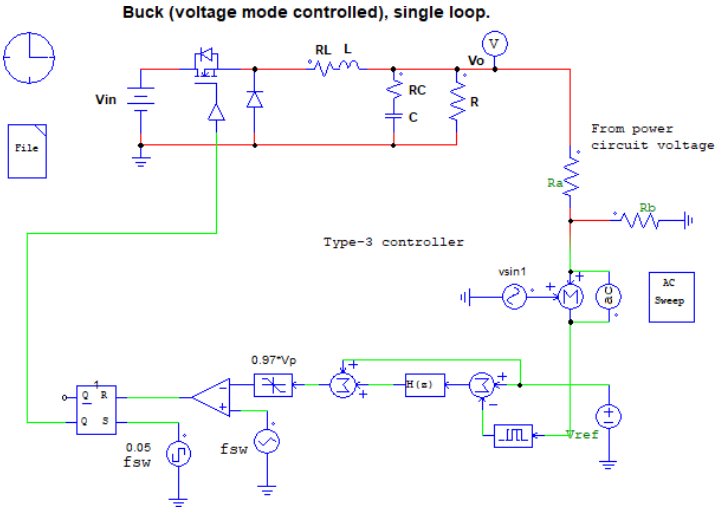


Figure 19: Modified Psim schematic for AC sweep

Figure 20 provides the result of the Psim AC sweep simulation.

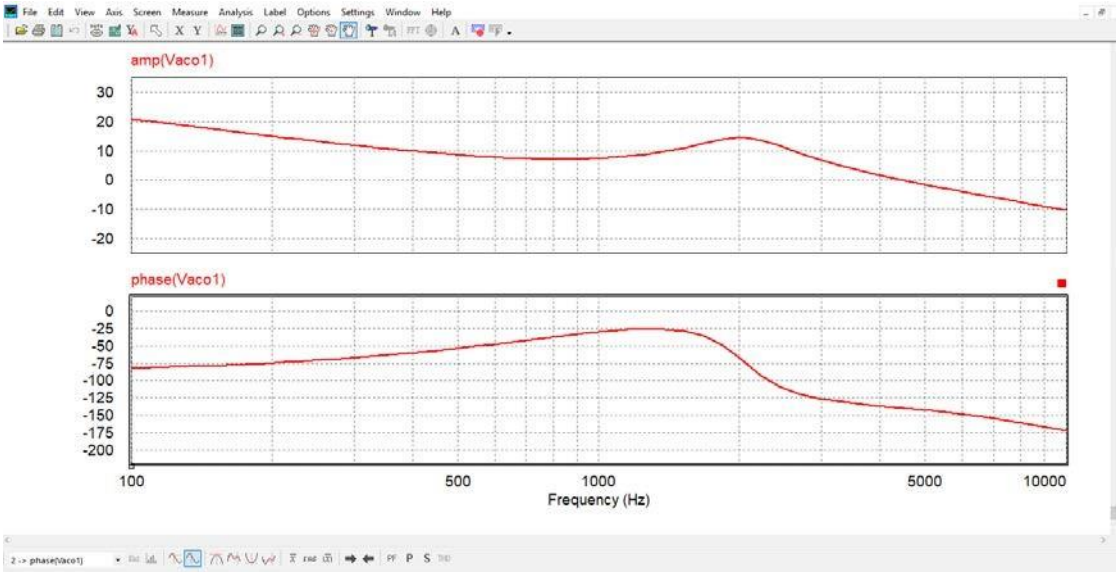


Figure 20: Psim open loop measured gain

Save the simulation data with **File** -> **save as** -> Psim_AC_data_points**.txt**

# 5. SmartCtrl comparison

In order to compare the obtained AC response and the theoretical calculated with SmartCtrl, this Psim transfer function can be loaded to SmartCtrl design.

To do this, in this use the former SmartCtrl design and click in **File** –> **Import** and select the path of the Psim_AC_data_points.txt file. See Figure 21.

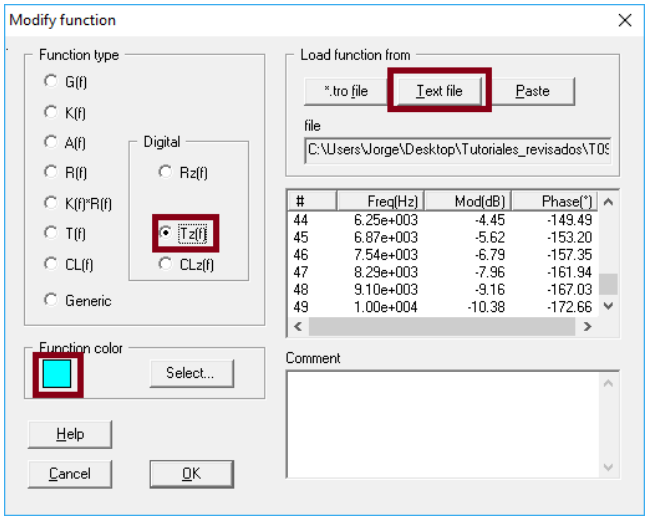


Figure 21: SmartCtrl importing wizard

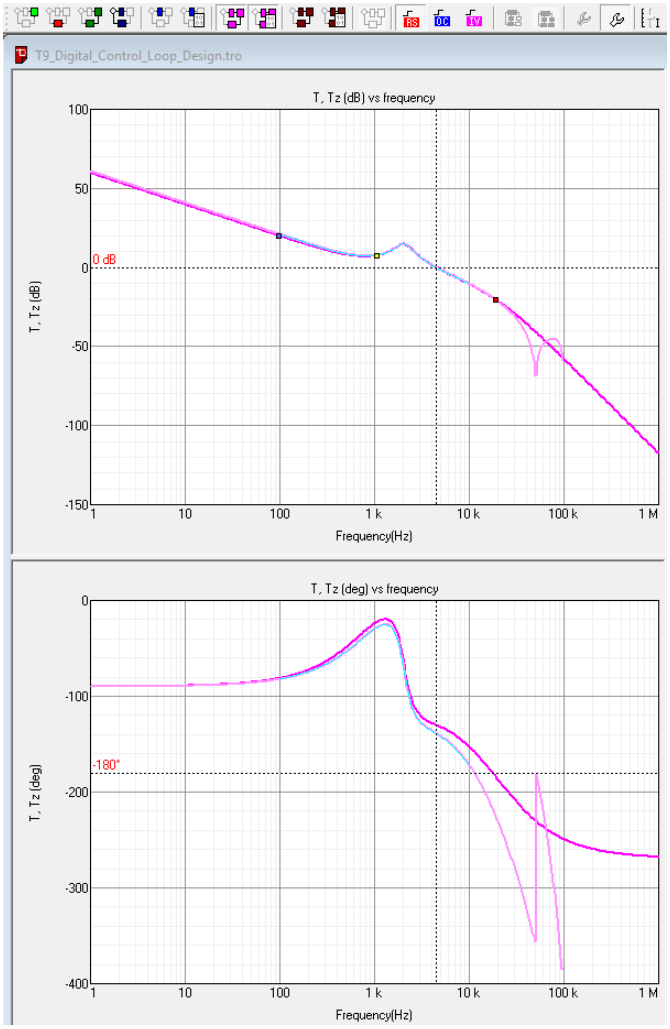


Figure 22: Open loop gain comparison (analog / digital / Psim AC sweep)

Figure 22 shows the comparison in SmartCtrl of the three open loop gains (OLG):

a) Analog OLG -> dark pink trace
b) Discretized OLG -> light pink trace
c) Psim measured OLG -> light blue trace

AS it can be seen, at cross frequency all the three OLG are exactly the same and there is quite a small deviation up to half the switching frequency.

It can be noticed how the design done in SmartCtrl is quite accurate and how simple is it to design a discretized controller.