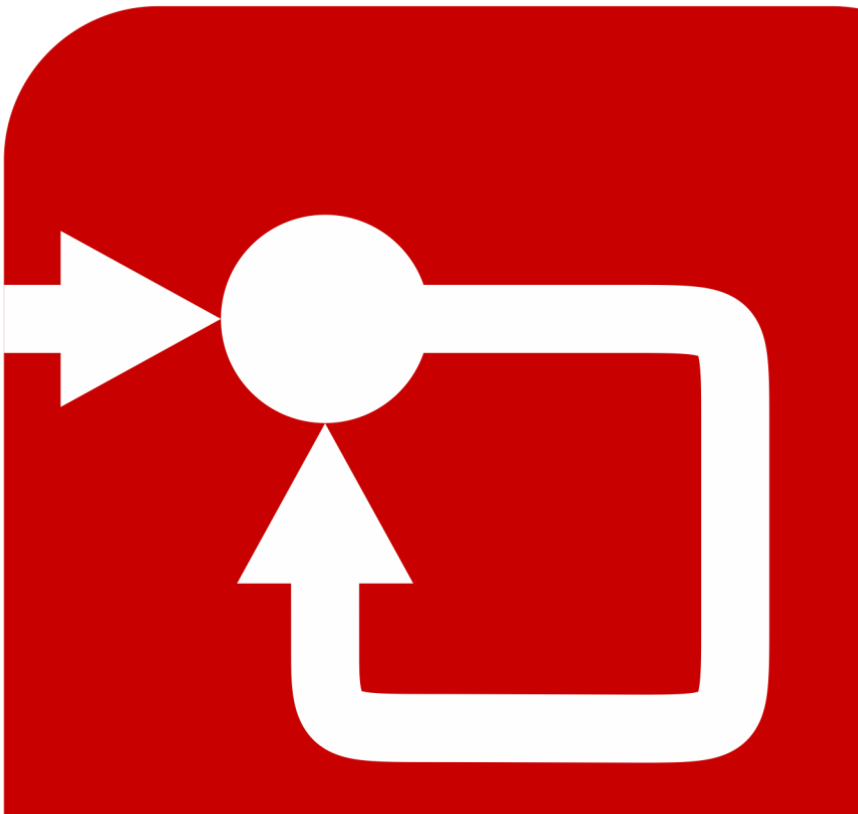
smart ctrl

control design for power electronics

Digital Control Double Loop Design

Tutorial –December 2025-



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Power Smart Control SL

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1. Introduction

SmartCtrl is a design software specifically designed for power electronics application. This tutorial is intended to guide you, step by step, to design the digital control loop of a buck converter and simulate it with PSIM. This document is the second part of the document “Discrete Digital Control Loop Design”.

In this document, a double loop control stage has been designed. To do so, part of the design already done in the tutorial “Discrete Digital Control Loop Design” has been used.

2. Inner loop design

Open SmartCtrl and choose a DC-DC converter averaged current mode control. See Figure 1 and select a buck LCS_VMC topology.

Configure the inner loop with the following parameters:

a) Plant: select a buck LCS_VMC topology. See Figure 2.
b) Sensor: select a Hall effect sensor. See Figure 3.
c) Compensator: select a Type 2. See Figure 4.
d) Solution map: select fc=2kHz and PM=40 degrees. See Figure 5.

At this point, the inner control loop is fully defined.

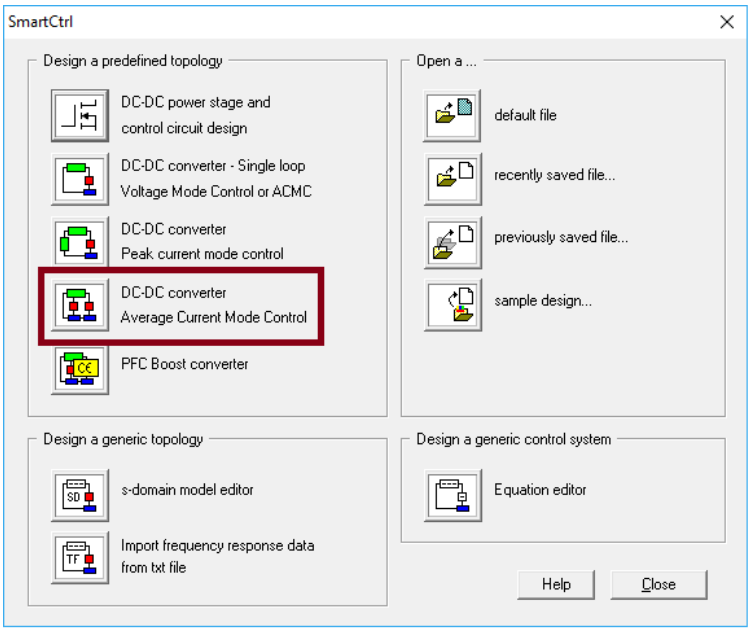

Figure 1: SmartCtrl initial window

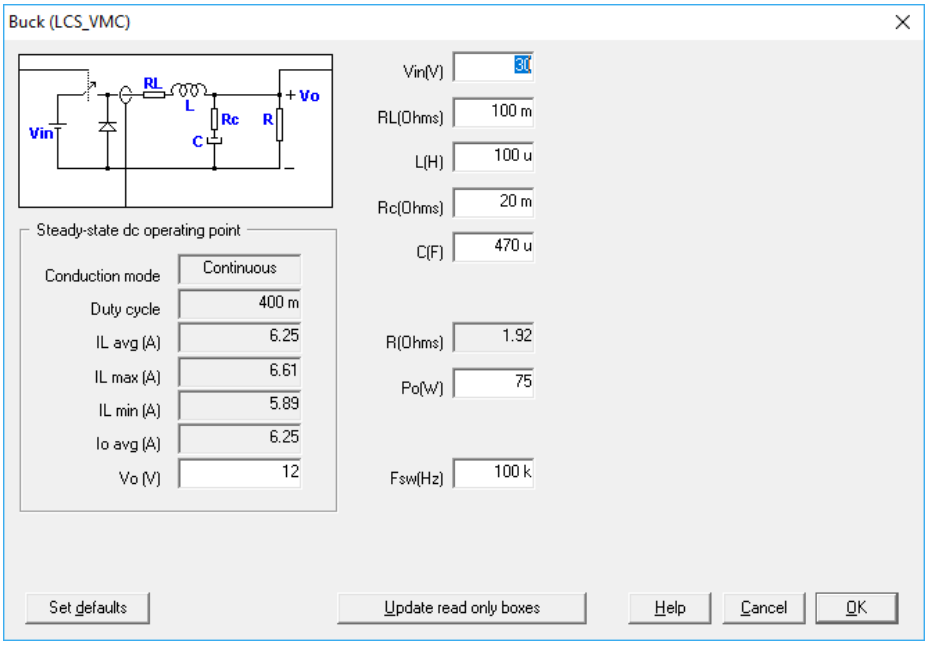

Figure 2: plant parameters

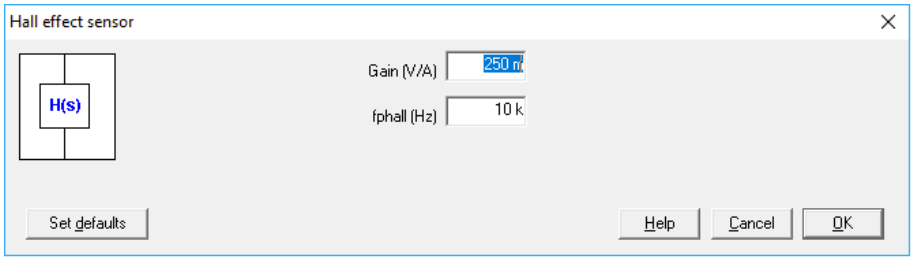

Figure 3: Sensor parameters

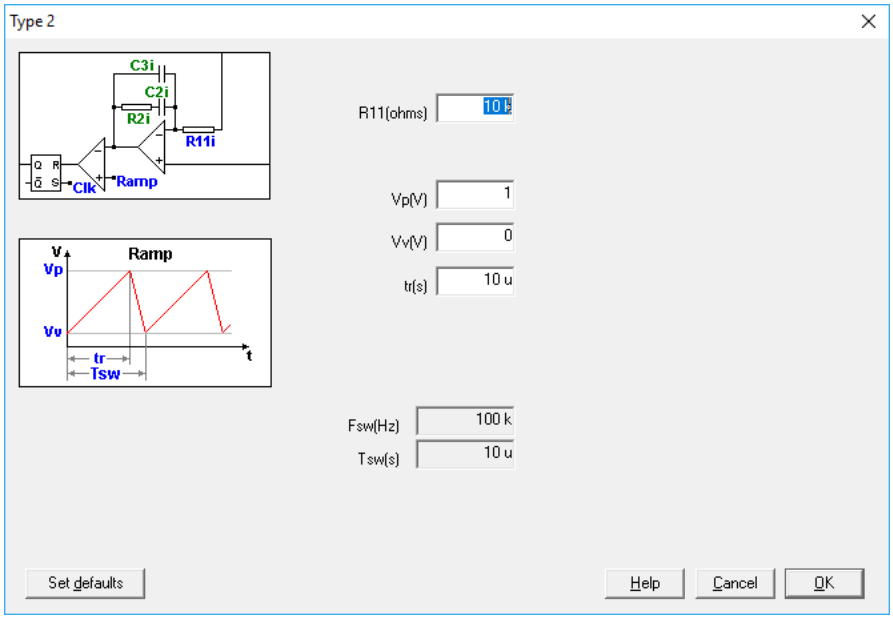

Figure 4: compensator parameters

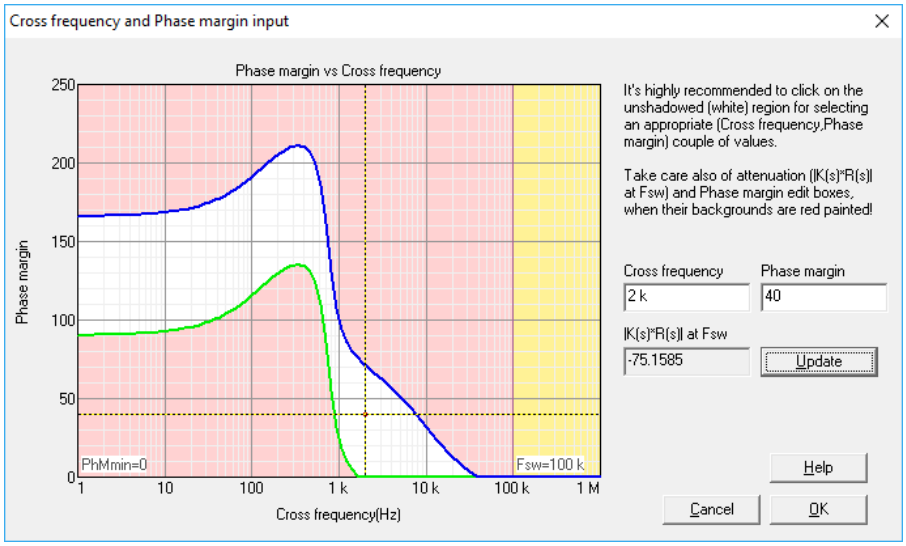

Figure 5: solution map point

It is used a Hall effect sensor as antialiasing filter since the quantity that is sampled (current trough the inductor) has a high ripple, when sampling under the Nyquist frequency (typically the switching frequency), antialiasing filter should be used, or an adequate synchronization with the ripple waveform must be ensured.

In this case, the pole frequency of the Hall effect sensor is 10 kHz as it can be seen in Figure 3.

After selecting plant, sensor and regulator (modulator) parameters, the cross over frequency fc and the phase margin PM desired for the inner control loop are selected using the graphical aid of the Solution Map

3. Outer loop design

This design procedure is quite similar to the one done in tutorial “Discrete Digital Control Loop Design”, so the details has not been covered in full depth.

Configure the outer loop with the following parameters:

a) Sensor: select a voltage divider sensor. See Figure 6.
b) Compensator: select a PI. See Figure 7Figure 4.
c) Solution map: select fc=1kHz and PM=100 degrees. See Figure 8.

At this point, the outer control loop is fully defined.

Note that the outer loop compensator does not include any information regarding the modulator as the modulator is included in the inner loop.

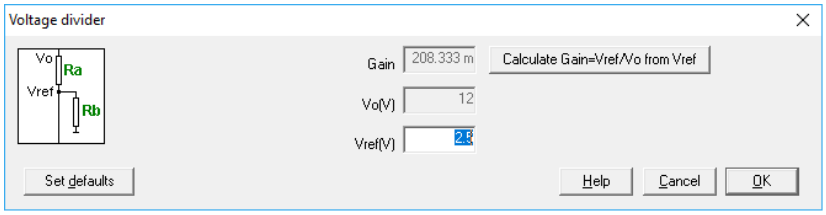

Figure 6: outer loop sensor

Figure 7: outer loop compensator

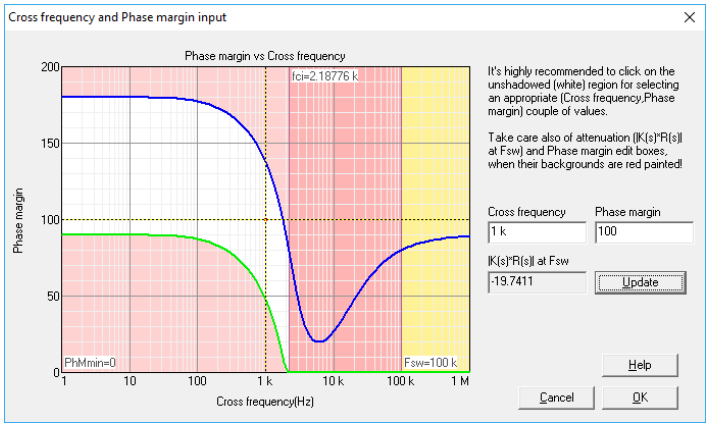

Figure 8: outer loop solution map

4. Discretize the compensators

At this point, analog control loop has been calculated. Then, by clicking in the "Digital settings" icon, the dialog box asking for digital loop parameters (sampling frequency, bits number and accumulated delay) appears. See Figure 9 and Figure 10.

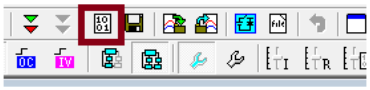

Figure 9: Discretise tool in SmartCtrl

Note that different parameters can be used for the inner loop and the outer loop. In this case, both loops have the same sampling frequency (equal to the switching frequency), the same number of bits (16) and the same accumulated delay. By checking the check-box "Calculate digital compensator" and clicking in the "OK" button, both inner and outer digital regulators are calculated.

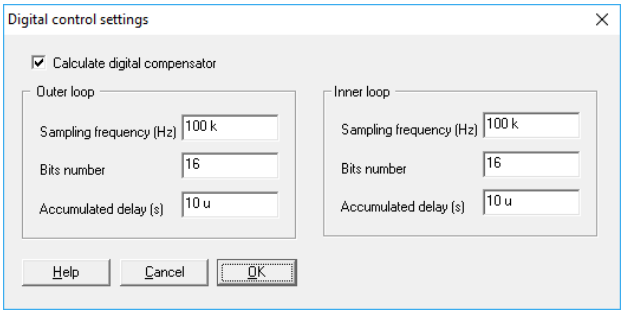

Figure 10: discretizing parameters for inner and outer loop

The button "export to PSIM (schematic)" allows exporting the entire design to PSIM (see the document "Digital control loop design" for more detail. See Figure 11 and Figure 12. The exported schematic is shown in Figure 13.

Figure 11: SmartCtrl export to Psim button

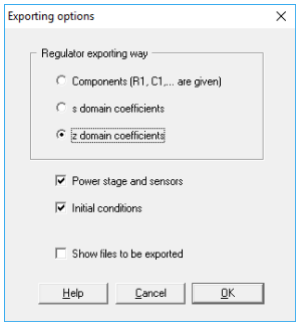

Figure 12: exporting options

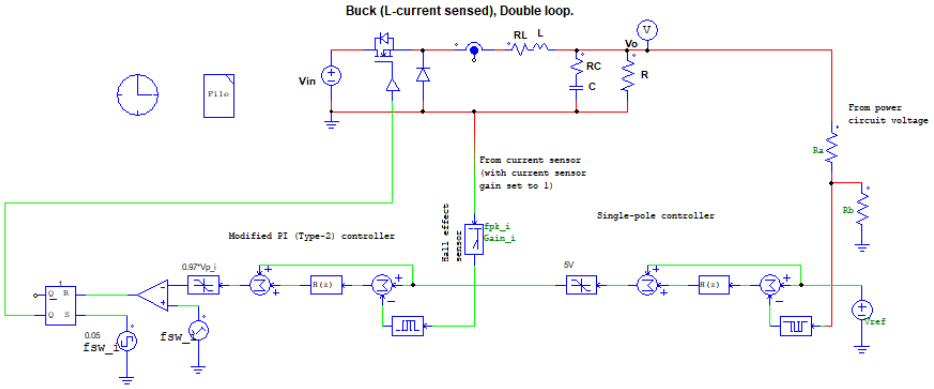

Figure 13: Psim exported schematic

The result of the time domain simulation can be seen in Figure 14. It can be seen how the output voltage is exactly 14V which is the value specified in SmartCtrl.

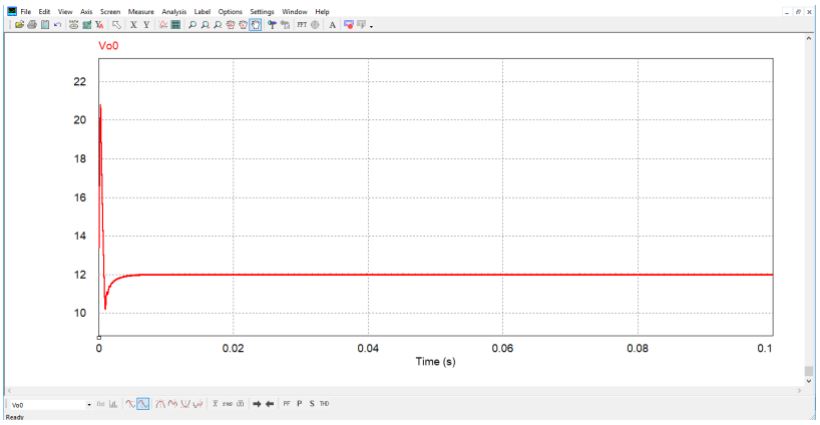

Figure 14: Time domain simulation result

In order to simulate the digital open loop transfer function corresponding to the inner loop, more additional elements are added to the schematic. First, the outer loop is disabled, and then an adder, a sinusoidal voltage source and an AC probe are added to perform the AC sweep and measure the current loop. See Figure 15 and Figure 16.

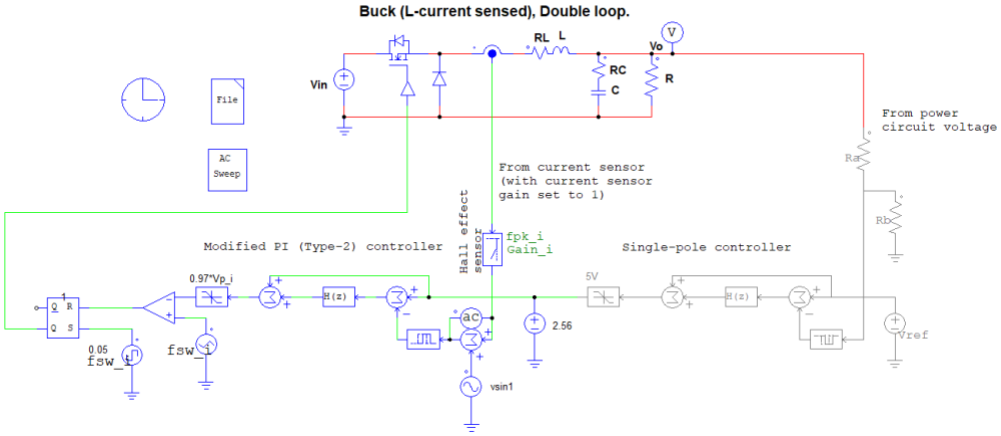

Figure 15: Inner open loop gain measurement

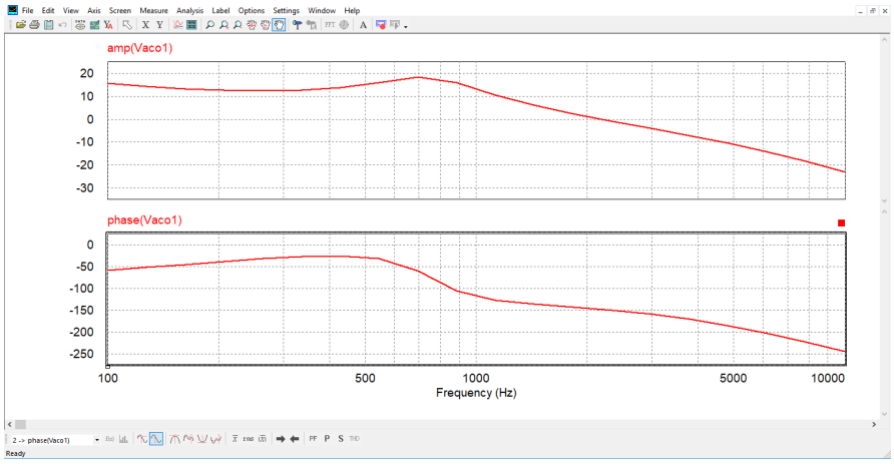

Figure 16: Inner open loop gain measurement result

Save the data with **File** -> **save as** -> Psim_inner_loop_Ac_sweep**.txt**

In the SmartCtrl project select the inner loop (Figure 17) and click in **File** -> **Import** (see Figure 18).

Figure 17: selecting the inner loop in SmartCtrl

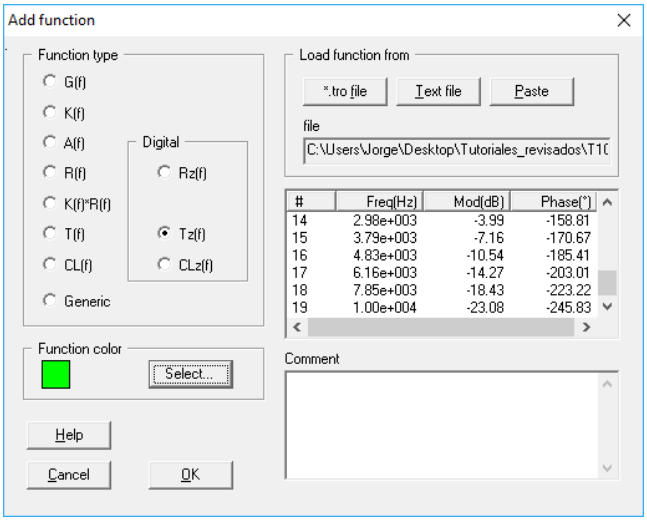

Figure 18: importing data wizard

In Figure 19 it has been compared open loop gain of inner loop:

a) Analog system -> dark pink trace
b) Discretized system -> light pink trace
c) Psim measured -> green trace

It can be seen how all of them are equal at cross frequency and quite similar until half of switching frequency.

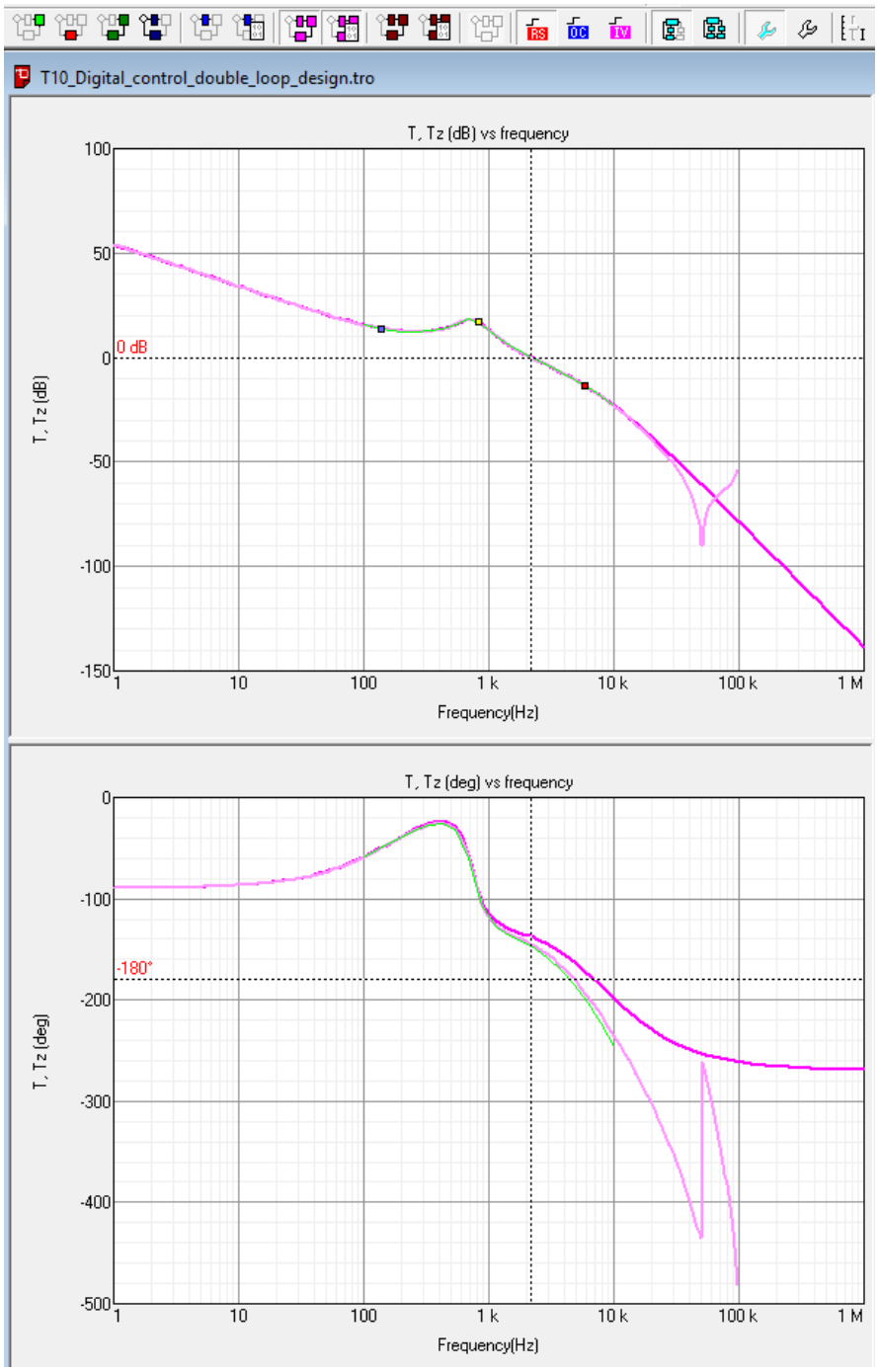

Figure 19: SmartCtrl open loop gain of inner loop comparison