

True-Device Real-Time Emulation SiC FET / Si MOSFET Cascode Buck Converter

Cascode Configuration

JFET Parameters

- Transconductance [A/V]: 4.00E+01
- Threshold Voltage [V]: -2.20E+01
- Drain-source on-resistance [ohm]: 8.60E-03
- Internal Gate resistance [ohm]: 6.00E+00
- Drain-source Capacitance [pF]: 1.00E+01
- Gate-drain Capacitance [pF]: 7.55E+02
- Gate-source Capacitance [pF]: 1.00E+03

MOSFET Parameters

- Transconductance [A/V]: 1.00E+02
- Threshold Voltage [V]: 5.50E+00
- Drain-source on-resistance [ohm]: 7.50E-03
- Internal Gate resistance [ohm]: 1.00E-03
- Drain-source Capacitance [pF]: 3.00E+03
- Gate-drain Capacitance [pF]: 4.15E+02
- Gate-source Capacitance [pF]: 8.51E+03

MOSFET Diode Parameters

- Forward Diode Voltage [V]: 2.40E+00
- Forward Diode resistance [ohm]: 1.00E-03

The implement cascode model includes the effect of parasitic capacities in addition to the equivalent behavior of its parts (MOSFET and JFET) in each of its operating modes.

Non Ideal Cascode Model

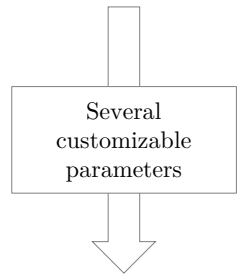
Power Stage Options: DC Source, Output Filter and Load, Cascode Parameters, Half Bridge Layout, Cascode Thermal Model, Cascode Snubber

Control Stage Options: PWM configuration, Driver control

FPGA Engine: Start SIM, Stop SIM, FPGA Oscilloscope

Benefits of high precision models of switching devices running in an acceleration hardware device

- **Switching power losses** emulation considering true device model and lay-out parasitic elements.
- Simulation of **junction temperature** evolution.
- Simulation of **conducted differential and common mode EMI** components.
- **Instant protections design** (overcurrent and short-circuit profiles, di/dt).
- **Cooling system design.**
- **EMI filters & lay-out design.**
- **Snubber design.**
- **Failure sequences** (snubber failure, device failure, gate driver failure, etc).
- **Faster than software simulator.**

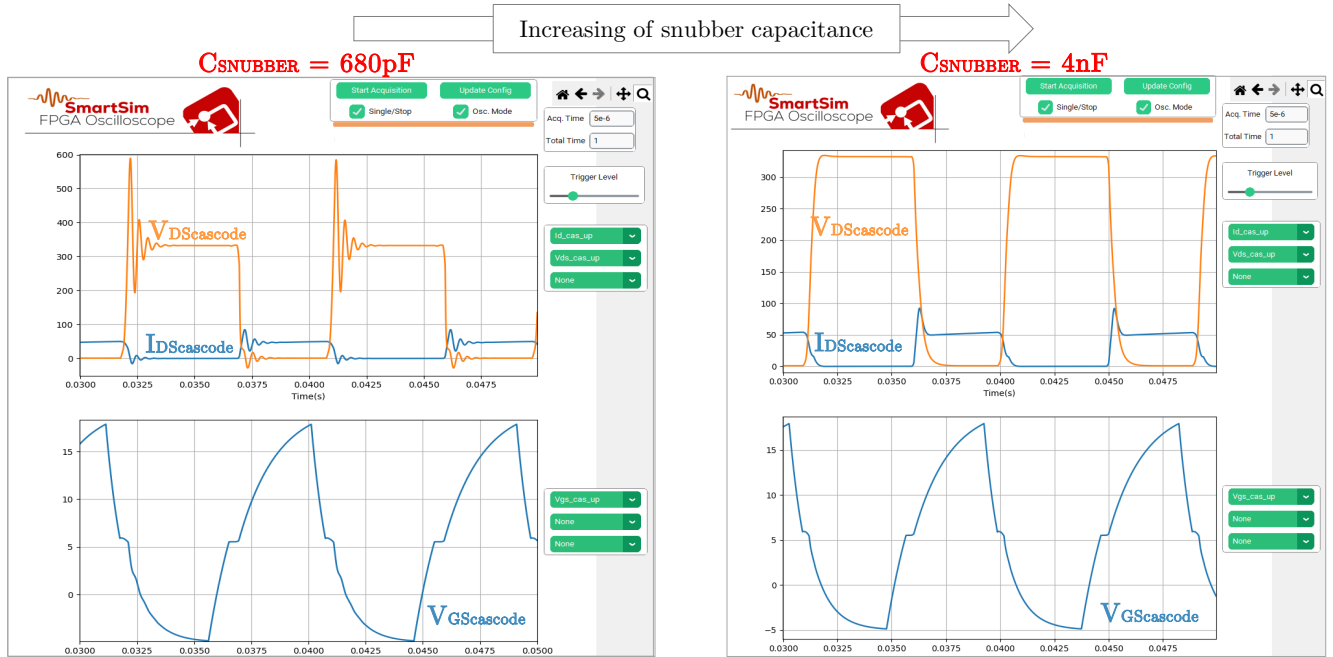


- **DC Power Input** Configuration
- **Output Filter** Configuration
- **Half Bridge Layout** Configuration
- **Cascode Parallel Snubber** Configuration
- **Foster Model** Configuration
- **Buck Converter PWM** Configuration
- **Driver** Configuration



Usage example: Snubber design

Non ideal switch models allow the designer to customize parameters such as snubbers. In order to optimize the effect that this parameter produces on the converter in order to obtain the required response.

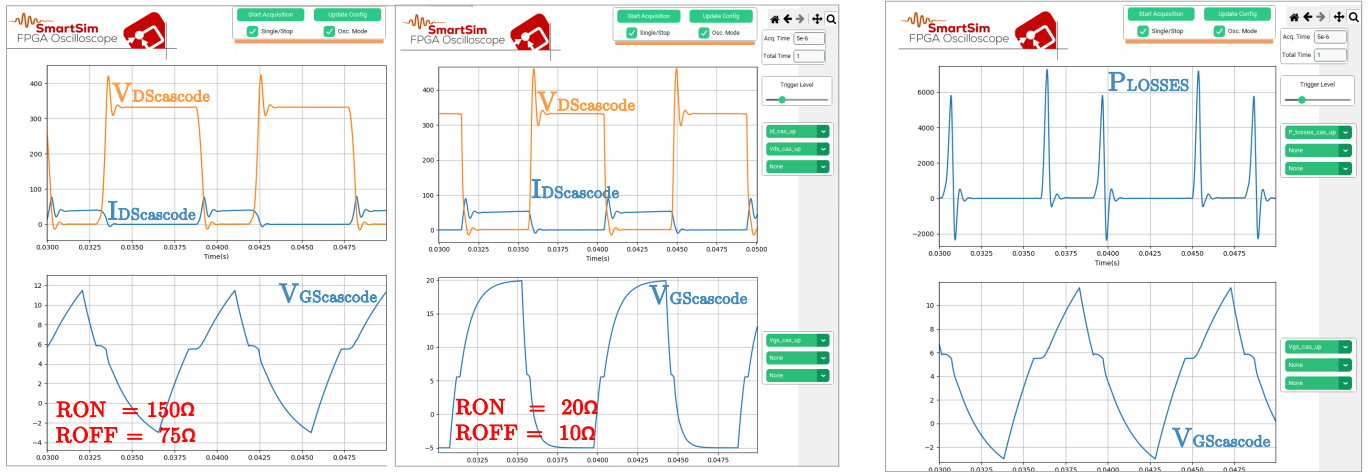


Usage example: Gate resistance variation and power losses

Quantification of the effect of gate resistance variation and instantaneous power losses.

Gate resistance decrease

Switching and conduction power losses



Characteristics

- Simulation of **switching power losses** bases on **actual turn-on, turn-off transitions**.
- **Parasitic lay-out effect** fully supported.
- **Parasitic device capacities** fully supported.
- True device models of Si MOSFET, SiC MOSFET, SiC Cascode and Si IGBT.



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