smart ctrl

control design for power electronics

SmartCtrl User's Guide 2024.1

by Power Smart Control S.L.

Power Smart Control SL

SmartCtrl User's Guide

2024.1 version

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1.1 Why SmartCtrl?

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Why SmartCtrl?

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SmartCtrl is the control designing tool for power electronics. It provides an easy to use interface for designing the control loop of almost any plant.

It includes the predefined transfer functions of some of the most commonly used power electronics plants, such as different DC-DC topologies, AC-DC converters, Inverters and motor drives.

However, it also allows the users to import their own plant transfer function by means of a text file. Therefore, this feature provides flexibility to design an optimize a control loop for almost any system, the plant, sensor and compensator can be user defined.

In order to ease the first attempt when designing a control loop, an estimation of the stable solutions space is given by the program under the name of "solutions map". Based on the selected plant, sensor and type of regulator, the solutions map provides a map of the different combinations of fc (Crossover Frequency) and phase margin that lead to stable systems.

Thus, the designer is able to select one of the points of the stable solutions space and to change the compensator parameters dynamically in order to adjust the system response to the user requirements in terms of stability, transient response, etc. since the program provides, at a glance, the frequency response of the system as well as the transient response and the compensator component values for the open loop given features. All of them are real time updated when any parameter of the system is varied by the designer.

The user can also work in S-domain or in Z-domain, for real digital control applications.

Key Features

✓ Pre-defined transfer functions of commonly used DC-DC converters, Power Factor Correction converters, sensors and regulators.

✓ Different control techniques for DC-DC converters are supported:
- Single control loop structures: voltage mode control and current mode control.
- Peak current mode control.
- Average current mode control implemented by means of two nested control loops

✓ Capability of designing the controller of any converter by means of:
- Modeling the converter using the basic models provided.
- Importing its frequency response data from a .txt file.
- Defining its transfer function through the equation editor.

✓ Capability of designing a generic control system, with customer definition for the plant, sensor and compensator.
✓ Real Digital control: working directly in Z-domain.
✓ Estimation of the stable solutions space ("Solutions Map").
✓ Sensitivity analysis of the system parameters.
✓ Real time updated results of the frequency response (Bode and Nyquist plots), transient response and the steady state waveforms.
✓ Possibility of importing and exporting any transfer function by means of .txt files.

1.2 Program Layout

Navigation: SmartCtrl >

Program Layout

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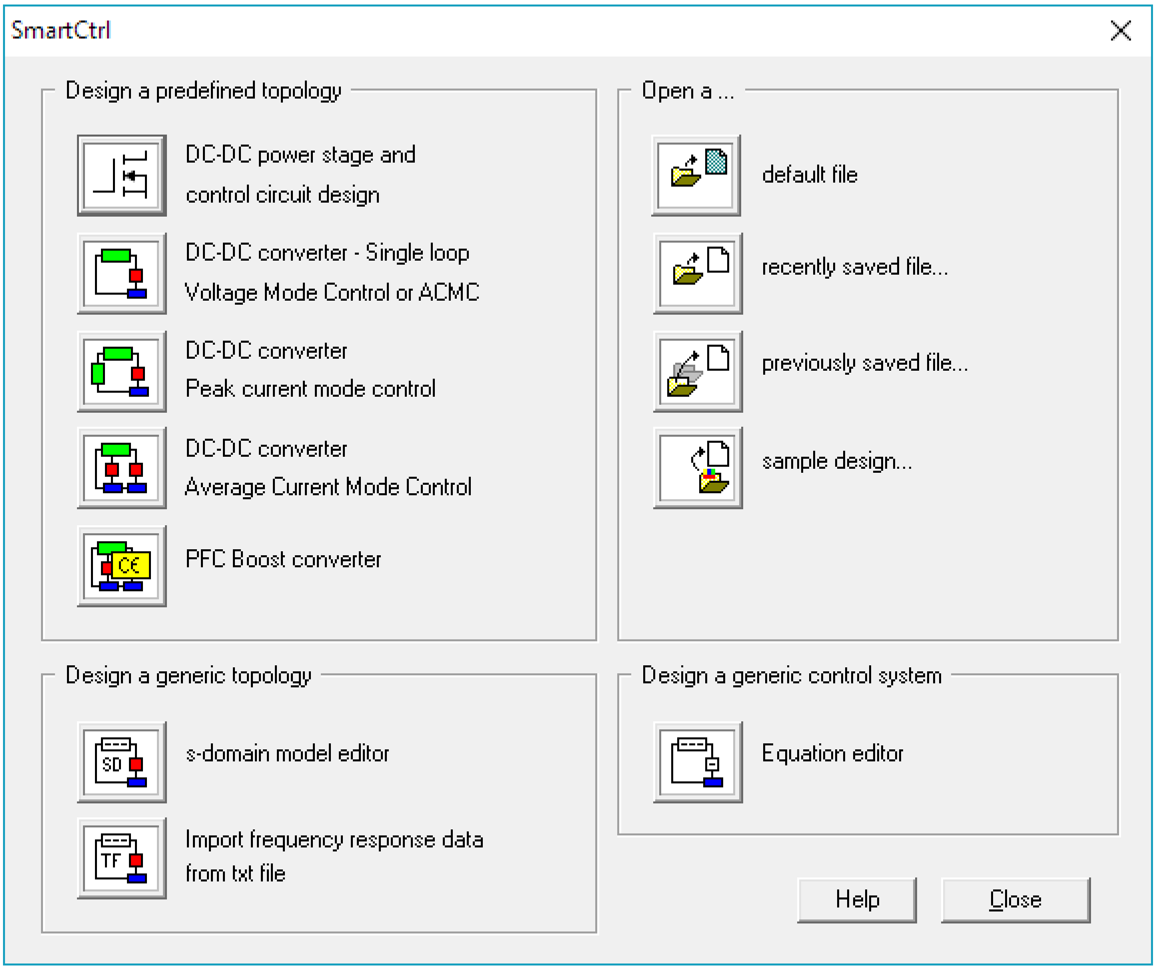
When SmartCtrl is started, all the available options are shown, and the user can select which of them is going to use. The aforementioned window is shown below. It is divided into four sections:



1. Design a predefined topology

This option provides an easy and straightforward way of designing the control circuit of the most widely used power converters. Through a guided process, the user will be able to select amongst different control strategies:

•DC-DC Power Stage and Control Circuit Design
•DC-DC Converter- Single loop

Two different control strategies are available in this case: voltage mode control and current mode control.

•DC-DC Converter - Peak Current mode control
•DC-DC Converter - Average current mode control

Two nested loops are needed to implement the average current mode control. The outer loop is a voltage mode control loop, and the inner one is a current mode control.

•PFC Boost converter

2. Design a generic topology.

This option allows to design a converter by two different ways:

•s-domain model editor.
•Importing the frequency response data from .txt file

3. **Design a generic control system - Equation editor.**
SmartCtrl also provides the option of defining the whole system though its equation editor. And so, help the user though the designing process of any control problem regardless its nature, for example temperature control, motor drives, etc

4. **Open...**

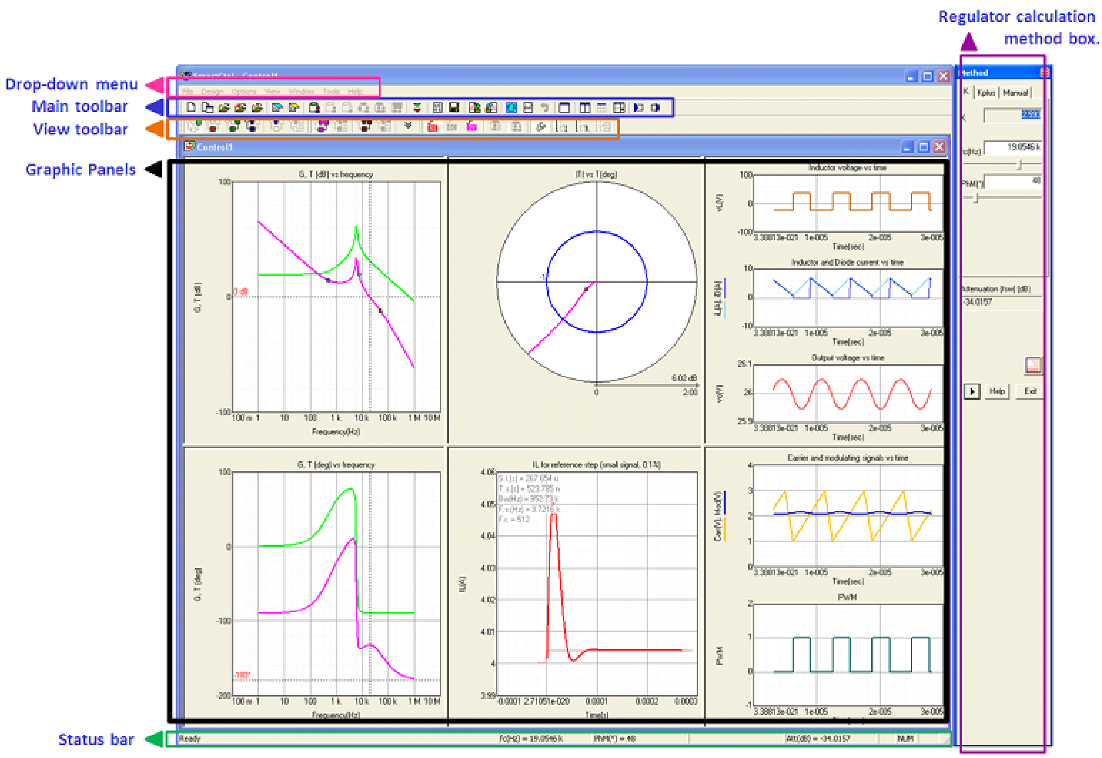
Default file. It opens a pre-designed example.
Recently saved file. It opens the last file the user worked with.
Previously saved file. It opens the folder where user used to save its designs
Sample design. It opens the folder where SmartCtrl examples have been previously recorded.

Regardless of the selected option, once the converter is completely defined, the main window of the program is displayed. Different areas are considered within the main window and all of them are briefly described below:

1. There are eight **drop-down menus**, this is:

File	It includes all the functions needed in order to manage files, import and export files, establish the printer setup and the print options.
Design	SmartCtrl libraries, modification of input data, access to the digital control settings (only available in SmartCtrl 2.0 Pro) and parametric sweep.
Options	For deactivating SmartCtrl licenses and check for updates
View	Allows the user to select which elements are displayed and which are not
Tools	Settings and Equation Editor access
Warehouse	Components library
Window	Functions to create, arrange and split windows
Help	SmartCtrl Help

2. The **Main Toolbar** provides quick access to the most commonly used program functions through left click on the respective icon.
3. The **View Toolbar** icons allows the user a quick selection of the elements displayed.
4. The Status Bar summarizes the most important parameters of the open loop control design (cross frequency, phase margin and attenuation at the switching frequency)
5. The compensator **Design Method Box** includes the three **calculation methods of the compensator** as well as the **Solution Map**.
6. **Graphic and text panels** include the most relevant information of the system: frequency response, polar plot, transient response and steady-state waveforms. To access the help topic regarding each panel just right click on that panel.



1.3 Main menus and toolbars

1.3.1 File Menu

Navigation: SmartCtrl > Main menus and toolbars >

File Menu

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New	Create a new project (Ctrl+N)
New and initial dialog	Create a new project and display the initial dialog box
Open	Open an existing project (Ctrl+O)
Open sample designs	Open a sample design from the examples folder
Close	Close the current project window
Save	Save the current project (Ctrl+S)
Save as...	Save the current project to a different file
Open txt files	Open any .txt file in Notepad

Import (Merge) Merge data of another file with the data of the existing file for display. The curves of these two files will be combined. (Ctrl+M)

Export The program provides different exporting options. It allows exporting the following.

- **Export to PSIM** the schematic and the parameters file, or update parameters file
- **Export to FPGA** the digital compensator design (more information)
- **Export transfer functions** to a file. The available transfer functions are: plant, sensor, control to output, compensator, digital, inner loop etc.
- **Export transient responses** to a file. The available transient responses are: voltage reference step, output current step and input voltage step
- **Export waveforms** to a file. The available steady state waveforms are: inductor voltage and current, diode voltage and current, carrier, modulating signal and PWM.

Generate report Generate a report to either a .txt file or notepad. It contains information regarding both the input data (steady-state dc operating point, plant input data, ...) and output data (compensator components, cross frequency, phase margin, ...)

Print preview Preview the printout of any of the graphic and text panels (Transfer function magnitudes (dB), Transfer function phase (º), Nyquist diagram, Transients, Data input, Results)

Print Print any of the panels of the main window (bode plots, Nyquist diagram, transient, input data or results)

Printer setup Setup the printer

Exit Exit SmartCtrl

1.3.2 Design Menu

Navigation: SmartCtrl > Main menus and toolbars >

Design Menu

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The SmartCtrl Design Menu contains the elements that can be used in the SmartCtrl schematic. The library is divided into the following sections:

Predefined topologies Contains the most commonly used DC-DC plants both in single and double loop configurations, as well as AC-DC plants.

Generic Topology Allows the user to define a generic plant transfer function either in s-domain or importing a .dat, .txt, or .fra file; uses the predefined sensors provided by SmartCtrl and, for the compensator, the user can select among the proposed types or define a compensator using the transfer function to design the closed-loop control system.

Generic Control System Allows the user to define the plant and the sensor transfer functions through the built-in equation editor. For the compensator the user can select among the proposed types or define a compensator using the transfer function.

Modify Data Open the schematic window of the current project to modify the parameters.

Digital control Access to the digital control settings (only available from SmartCtrl 2.1 Pro).

Parametric Sweeps Allows performing the sensibility analysis of the system parameters. It is divided into three different parametric sweeps: Input Parameters, Compensator Components and digital factors.

Reset all Clear the active window

1.3.3 Options Menu

Navigation: SmartCtrl > Main menus and toolbars >

Option Menu

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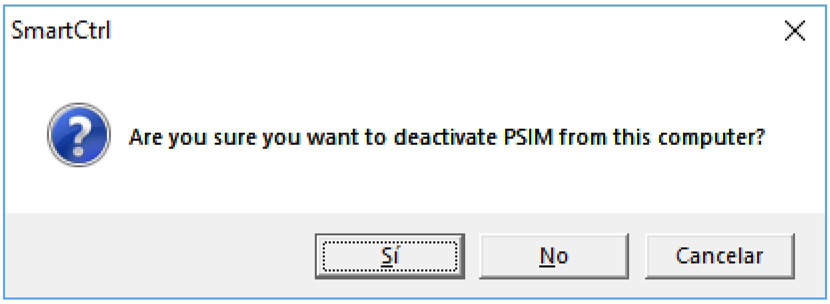
Deactivate When the user check the option DEACTIVATE the following message will appear:



When SmartCtrl is launched, it will contact the license server and activate the license.

For NETWORK licenses, when SmartCtrl exists it will automatically deactivate the license, and someone else can use it.

However for STAND ALONE licenses, the license will not be deactivated, it will remain active for 7 days on this computer, so considering this type of license can be used with 2 different computer IDs, it is recommendable to deactivate the license in one of them if the user is planning to use the other.

Note that activating / deactivating the license requires internet connection.

Check for software updates... Check for a new version of SmartCtrl available

This option will run the program SmartCtrlUpdate.exe to check if there is a new version available.

1.3.4 View Menu

Navigation: SmartCtrl > Main menus and toolbars >

View Menu Previous Top Next

Comments Open the comments window. It allows the user to add comments to the design. These comments will be saved together with the designed converter.

Loop Select the loop to be displayed in the active window (inner or outer loop).

Transfer Functions Select the transfer function to be displayed:

- •Plant transfer function, G(s)
- •Sensor transfer function, K(s)
- •Compensator transfer function, R(s)
- •Control to output without regulator transfer function, A(s)
- •Control to output transfer function, T(s)
- •Reference to output transfer function, CL(s)
- •Digital compensator transfer function
- •Digital control to output transfer function
- •Digital reference to output transfer function

Additional transfer functions Select the additional transfer functions to be displayed, like the audiosusceptibility Gvv, the output impedance Gvi, etc. For more information regarding these transfer function, see **view toolbar**.

Transients Select the transient response to be displayed.

The available transient responses are:

•Input voltage step transient
•Output current step transient
•Reference step transient.

Organize panels Resize all panels and restore the default appearance of the graphic and results panels window.

Enhance Select the panel to be displayed in full screen size

•Bode (magnitudes) panel	(Ctrl+Shift+U)
•Bode (phase) panel	(Ctrl+Shift+J)
•Nyquist diagram panel	(Ctrl+Shift+I)
•Transient responses panel	(Ctrl+Shift+K)
•Input data panel	(Ctrl+Shift+O)
•Output (results) panel	(Ctrl+Shift+L)

Input data View design input data

Output data View design output data

1.3.5 Tools Menu

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Tools Menu

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Settings It allows the customization of the frequency range (frequency settings) and the default re-arrangement of the graphic and text panels to their default size and appearance (Layout settings)

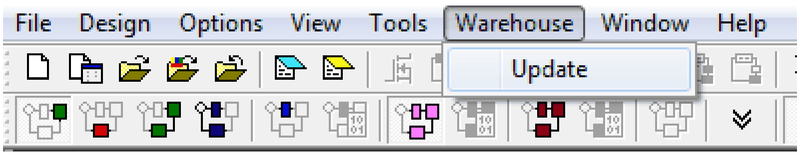
Equation editor The equation editor provides direct access to the SmartCtrl built-in Equation editor. Through the Equations ditor, SmartCtrl allows the user to program any transfer function, export its frequency response and afterwards, if needed, import and visualize it within the Bode plots graphic panel

1.3.6 Warehouse Menu

Navigation: SmartCtrl > Main menus and toolbars >

Warehouse Menu Previous Top Next

SmartCtrl provides a wide selection of different components used in the design of power circuits, called warehouse. This database is available through the next button:



For more information: **Warehouse**

1.3.7 Window Menu

Navigation: SmartCtrl > Main menus and toolbars >

Window Menu Previous Top Next

New Window Create a new window

Maximize active window Maximize the current window

Cascade Arrange the windows in cascade form

Tile horizontal Tile the currently open windows horizontally

Tile vertical	Tile the currently open windows vertically
Split	Click on the intersection of the lines that delimit the different window panels and drag. This will change the size of the panels
Organize all	It restores the default size of the graphic and text panels

.

1.3.8 Help Menu

Navigation: SmartCtrl > Main menus and toolbars >

Help Menu Previous Top Next

What's new in this version	New features included in the last SmartCtrl version
Contents	Help file
About SmartCtrl...	SmartCtrl information

1.3.9 Main toolbar

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Create a new project


Create a new project and open initial dialogue box


Open an existing project

Open sample design

Close the current project window

Generate report

View document comments

DC-DC complete design (Power stage and control circuit)

DC-DC converter - Single loop

DC-DC converter - Peak Current Mode Control

DC-DC converter - Average Current Mode Control

PFC Boost converter

Design a generic topology using a s-domain model editor

Design a generic topology from a .txt file

Design a generic control system

Modify data

Modify data

Digital control settings

Save the current project

 Export transfer functions

 Import transfer function from a file and merge with other Transfer Functions

 Export to PSIM (schematics)

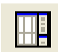
 Export to PSIM (update parameter file)

 Update parameters file of the previously exported schematic

 Maximize active window

 Tile windows

 See all panels

 Organize all panels

 View input data

 View output data

1.3.10 View toolbar

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View toolbar

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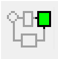
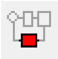
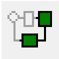
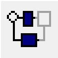
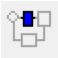
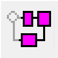
 Display the frequency response (Bode plot) of the plant transfer function

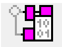
 Display the frequency response (Bode plot) of the sensor transfer function

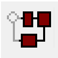
 Display the frequency response (Bode plot) of the control to output without compensator transfer function

 Display the frequency response (Bode plot) of the sensor-compensator transfer function

 Display the frequency response (Bode plot) of the compensator transfer function

 Display the frequency response (Bode plot) of the control to output transfer function

 Display the frequency response (Bode plot) of the control to output transfer function with digital control

 Display closed loop transfer function

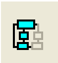
 Display closed loop transfer function with digital control

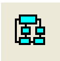
 Display transient response due to a reference voltage step

 Display the transient response due to an output current step

 Display the transient response due to an input voltage step

 Additional waveforms (for Phase Shifted Full Bridge converter)

 View inner loop

 View outer loop

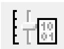
 Launch inner method box / Display inner loop results

 Enables or disables the display of the compensator calculation method toolbox. Launch outer method box or Method box / Display outer loop results

 Modify input parameters (Input Parameters Parametric sweep)

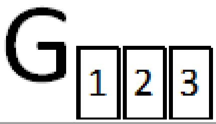
 Modify compensator components (Compensator Parameters Parametric sweep)

 Source code parametric sweep (Modify Plant and sensor components defined in the Equation Editor)

 Digital factors sweep

SmartCtrl additional transfer functions

All those transfer functions colored in grey are not allowed for the design. The nomenclature of the transfer functions is as follows:



1	Subscript 1 refers to the type of transfer function studied. The character t denotes that the transfer function has been evaluated in closed loop; otherwise it refers to open loop.
2	Subscript 2 refers to the perturbed magnitude: **iL:** inductor current. **iD:** diode current. **vo:** output voltage
3	Subscript 3 refers to the perturbing magnitude: **io:** output current.

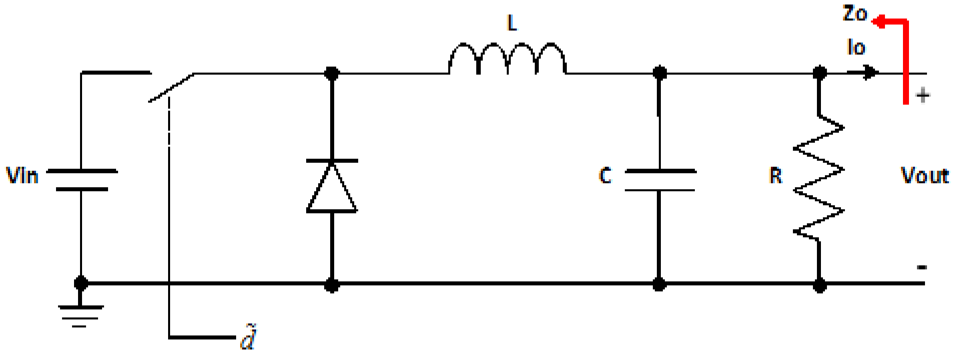
	vi: input voltage.

The considered transfer functions are:

Open loop transfer functions.	
$Gvvi = \frac{\tilde{v}_o}{\tilde{v}_i}$	Open loop Audiosusceptibility
$Gvio = \frac{\tilde{v}_o}{\tilde{i}_o}$	Open loop Output impedance
$GiLvi = \frac{\tilde{i}_L}{\tilde{v}_i}$	Open loop Input voltage to inductor current transfer function.
$GiLio = \frac{\tilde{i}_L}{\tilde{i}_o}$	Open loop Output current to inductor current transfer function.
$GiDvi = \frac{\tilde{i}_D}{\tilde{v}_i}$	Open loop Input voltage to diode current transfer function.
Closed loop transfer functions.	
$Gtvvi = \frac{\tilde{v}_o}{\tilde{v}_i}$	Closed loop Audiosusceptibility
$Gtvio = \frac{\tilde{v}_o}{\tilde{i}_o}$	Closed loop Output impedance
$Gtivi$	Closed loop Input voltage to inductor current or diode current transfer function
$Gtiio$	Closed loop Output current to inductor current or diode current transfer function

The nomenclature will be clarified through two examples.

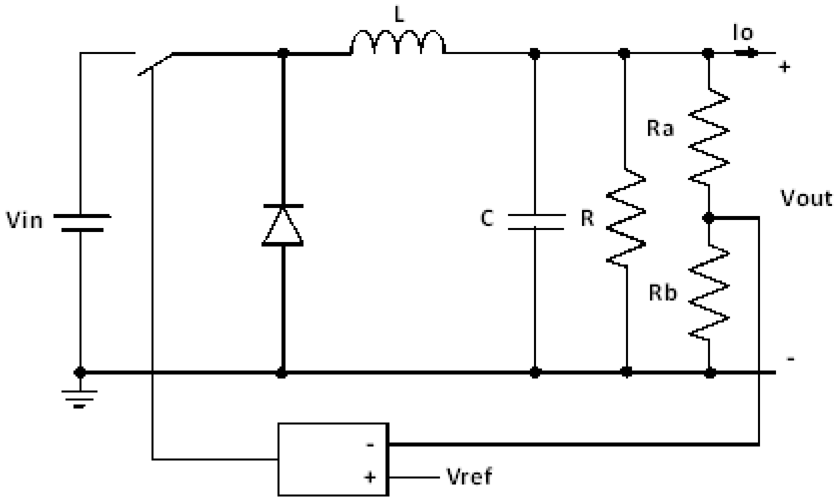
Example 1: Open loop transfer function.



$$Gvio = \frac{\tilde{v}_o}{\tilde{i}_o}$$

Load resistor is included within the output impedance transfer function

Example 2: Closed loop transfer function.



$$Gtvio = \frac{\tilde{v}_o}{\tilde{i}_o}$$

Closed loop Output impedance transfer function

1.4 Design a predefined topology

Navigation: SmartCtrl >

Design a predefined topology

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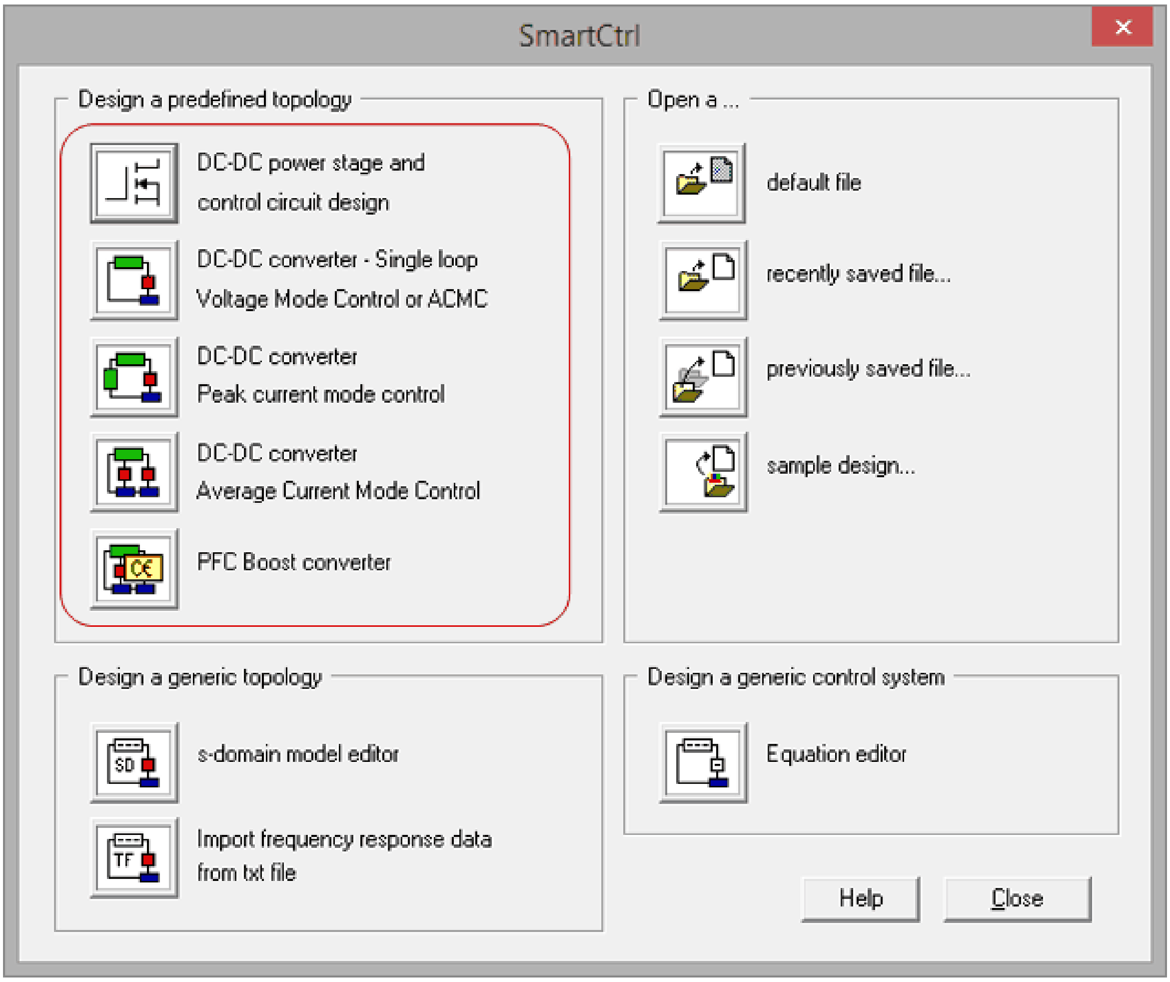
The most widely used topologies are available as pre-defined topologies, in order to ease their design.



The available pre-designed topologies are:

•**DC-DC power stage and control design.**

•**DC-DC converter - Single loop (Voltage mode control and current mode Control).**
•**DC-DC converter - Peak current mode control.**
•**DC-DC converter - Average current mode control.**
•**PFC Boost converter**

1.4.1 DC-DC power stage and control design

Navigation: SmartCtrl > Design a predefined topology >

DC-DC power stage and control design

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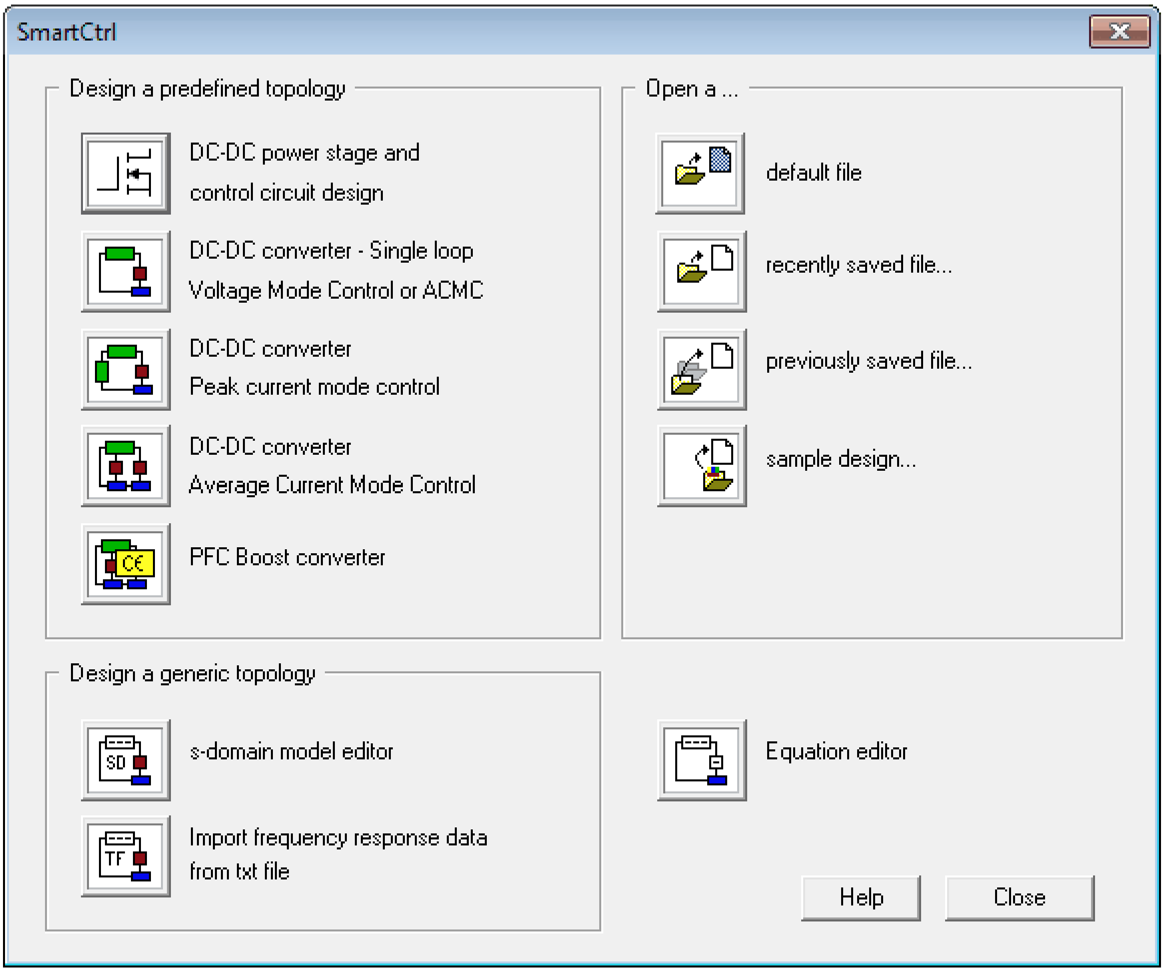
If this option is selected, SmartCtrl helps to design a complete DC-DC converter (plant, sensor and controller) from simple specifications.



Predefined topologies for this option are:

•Buck

•Boost

•Buck-boost

•Forward

•Flyback

All these topologies are designed for a Continuous Conduction Mode (CCM), and a simple Voltage Control Mode (VCM).

The first step is to **specify the characteristics of the circuit**. These are:

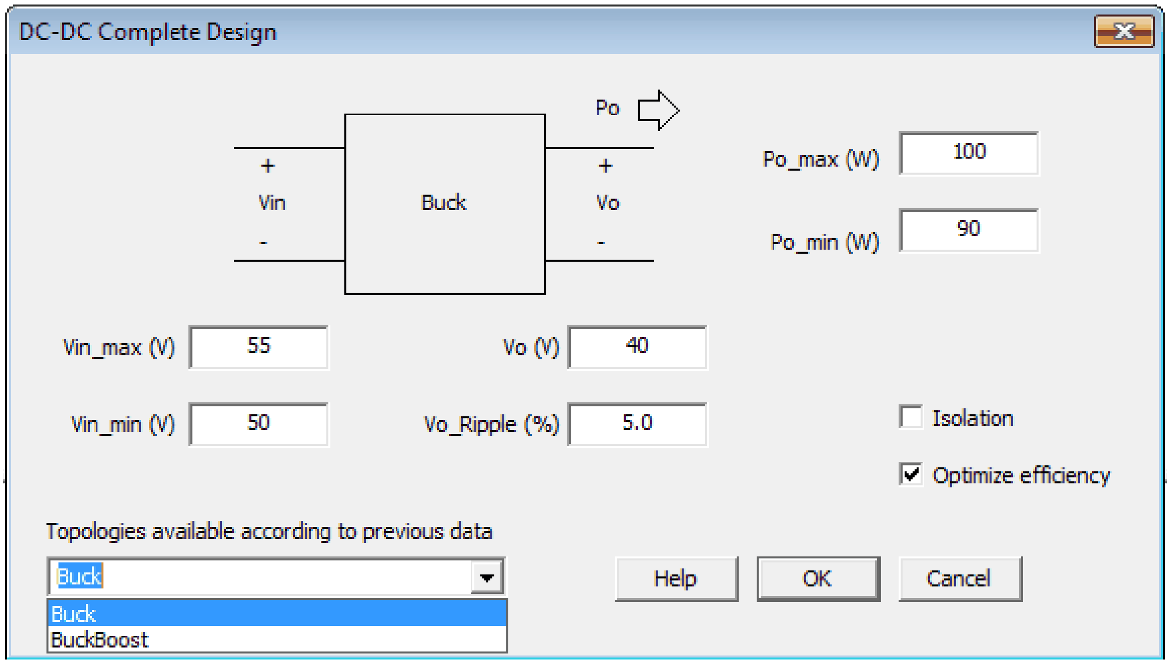
•Input voltage range (maximum and minimum)

•Output voltage

•Maximum output voltage ripple

•Ouput power range

If desired, the check box Isolation can be selected to use a topology with isolation (Forward or Flyback).

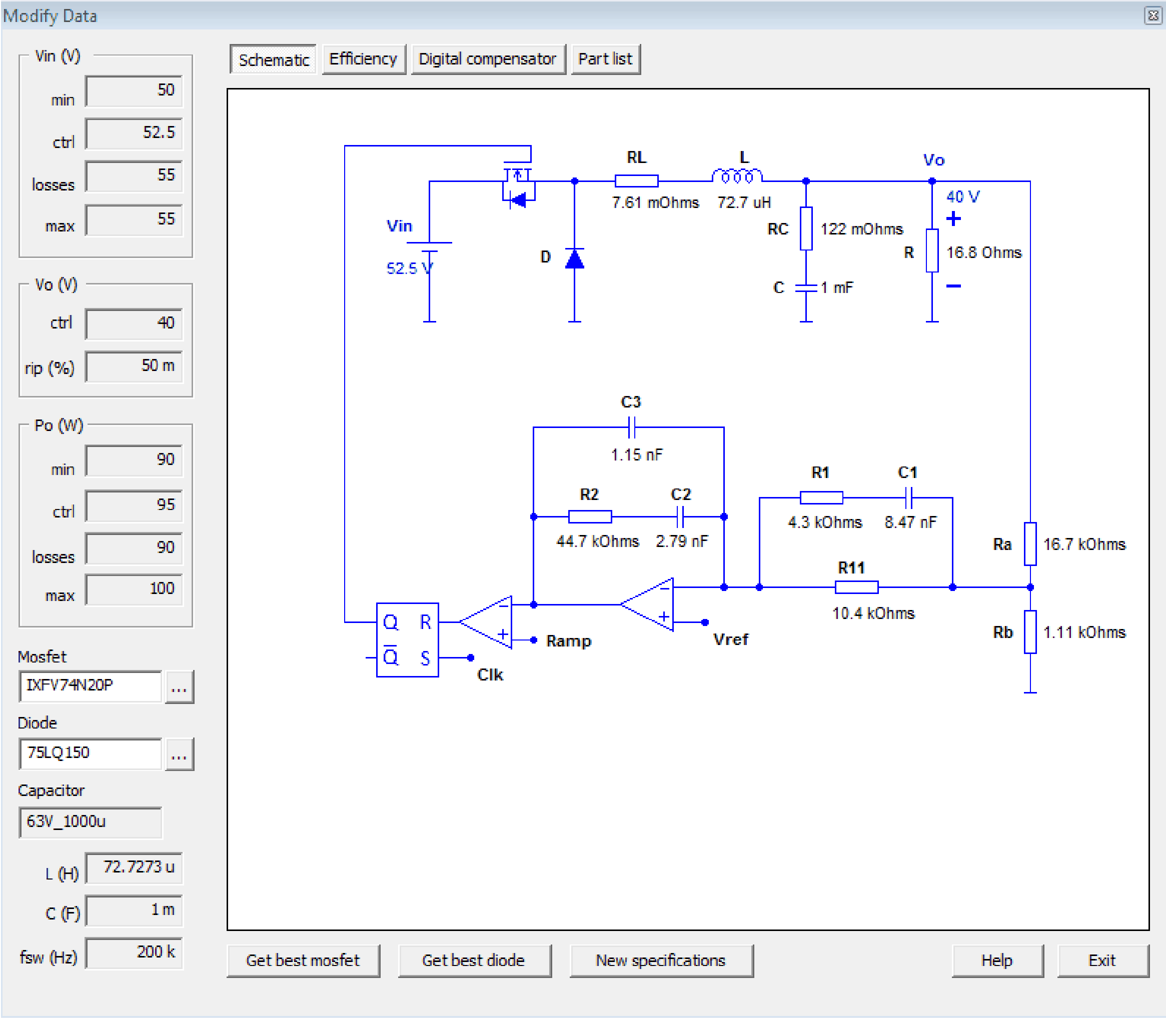


SmartCtrl determines the available topologies for these specifications. Once a topology has been selected, click on Ok button.

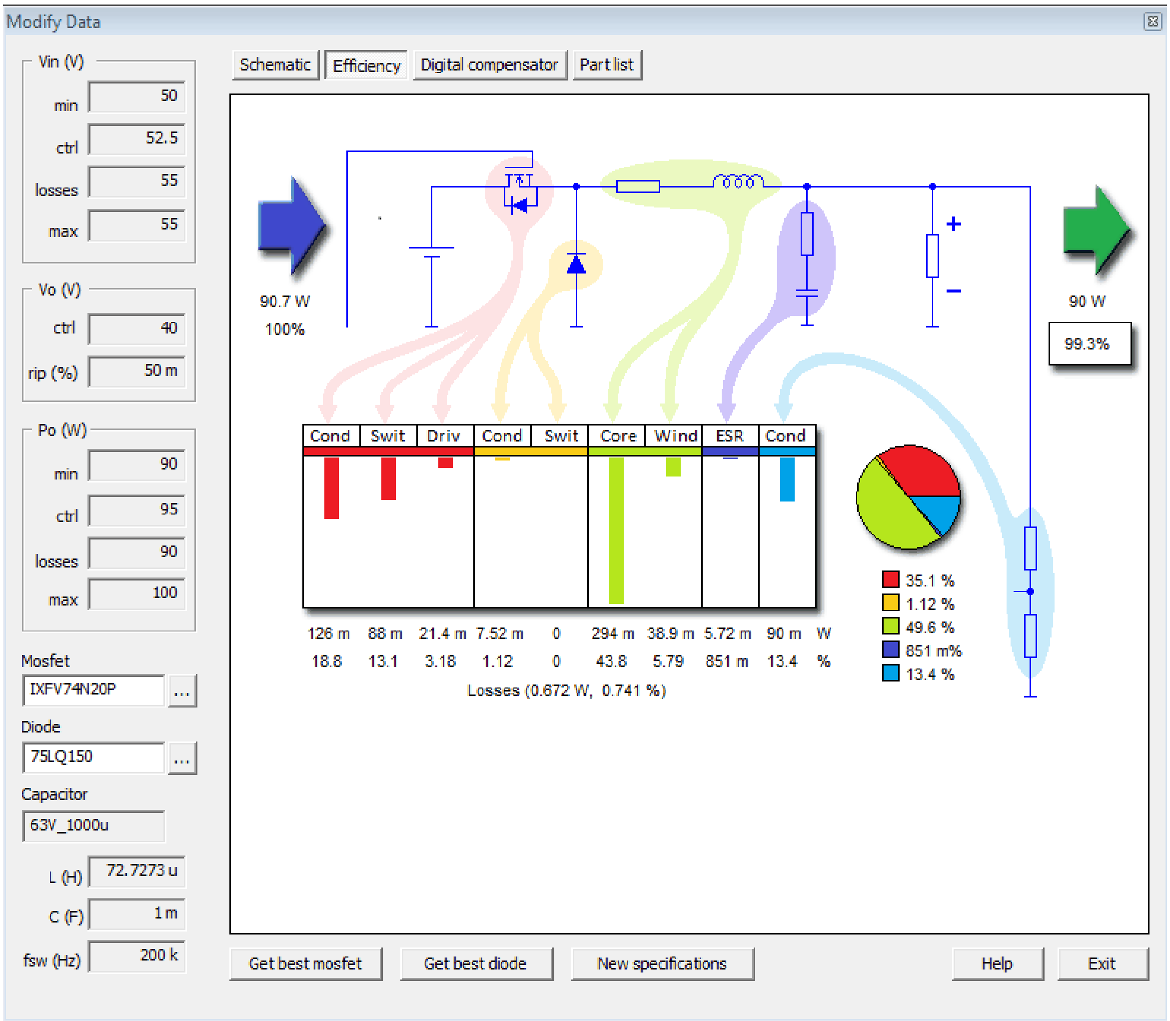
After that, a new window is shown with four tabs:

- Schematic
- Efficiency
- Digital compensator
- Part list

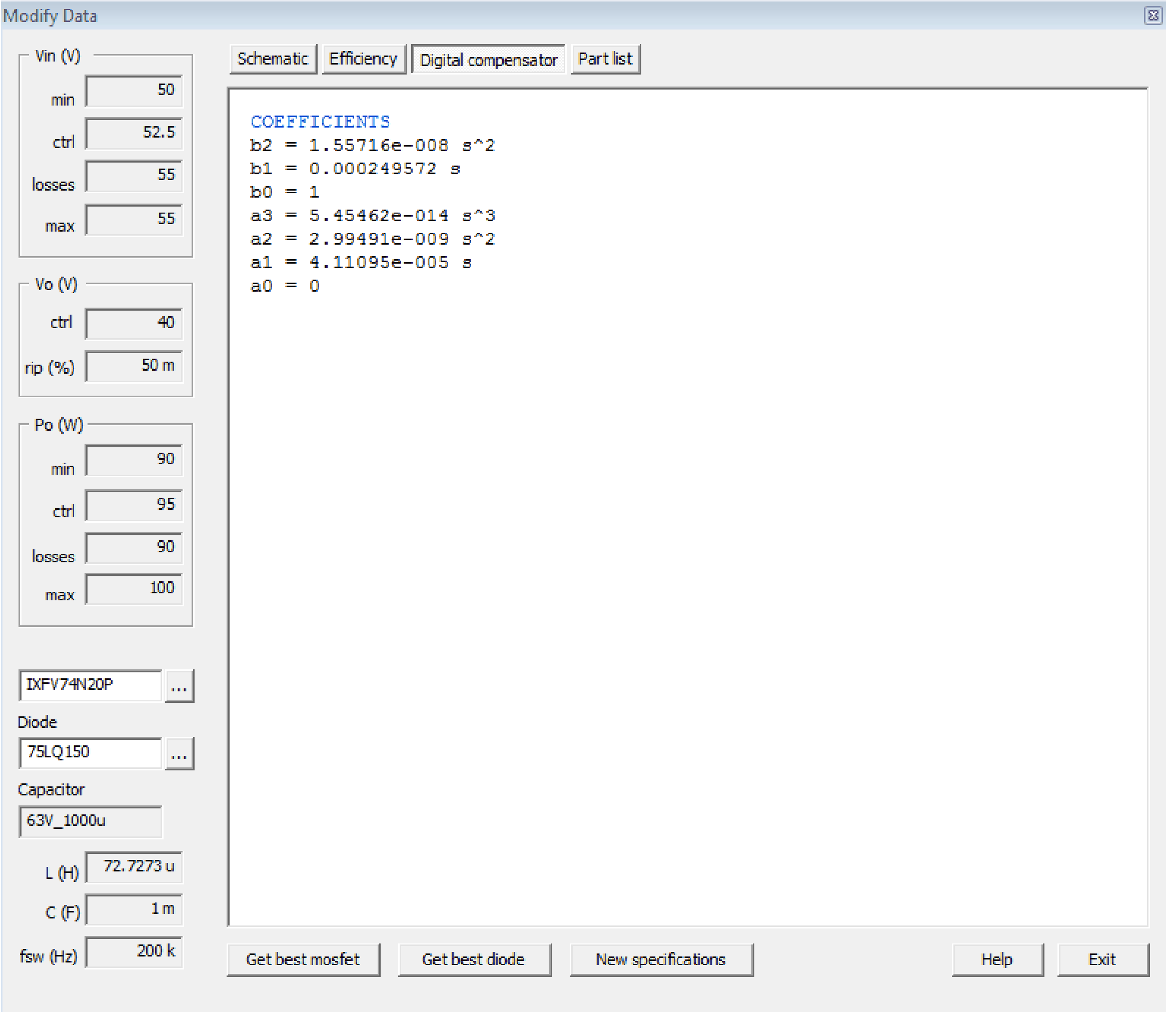
In the tab **Schematic**, the complete circuit is shown, including sensor and regulator. All values are detailed on each component.



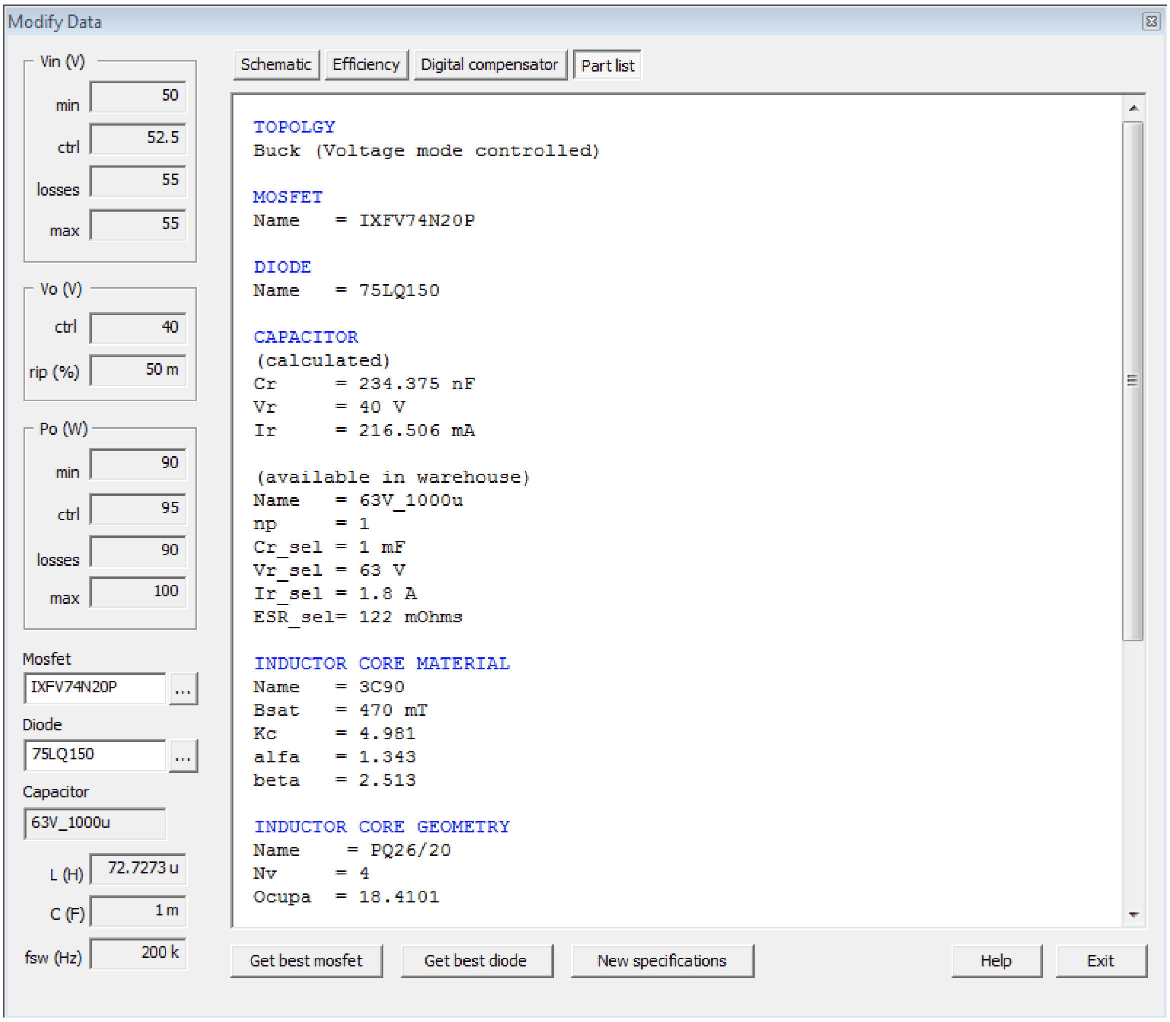
If the tab **Efficiency** is selected, the information about the loses in each component is shown.



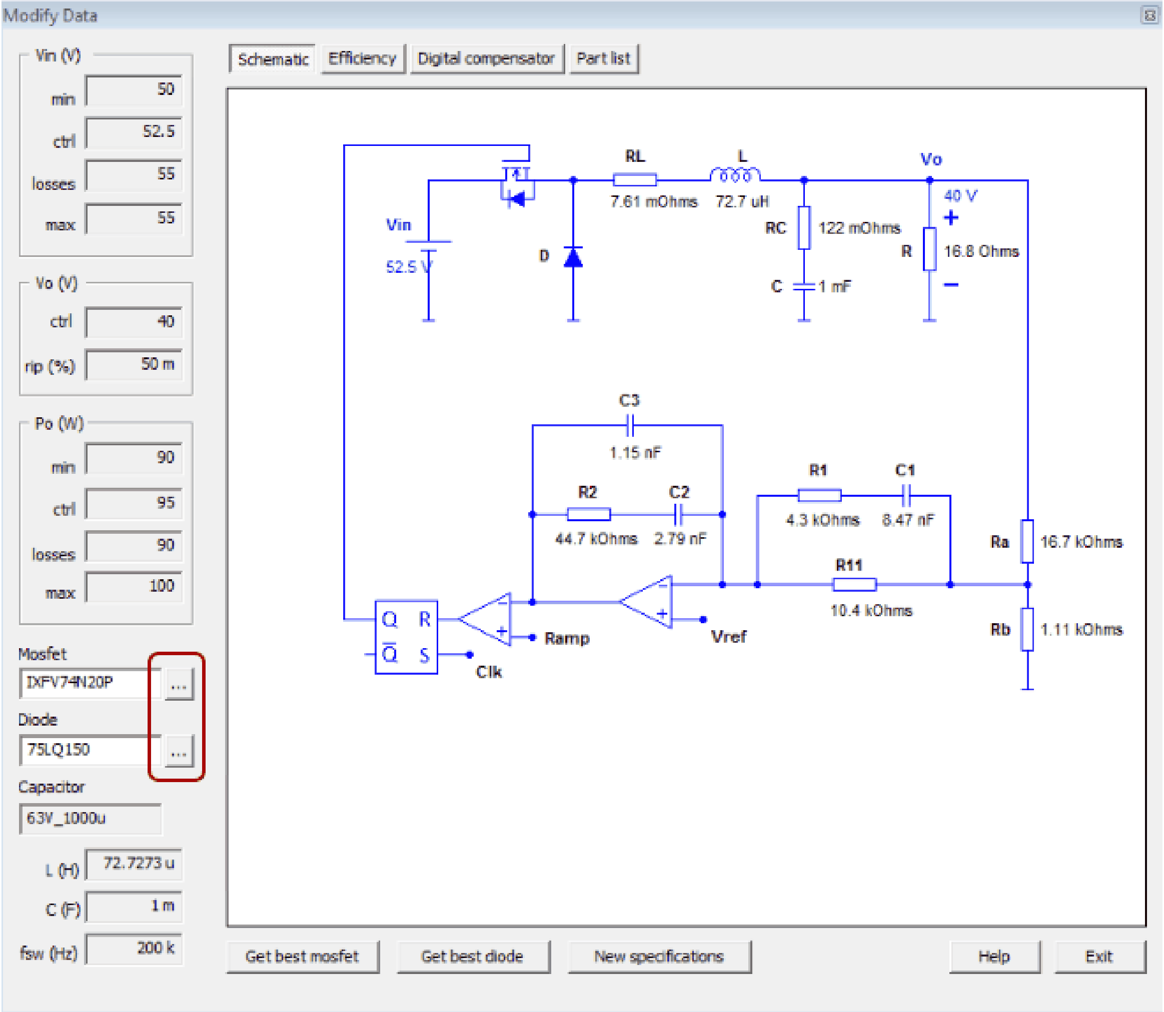
In the tab **Digital compensator** the coefficients for a digital control are shown.



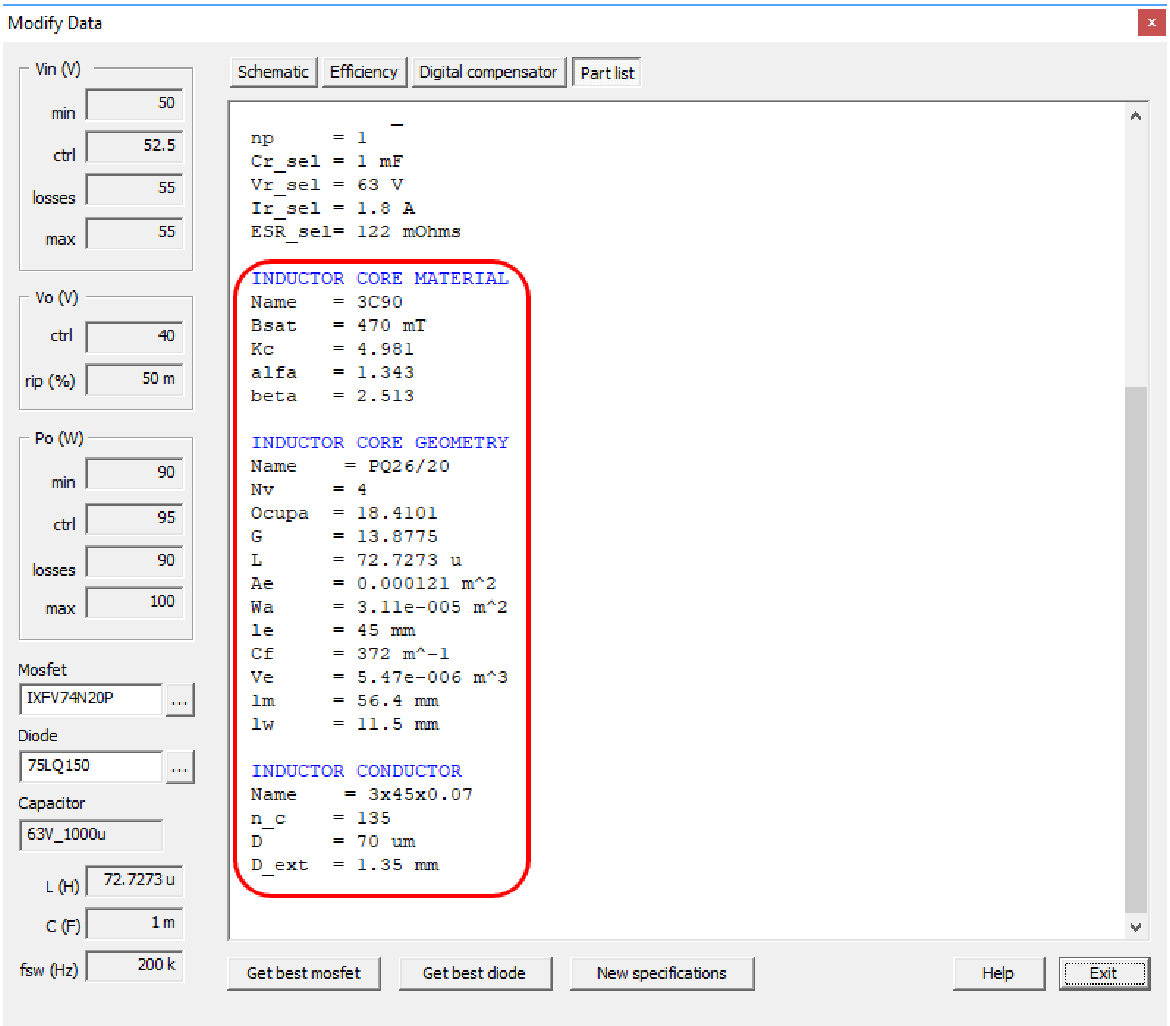
In the tab **Part list** there is a list with the components from the warehouse selected for the optimum design.



In any of these tabs, it is possible to change the selected diode and MOSFET between the available ones in the warehouse by clicking in the buttons marked in the next picture:

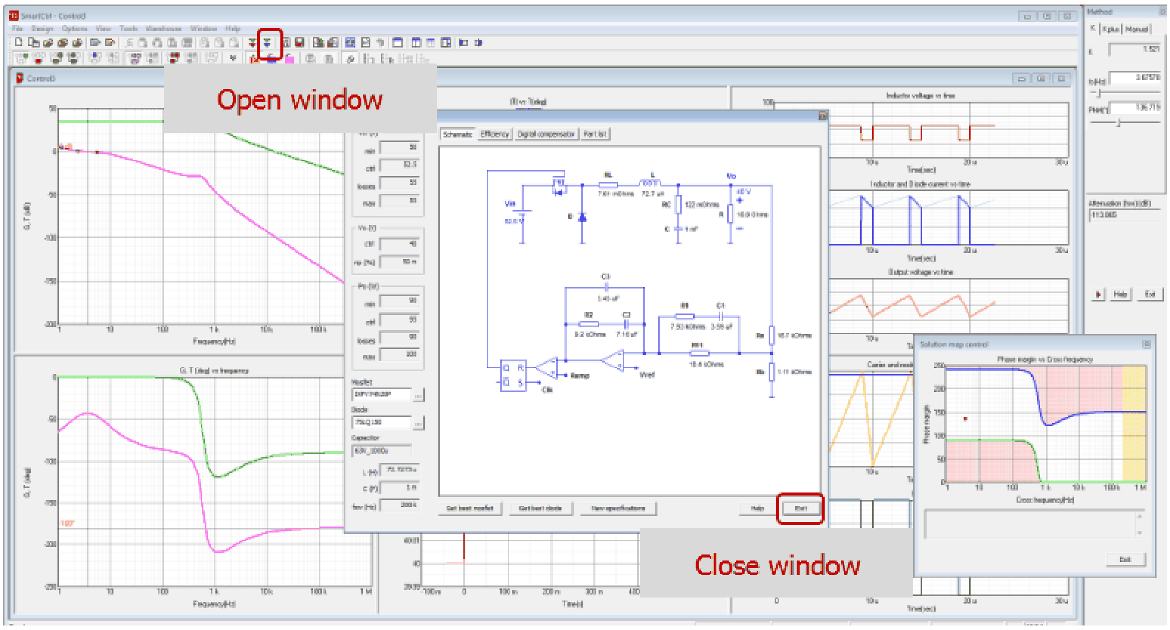


In this part list the user also gets information about how to build the **inductor** used in the design, with complete details about the core material, core geometry and wire and number of turns.



Once the system has been defined, the designer can select a point within the solution space. The variations of this design will be updated automatically in the solutions window.

The window with the results off the design can be closed and opened by clicking in the buttons marked in the next picture:



1.4.2 DC-DC Converter - Single loop

Navigation: SmartCtrl > Design a predefined topology >

DC-DC Converter - Single Loop

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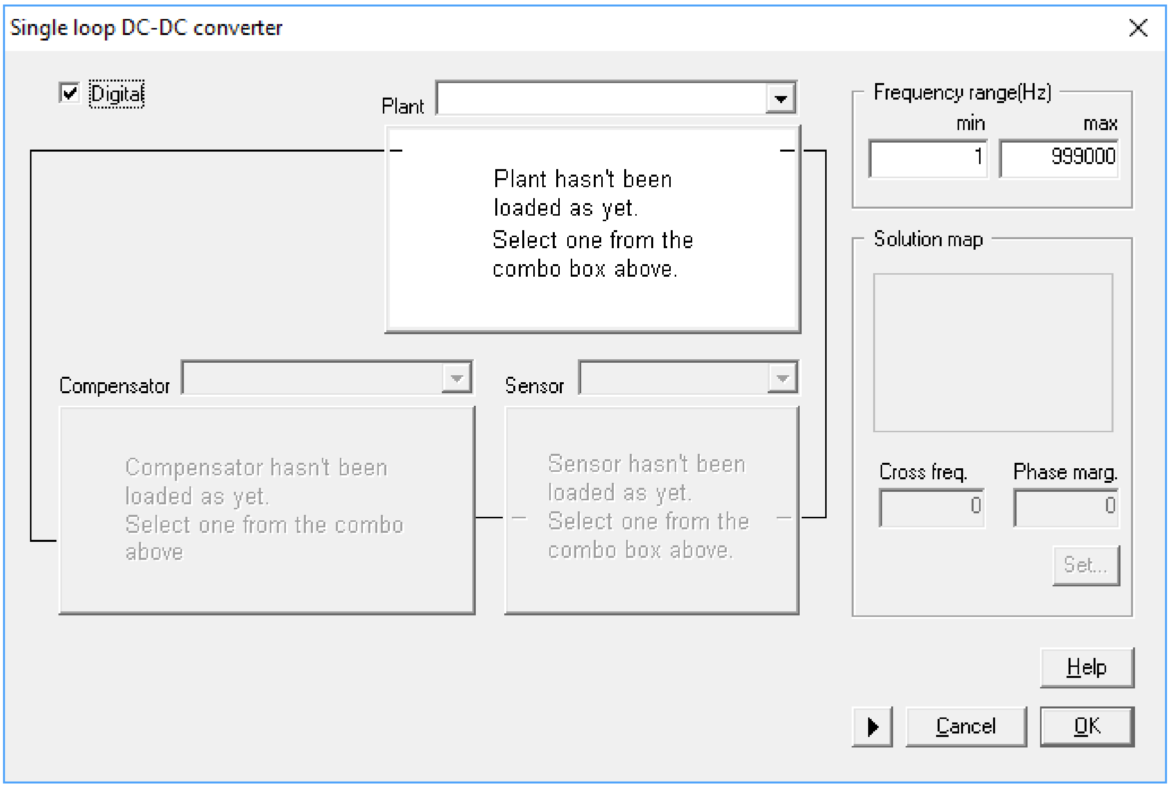
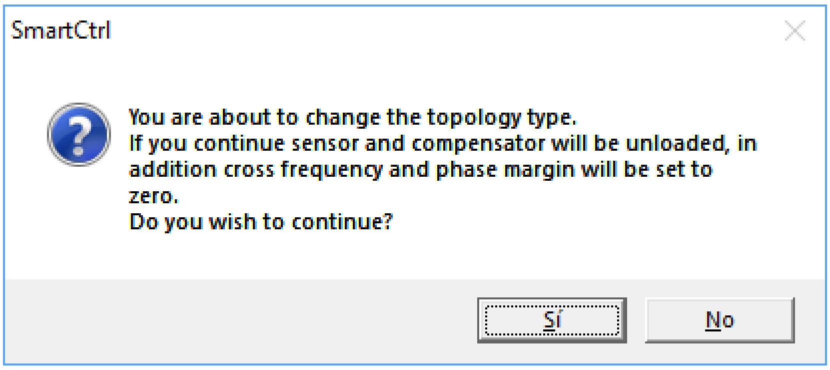
The single loop is formed by three different transfer functions: plant, sensor and compensator, which must be selected sequentially.

First of all the user should decide if is going to define a **digital control or an analog control**. This check box should be selected since the beginning because it determines the different options that can be selected further on.

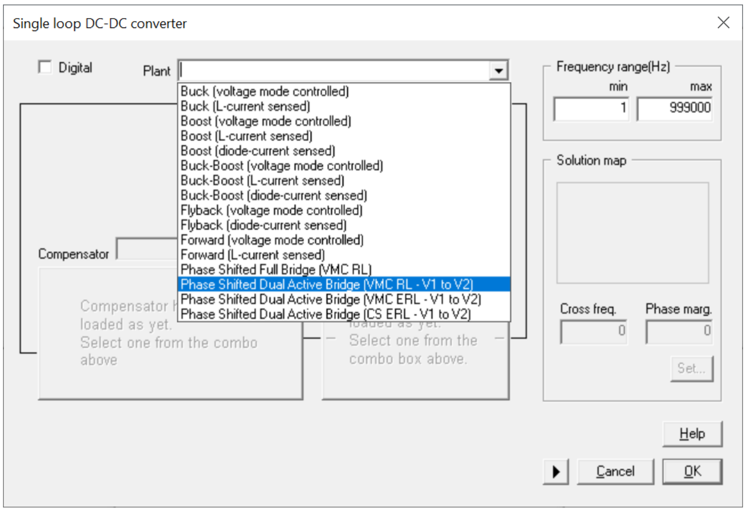


In case this check box is modified during the design process, the user will receive an error message and it will start again in the single loop DC-DC converter window.



For both options, analog or digital control, the user should follow the same steps.

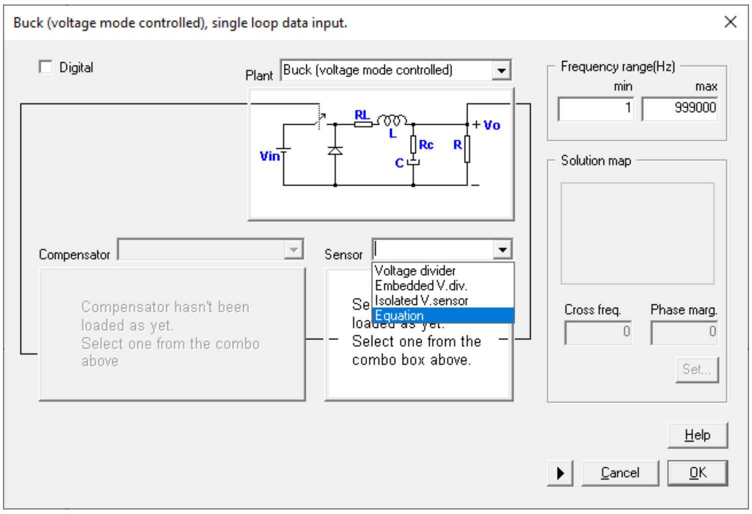
The first step is to define the system is the selection of the plant. The plant can be either a pre-defined one or a user defined one. This is, the user can import a generic transfer function by means of a .txt file or select one of the pre-defined topologies.



The predefined DC-DC plants are the following:

- [Buck]
- [Buck-Boost]
- [Boost]
- [Flyback]
- [Forward]
- •[Phase Shifted Full Bridge (VMC RL)]
- •[Phase Shifted Dual Active Bridge (VMC RL - V1 to V2)]
- •[Phase Shifted Dual Active Bridge (VMC ERL - V1 to V2)]
- •[Phase Shifted Dual Active Bridge (CS ERL - V1 to V2)]

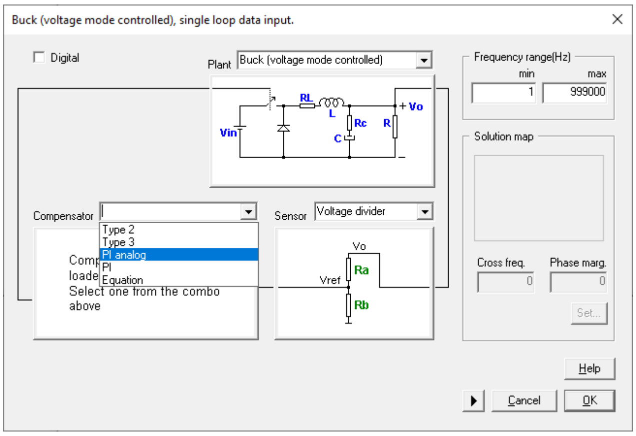
Once the plant has been selected, considering if the magnitude to be controlled is voltage or current and if the control is analog or digital, the program will display the appropriate type of sensor.



The different sensors available are the following:

- [Voltage Divider]
- [Embedded Voltage Divider]
- [Isolated Voltage Sensor]
- [Current Sensor]
- [Hall Effect Sensor]
- •[Equation Editor (User Defined Sensor)]

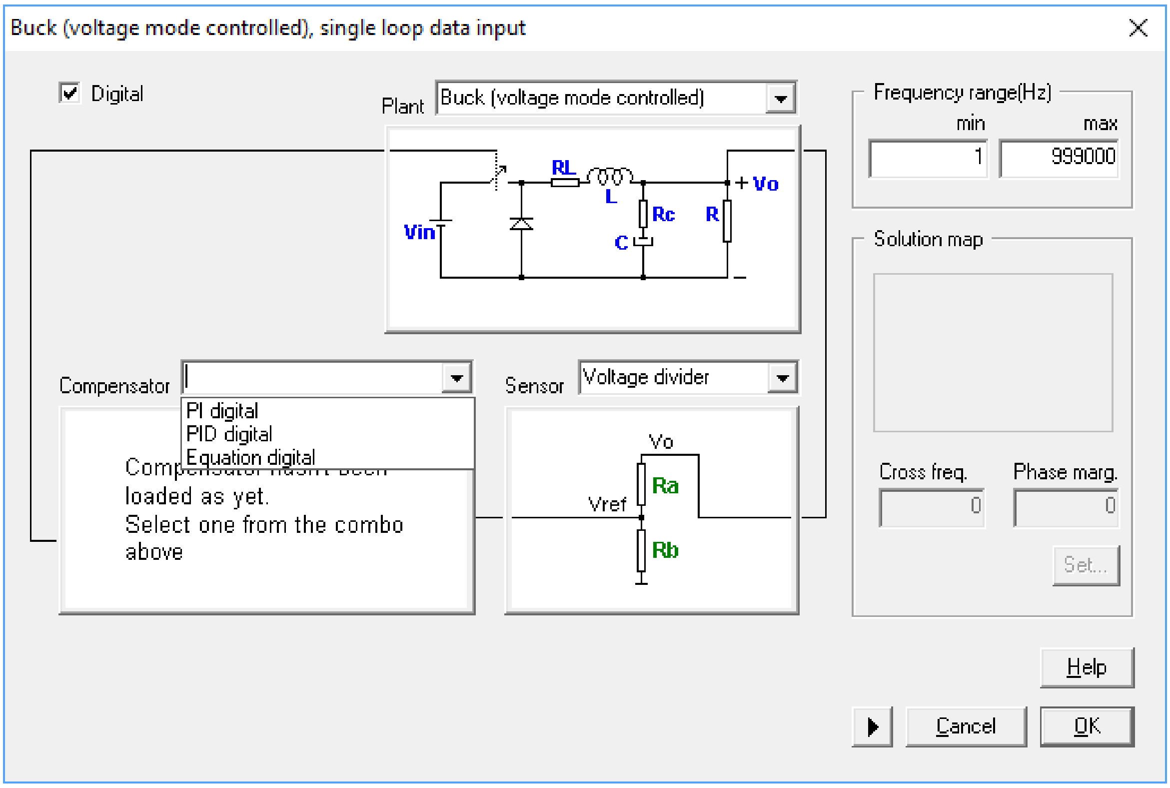
Finally, the compensator is selected, considering the suitable compensator according to the predefined DC-DC plant selected and if the design is digital or analog.
The user can select among the ones provided by SmartCtrl or use the Equation Editor to define the compensator transfer function:



Compensator types:

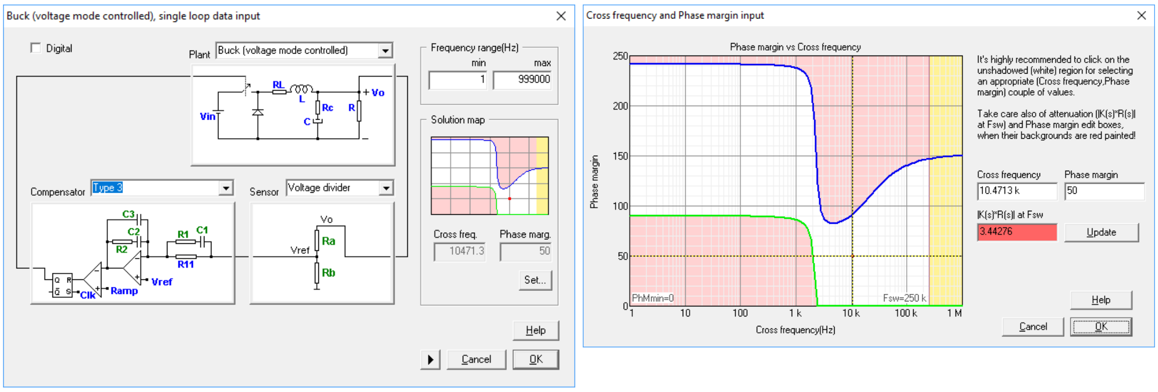
- [Type 3](#)
- [Type 3 Unattenuated](#) (when selecting Embedded Voltage Divider sensor)
- [Type 2](#)
- [Type 2 unattenuated](#) (when selecting Embedded Voltage Divider sensor)
- [PI](#)
- •[PI analog](#)
- [PI unattenuated](#) (when selecting Embedded Voltage Divider sensor)
- [Single Pole](#)
- [Single Pole unattenuated](#) (when selecting Embedded Voltage Divider sensor)
- •User defined compensator using [Equation Editor](#)

In case a digital control is selected from the beginning, only the digital compensators or the Equation Editor for custom defined compensator, will be available.

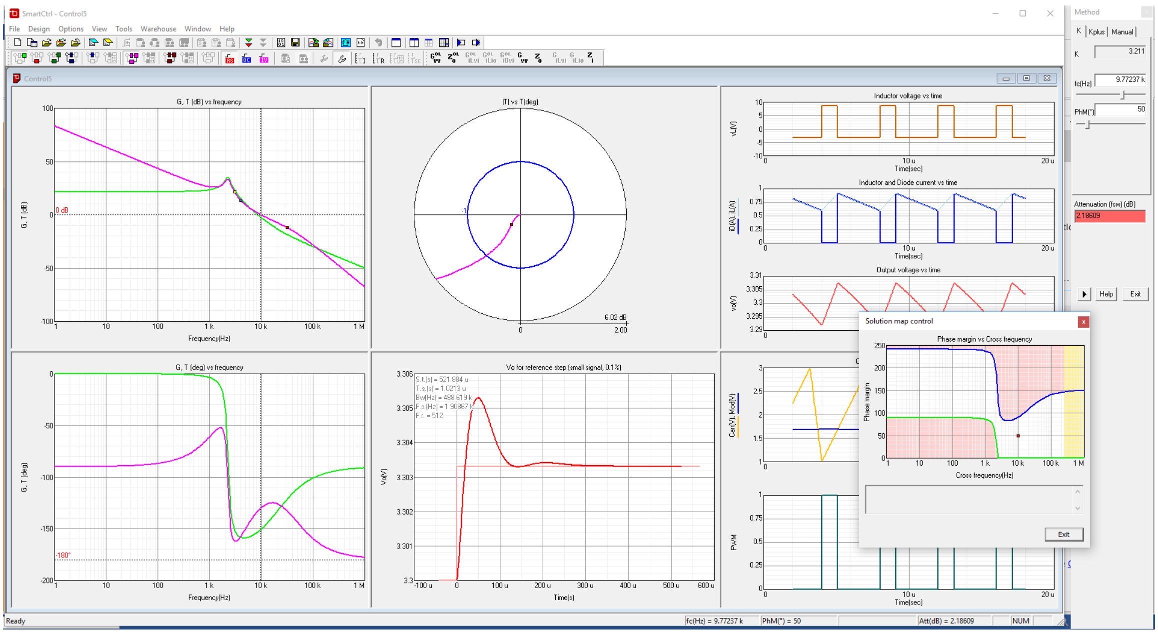


Once the system has been defined, SmartCtrl calculates the stable solution space in which all the possible combinations of crossover frequency and phase margin that lead to stable solutions are shown graphically. It is called Solutions Map. This option is available only for pre-defined compensators.

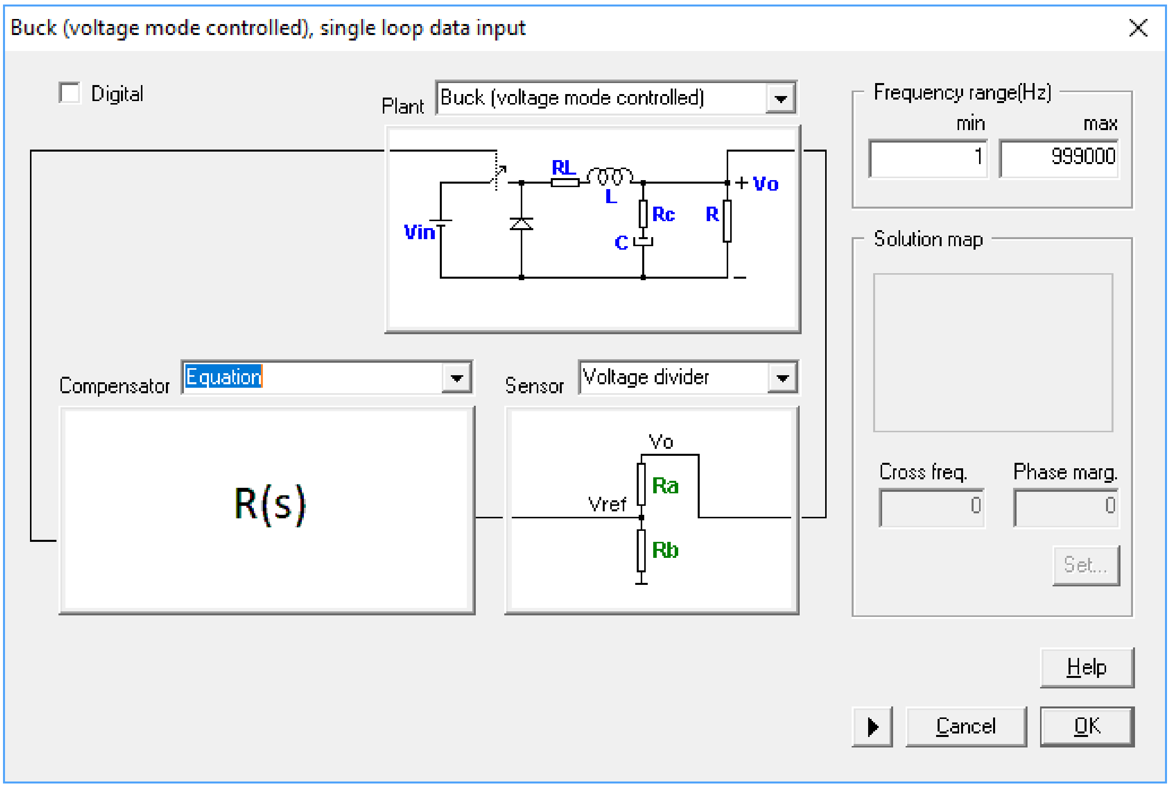
The designer is asked to select a point within the solution space to continue. To do that, just click on Set and select a point within the white zone.



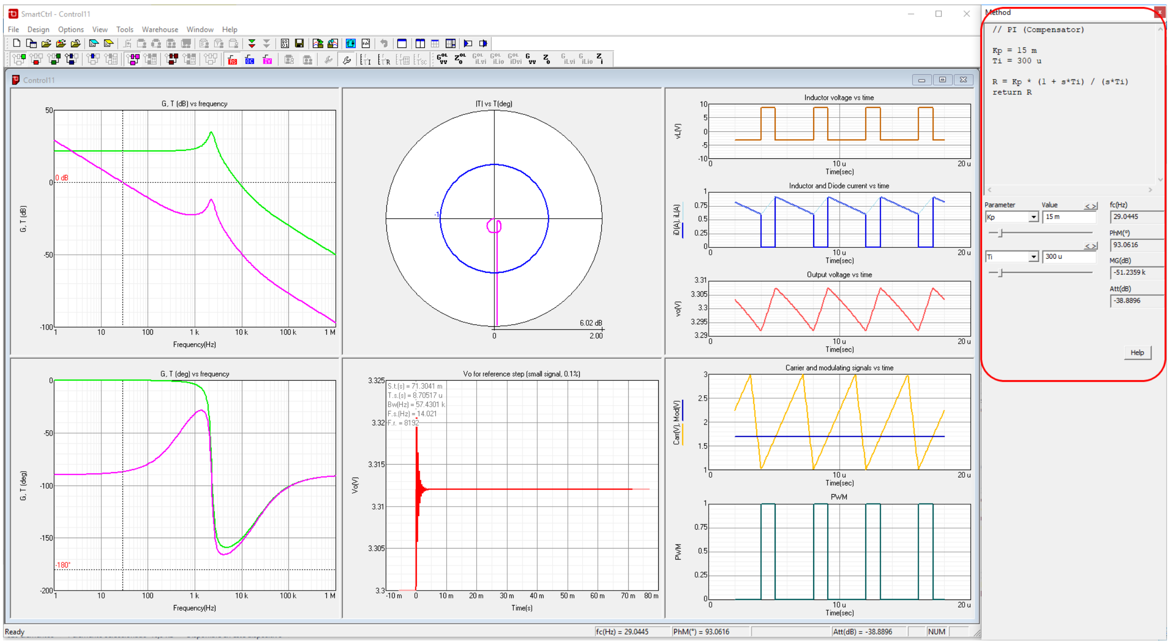
Now accept the selected point and confirm the design, the program will automatically show the performance of the system in terms of frequency response, transient response... (See Graphic and text panels window for detailed information)



When the compensator has been defined using the Equation Editor, the solutions map is not available.



Instead of using the solutions map a Method box will appear with the compensator parameter sweep to check the system response using the graphic panels.



1.4.3 DC-DC Converter - Peak Current Mode Control

Navigation: SmartCtrl > Design a predefined topology >

DC-DC Converter - Peak Current Mode Control

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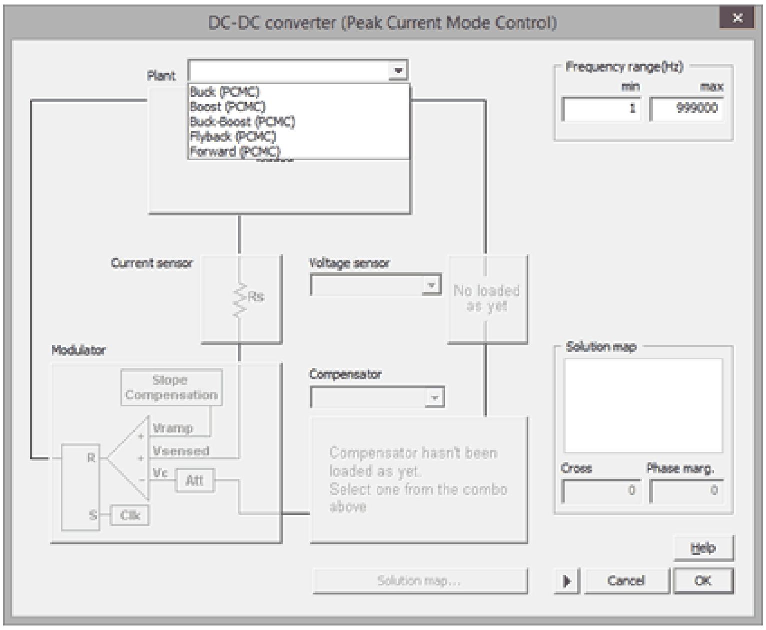
The implementation of the peak current mode control includes five different elements which are described along the following paragraphs:

•DC-DC converter (pre-defined topologies).
•Current sensor (implemented by means of a resistor).
•Modulator.
•Voltage sensor.
•Compensator.

The program will guide you through the parameterization of the different elements, which must be carried out sequentially.

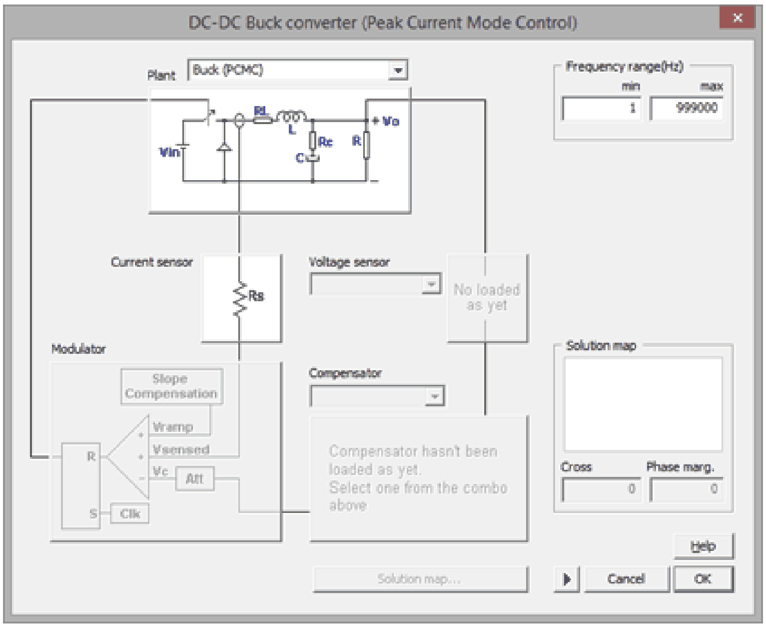
The first step to define the system is to select the plant from an existing library.



The predefined DC-DC plants are the following:

•**Buck**
•**Buck-Boost**
•**Boost**
•**Flyback**
•**Forward**

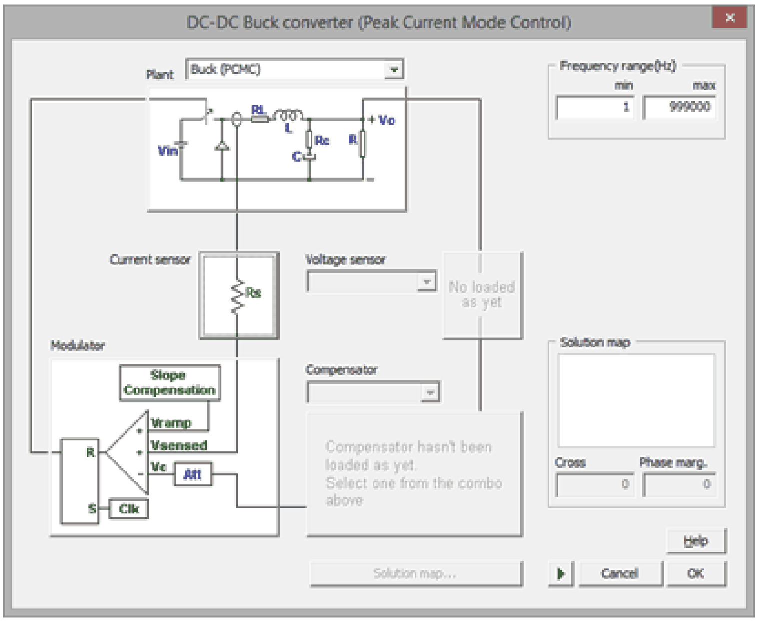
Once the plant has been selected, the value of the resistor that implements the current sensor must be set.



Current sensor available:

[Resistor]

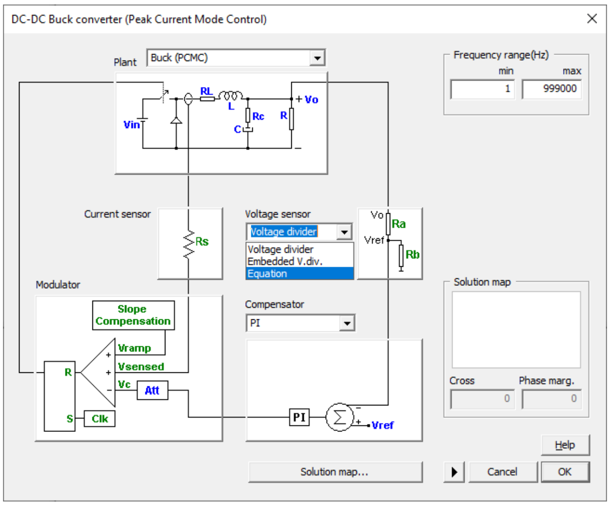
Next, the modulator must be configured.



Modulators available:

[Modulator (Peak Current Mode Control).]

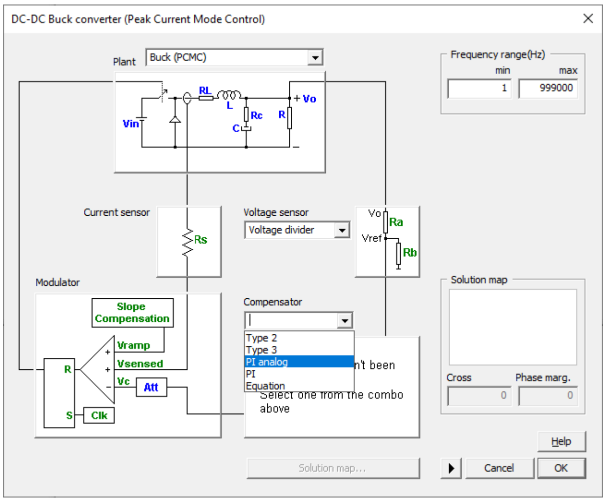
Right after the selection of the modulator, the voltage sensor must be selected.



Voltage sensor available:

[Voltage divider.](#)
[Embedded Voltage Divider](#)
•[Equation Editor (User Defined Sensor)](#)

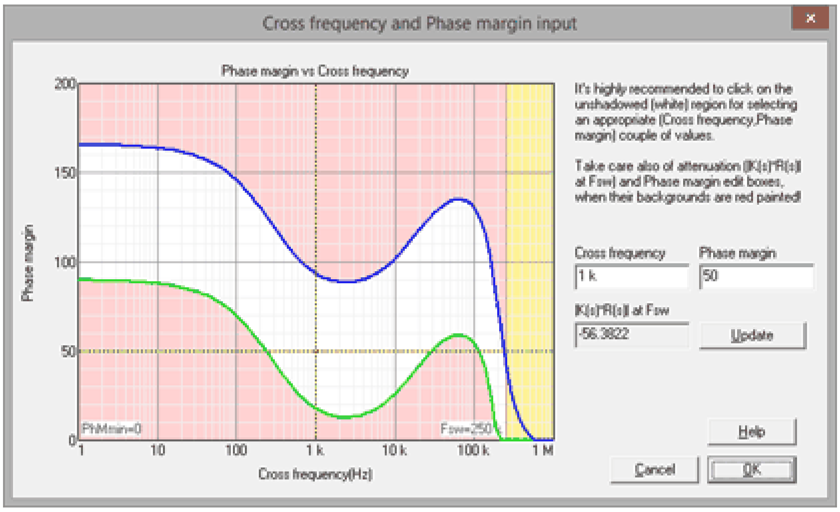
The last element that must be set is the compensator.



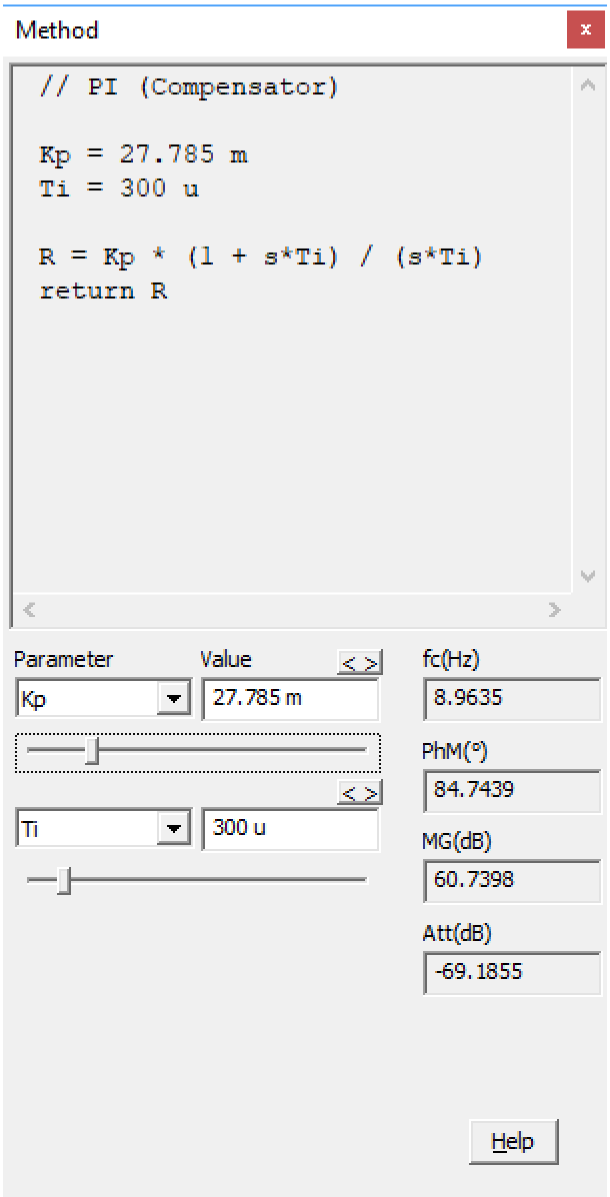
Compensator types:

•[Type 3](#)
•[Type 3 Unattenuated](#) (when selecting Embedded Voltage Divider sensor)
•[Type 2](#)
•[Type 2 unattenuated](#) (when selecting Embedded Voltage Divider sensor)
•[PI analog](#)
•[PI](#)
•[PI unattenuated](#) (when selecting Embedded Voltage Divider sensor)
•User defined compensator using [Equation Editor](#)

The user must select the control loop initial characteristics (cross frequency and phase margin), aided by the Solutions Map (only for pre-defined compensators). After that, click OK and the program will automatically show the graphics panels.



In case the user has selected a customized compensator using the equation editor, use the compensator parameter sweep available in the Method box.



1.4.4 DC-DC Converter - Average Current Control

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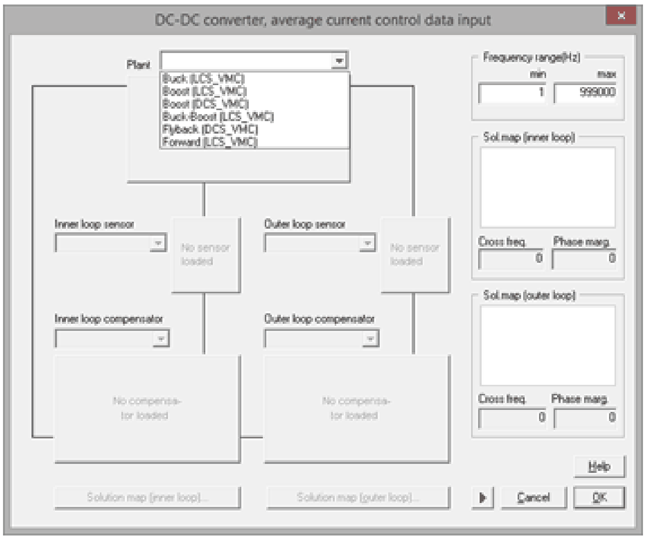
DC-DC Converter - Average Current Control

The average current control is composed by an inner current loop and an outer voltage mode loop. Same as the single loop, the double loop setup must be built sequentially. The program will guide you to build it, enabling the following step and keeping everything else disabled.

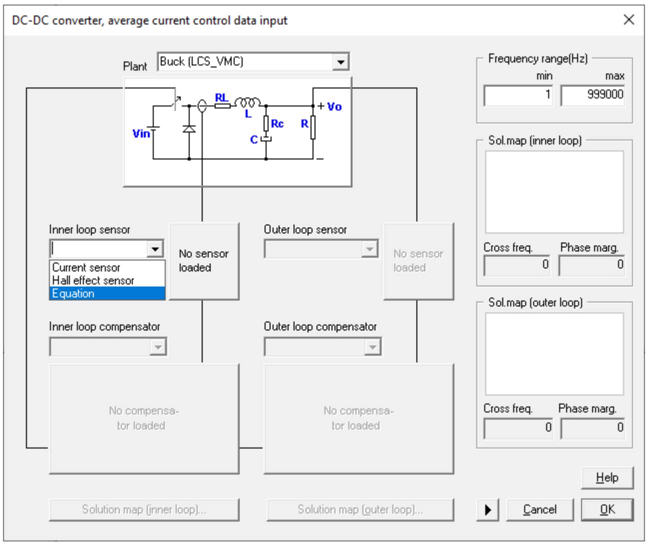
In all the available plants, the outer loop is a voltage mode control (VMC), while the inner loop is a current controlled one. Depending on the selected plant, the current is sensed either on the inductance (LCS) or on the diode (DCS). The DC-DC plant must be selected among the following list.



The predefined DC-DC plants are the following:

- **Buck** (LCD-VMC)
- **Buck-Boost** (LCS-VMC)
- **Boost** (LCS-VMC)
- **Boost (DCS-VMC)**
- **Flyback** (DCS-VMC)
- **Forward** (LCS-VMC)

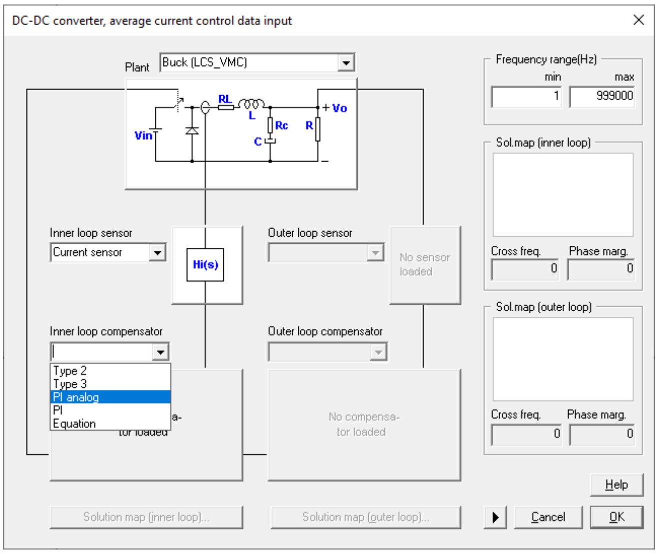
Next, the inner control loop will be configured. This is, the current sensor and the regulator type must be selected.



The available current sensors are the following:

- **Current Sensor**
- **Hall Effect Sensor**
- **Equation Editor (User Defined Sensor)**

Finally, the inner loop compensator is selected.

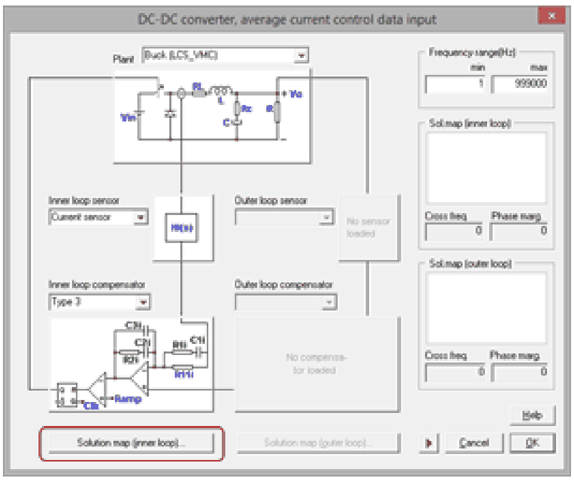


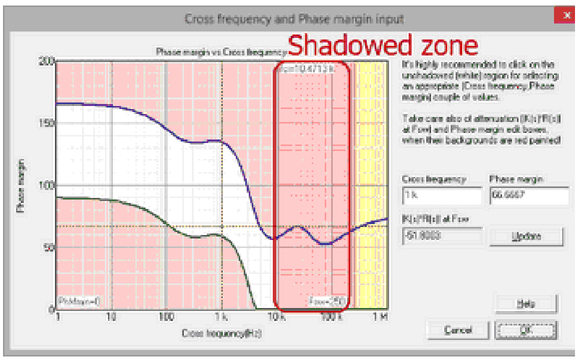
Compensator types:

- •[Type 3]
- •[Type 2]
- •[PI analog]
- •[PI]
- •[Single Pole]
- •User defined compensator using [Equation Editor]

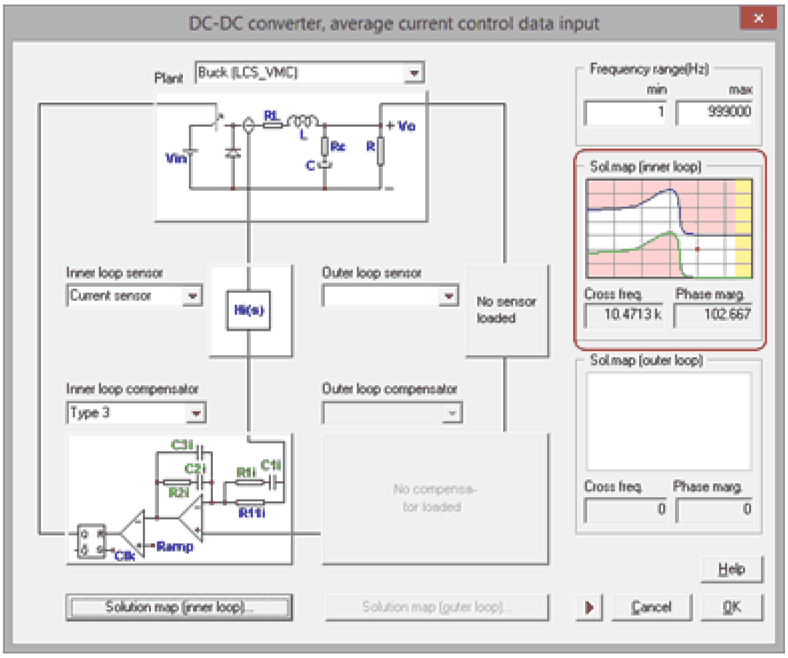
Once all the inner loop transfer functions have been defined, The cross frequency and the phase margin must be selected. Under the name of Solution Map, SmartCtrl provides the stable solution space in which all the possible combinations of cut off frequency and phase margin that lead to stable solutions are shown graphically. Just clicking on the "Solutions map (inner loop)" button the solution map corresponding to the inner loop is displayed.
The designer is asked to select the crossover frequency and the phase margin just by clicking within the white zone to continue.

This option is only available for pre-defined compensators.

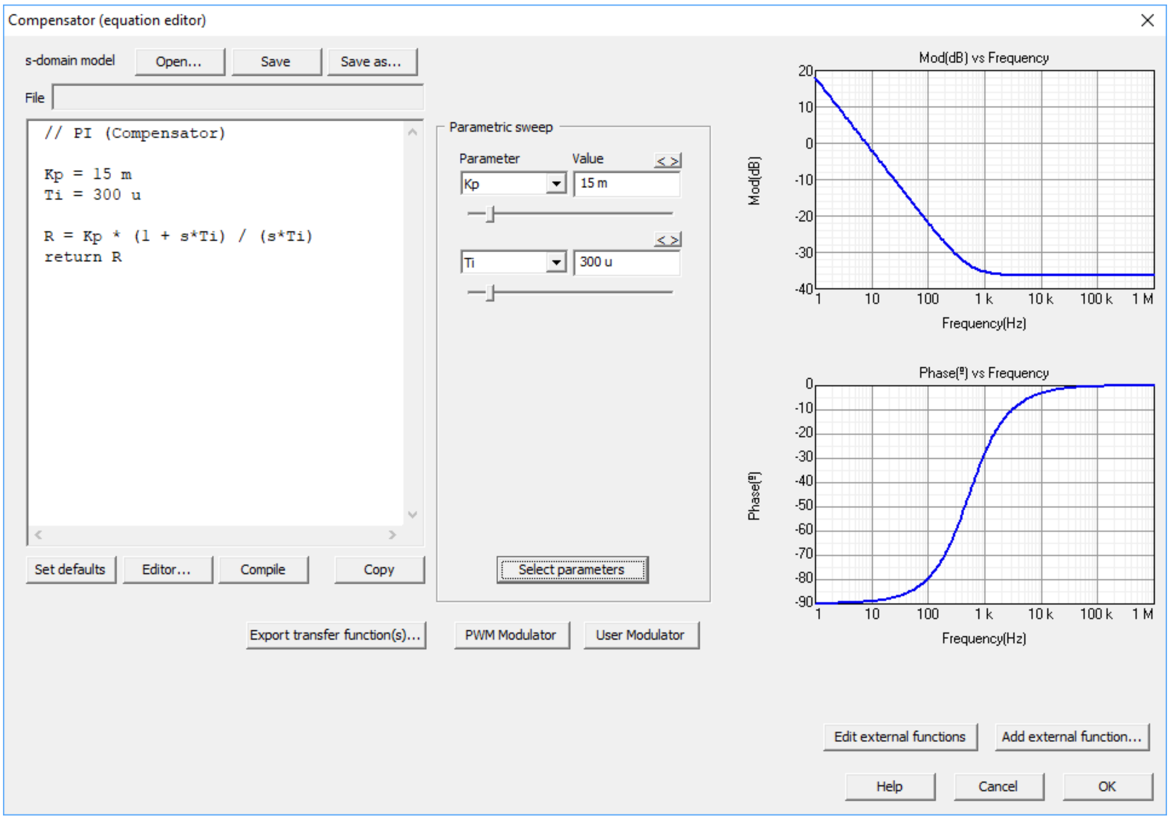




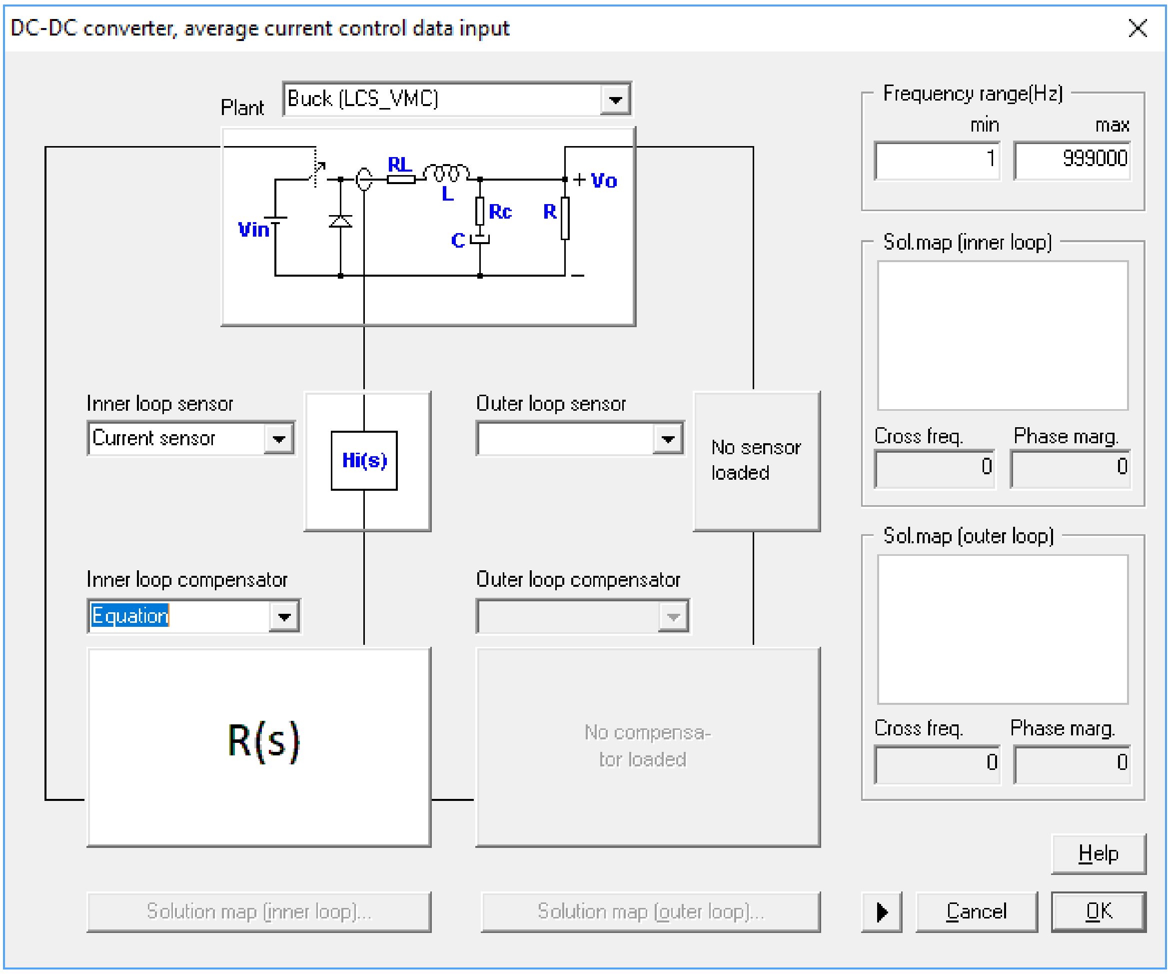
Once the cross frequency and the phase margin have been selected, the solution map will be shown on the right of the side of the DC-DC average current control input data window. If, at any time, the two aforementioned parameters need to be changed, just click on the shown solution map. (See below figure)



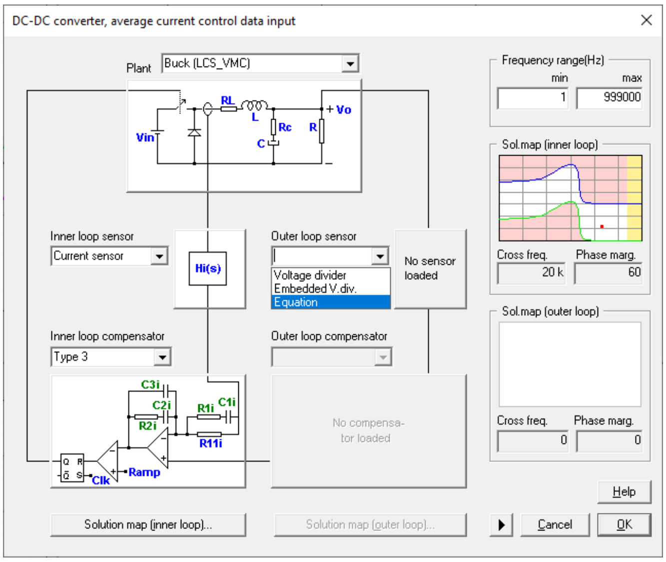
In case the user select the option **Equation Editor** for the inner loop compensator this window allows to open an existing one or to define with the editor the compensator transfer function.



In this case the Solutions Map is not available because the user is defining the regulator parameters, once the design is complete these parameters can be easily modified to check the solution stability in the graphic panels.



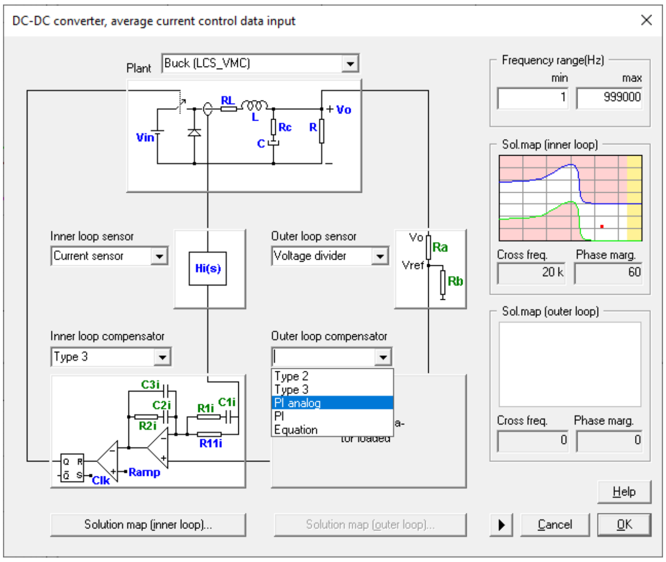
Now, the outer loop can be defined. First, the voltage sensor must be selected.



The different sensors available are the following:

- •Voltage Divider
- •Embedded Voltage Divider
- •Equation Editor (User Defined Sensor)

Next, the outer loop compensator must be selected.

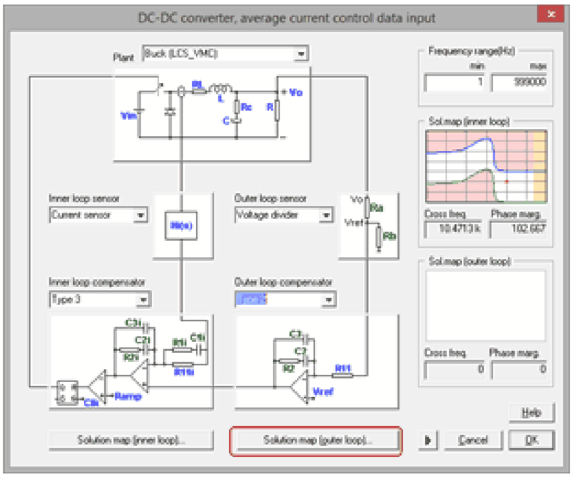


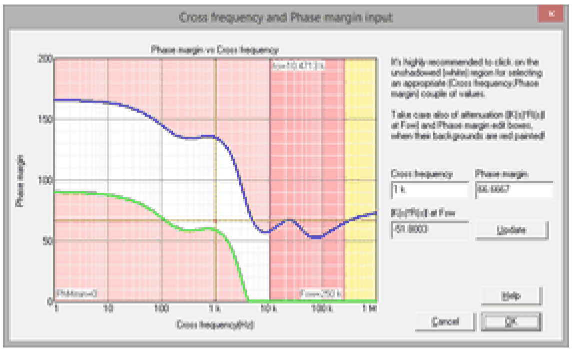
Compensator types:

- •Type 3
- •Type 3 Unattenuated
- •Type 2
- •Type 2 unattenuated
- •PI analog
- •PI
- •PI unattenuated
- •Single Pole
- •Single Pole unattenuated
- •Customer defined compensator using Equation Editor

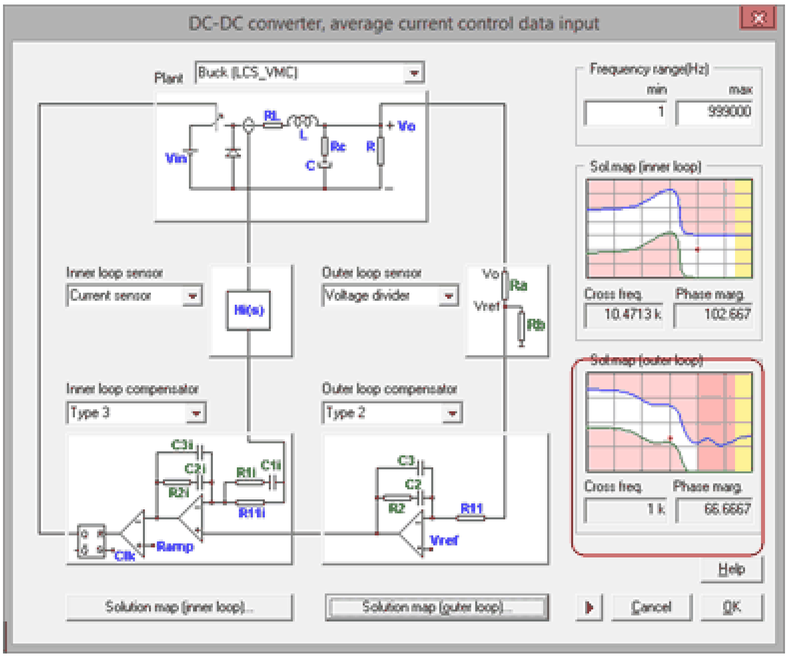
As well as in the case of the inner loop, the cross frequency and the phase margin must be selected. Also in this case, the solution map is available to help the selection of an stable solution. Press the "Solution map (outer loop)" button and the solution map will be displayed. Then select a point just by clicking within the white area.

It should be remarked that, due to stability constraints, the crossover frequency of the outer loop cannot be greater than the crossover frequency of the inner loop. In order to prevent the selection of an outer loop fc greater than the inner loop one, a pink shadowed area has been included in the solutions map of the outer loop.



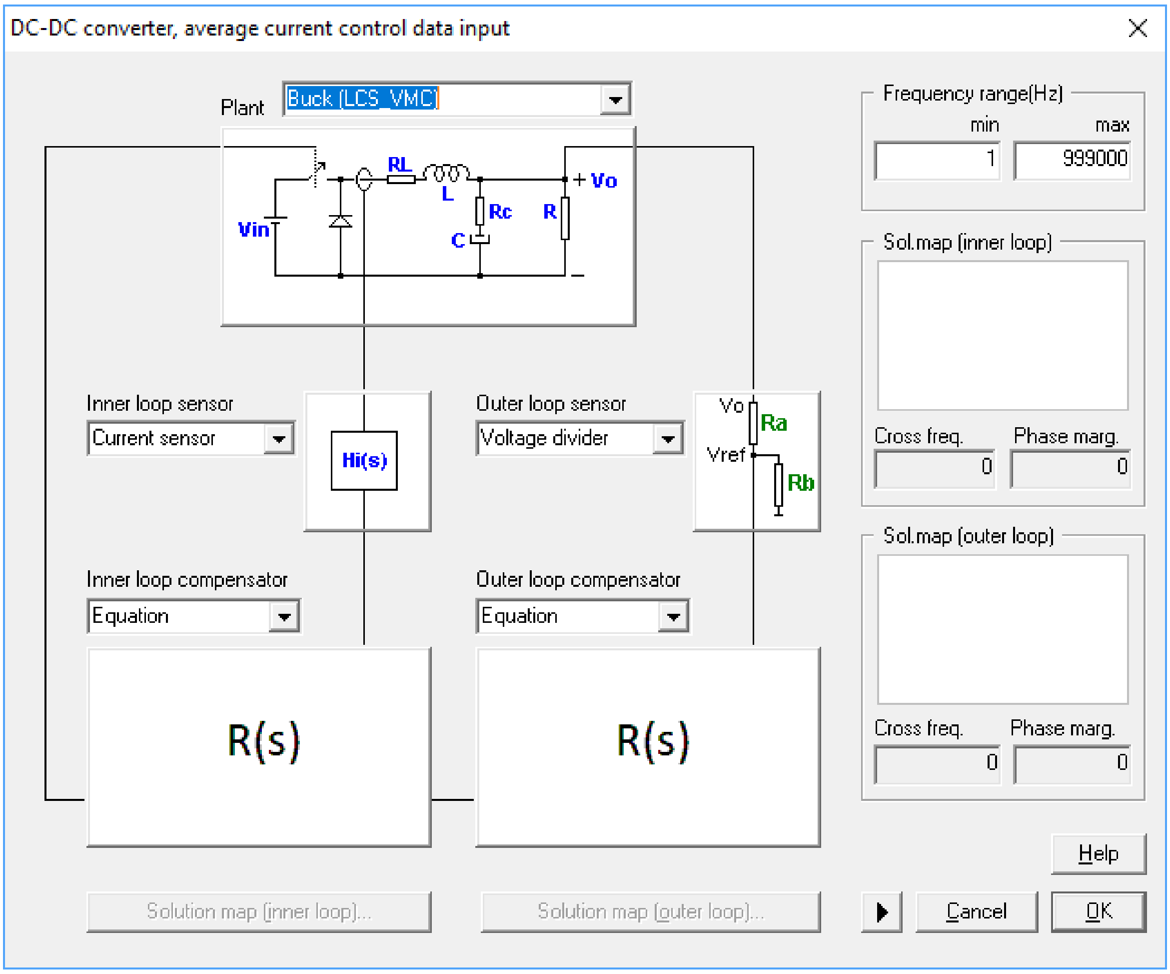


Once the crossover frequency and the phase margin have been selected, the solution map will be shown on the right of the side of the DC-DC average current control input data window. If, at any time, the two aforementioned parameters need to be changed, just click on the shown solution map. (See next figure)

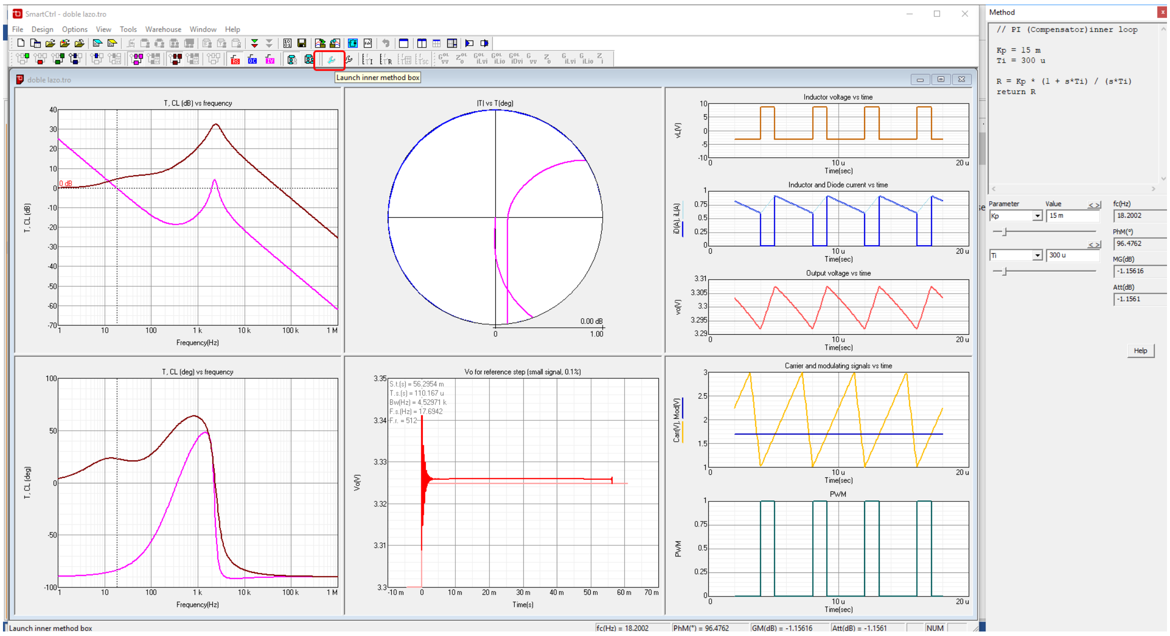


Now accept the selected configuration and confirm the design, the program will automatically show the performance of the system in terms of frequency response, transient response... (See Graphic and text panels window for detailed information)

In case the user selected for both loops the customized compensator using the Equation Editor, once accepted the design, the compensator parameters sweep in the Method box allows the user to check the design stability.



Using the icon  "Launch inner method box" in the toolbar, the user can modify the inner loop compensator parameters.



Using the icon  "Launch outer method box" in the toolbar, the user can modify the outer loop compensator parameters.

1.4.5 Power factor corrector

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Power factor corrector

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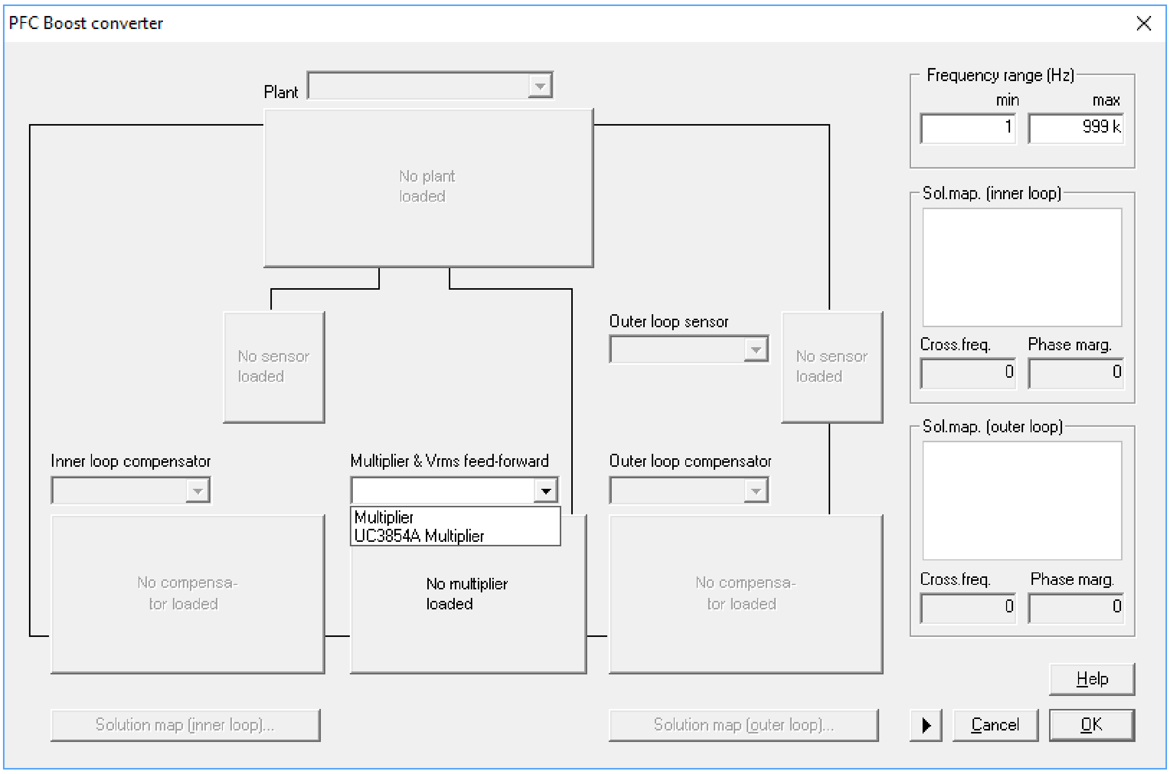
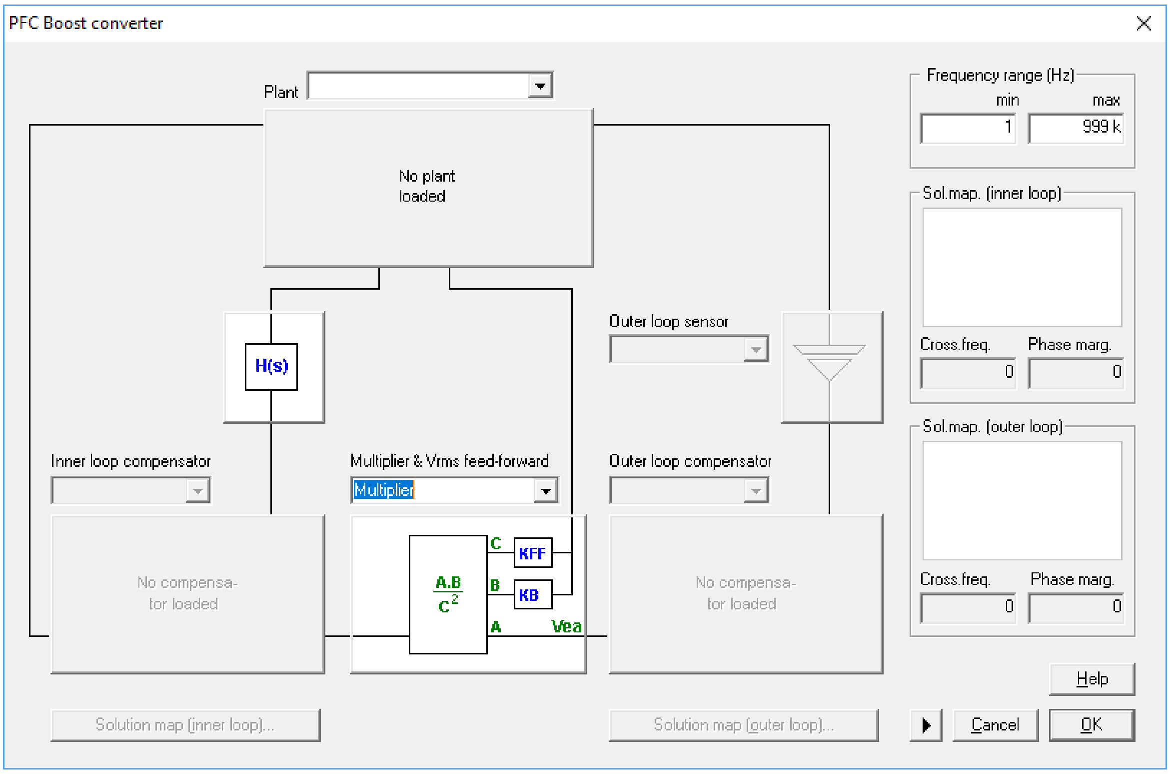
The power factor corrector based on a boost topology has a double control loop, formed by an inner (inductance) current loop and an outer voltage mode loop. The double loop setup must be built sequentially. The program will guide you to build it, enabling the following step and keeping everything else disabled.

The first step chooses between the two types of multiplier and Vrms feed-forward:
•Multiplier: A generic, parametrizable multiplier, with a Hall Effect current sensor.
•UC3854A Multiplier: UC3854A Multiplier: An UC3854A commercial multiplier, with its external resistors to be chosen.

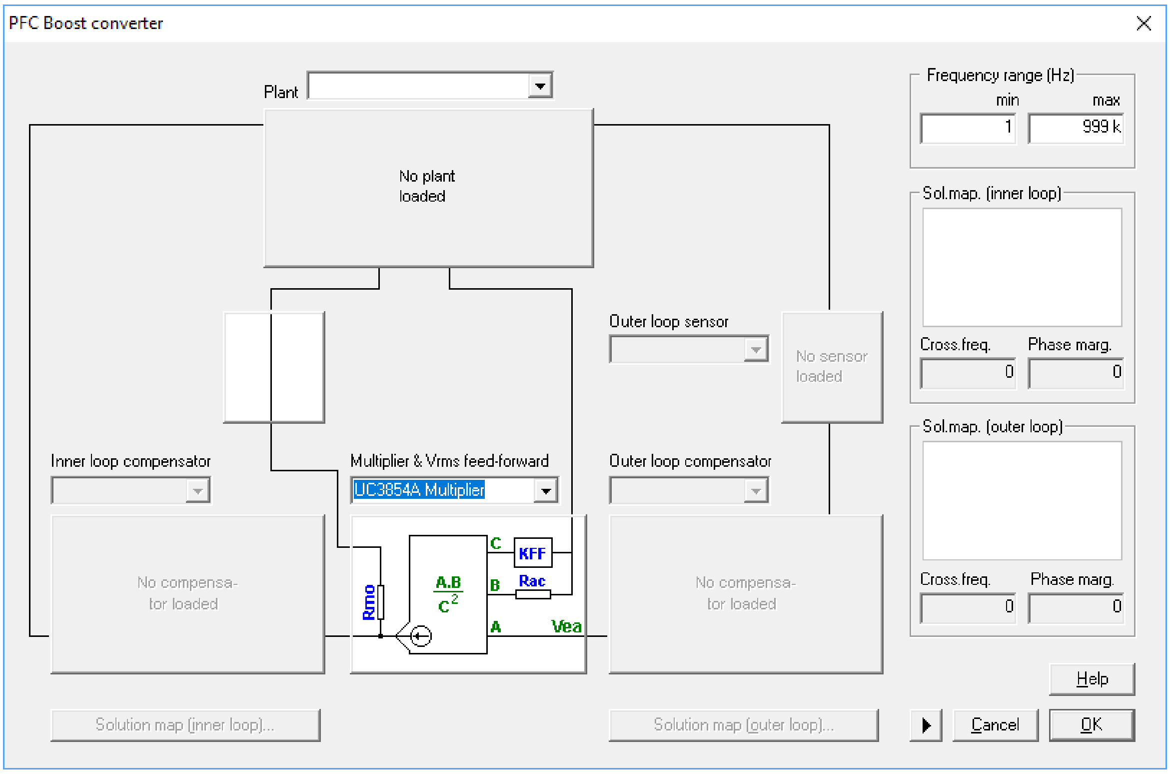


Depending on the first choice, there are two different options to generate the power factor corrector.

If a Generic Multiplier is selected, the current is sensed by the Hall Effect sensor H(s).

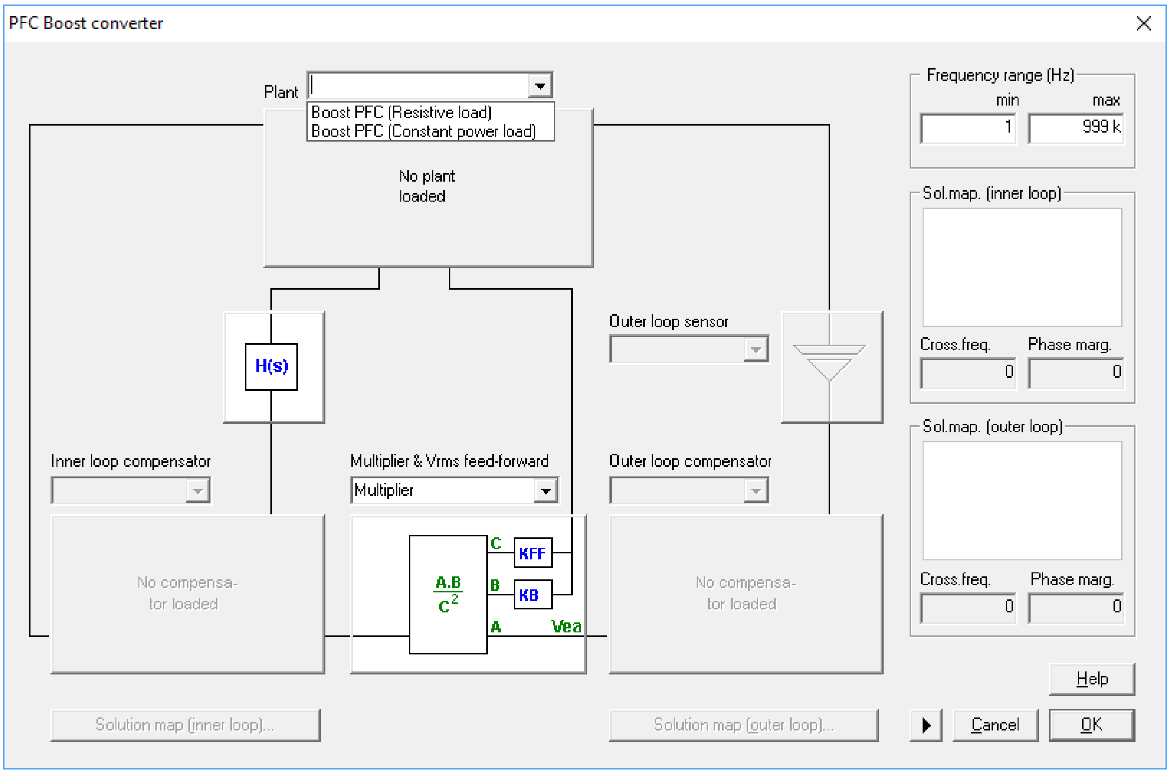


Otherwise, if the selection is UC3854A multiplier, the current sensor is implemented by means of the resistor Rs.

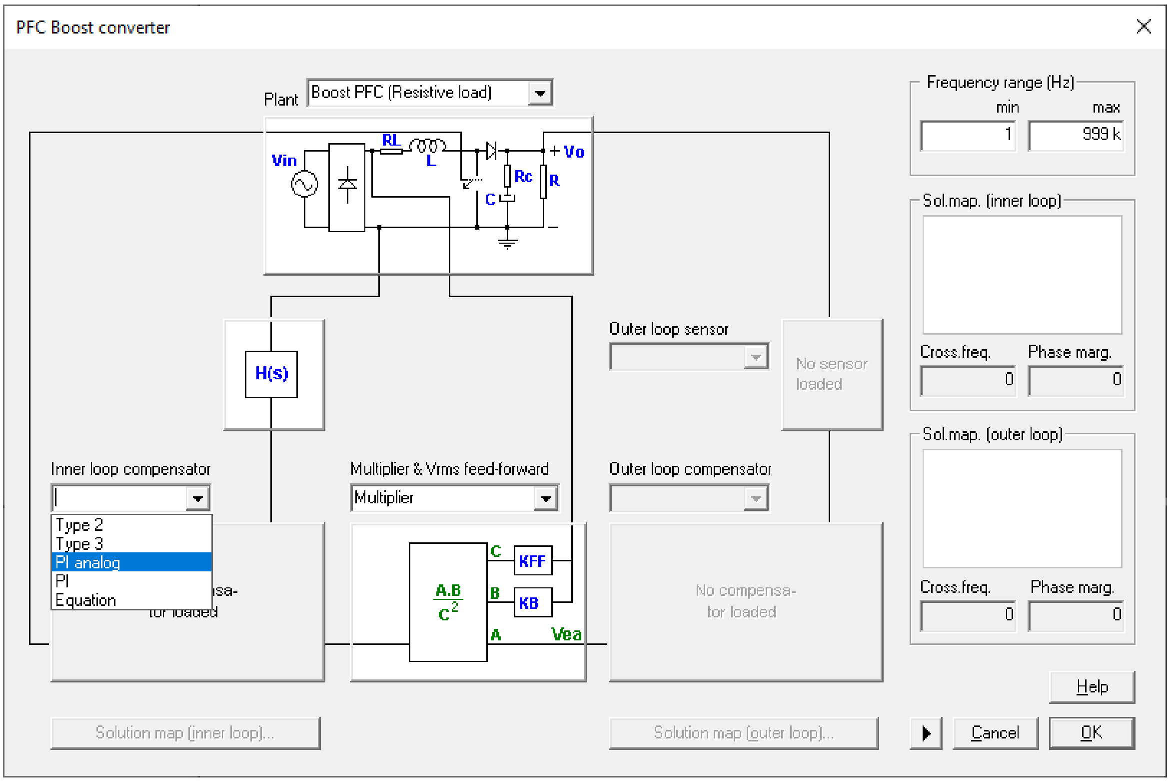


Next, the plant must be selected. The predefined plants are the following:

•**Boost PFC**(Resistive load)
•**Boost PFC** (Constant power load)



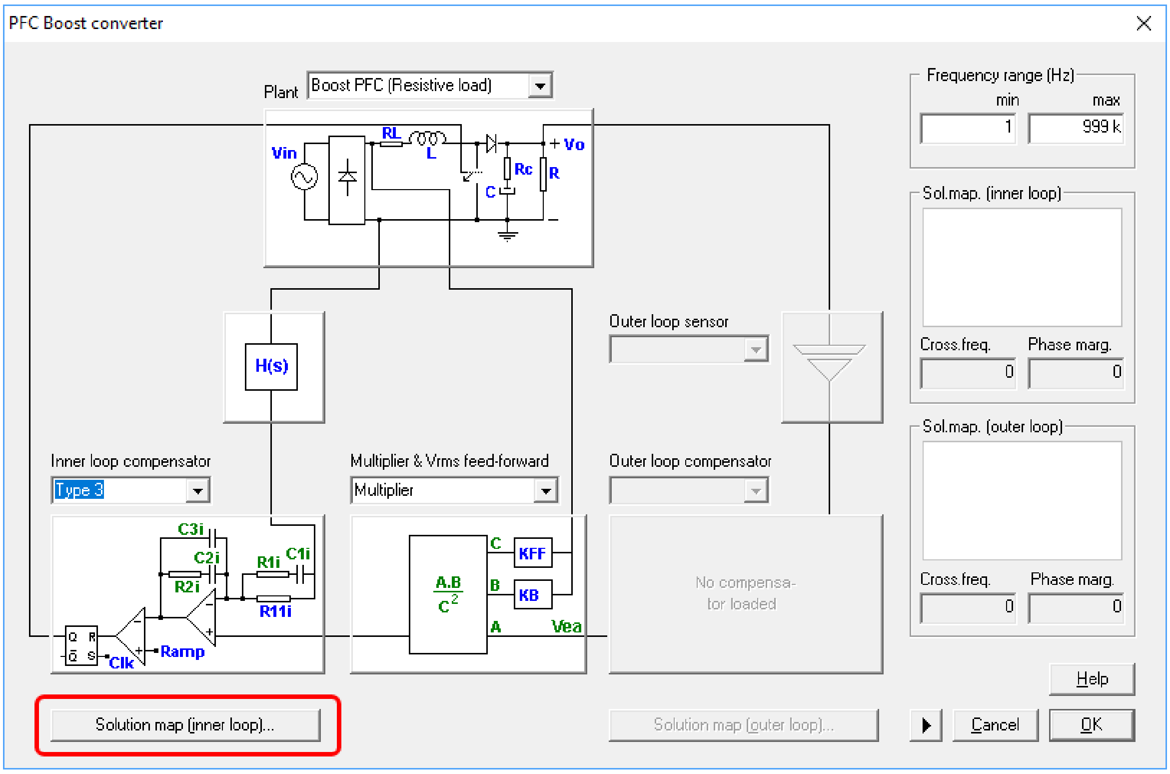
Next, the inner control loop will be configured: since the current sensor has been already set, it is necessary to select the inner loop compensator.



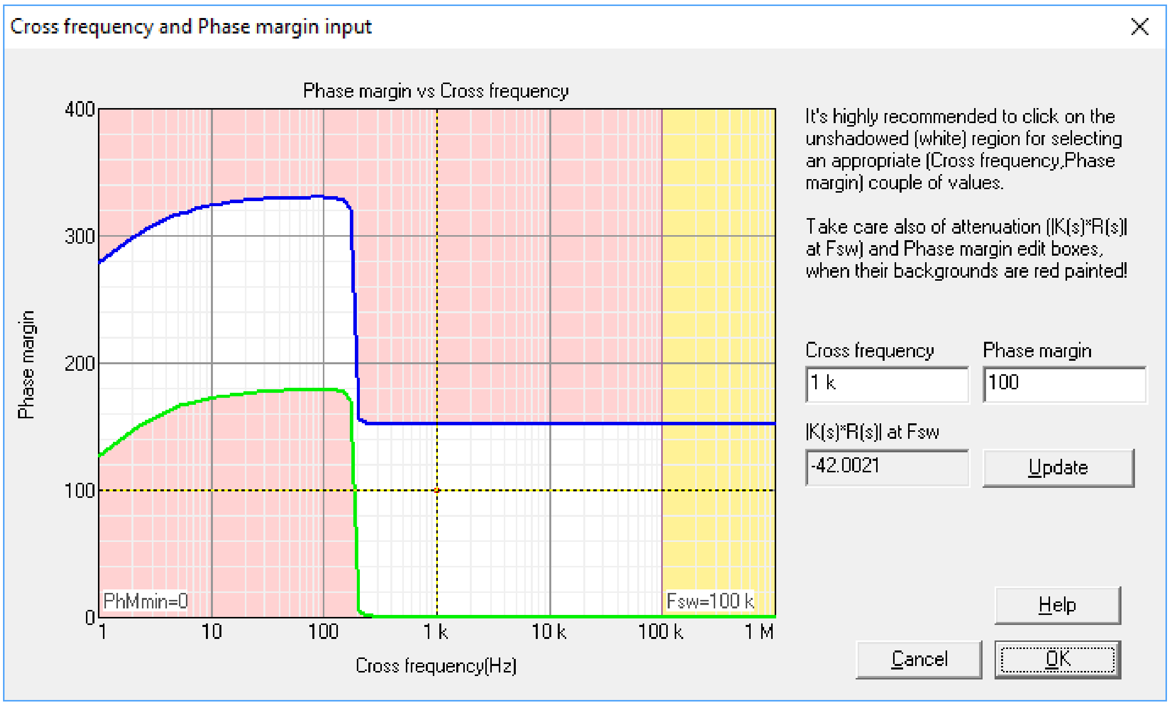
Compensator types:

•**Type 3** (It is only available for Multiplier option)
•**Type 2**
•**PI**
•**PI analog**
•**User defined compensator: Equation Editor**

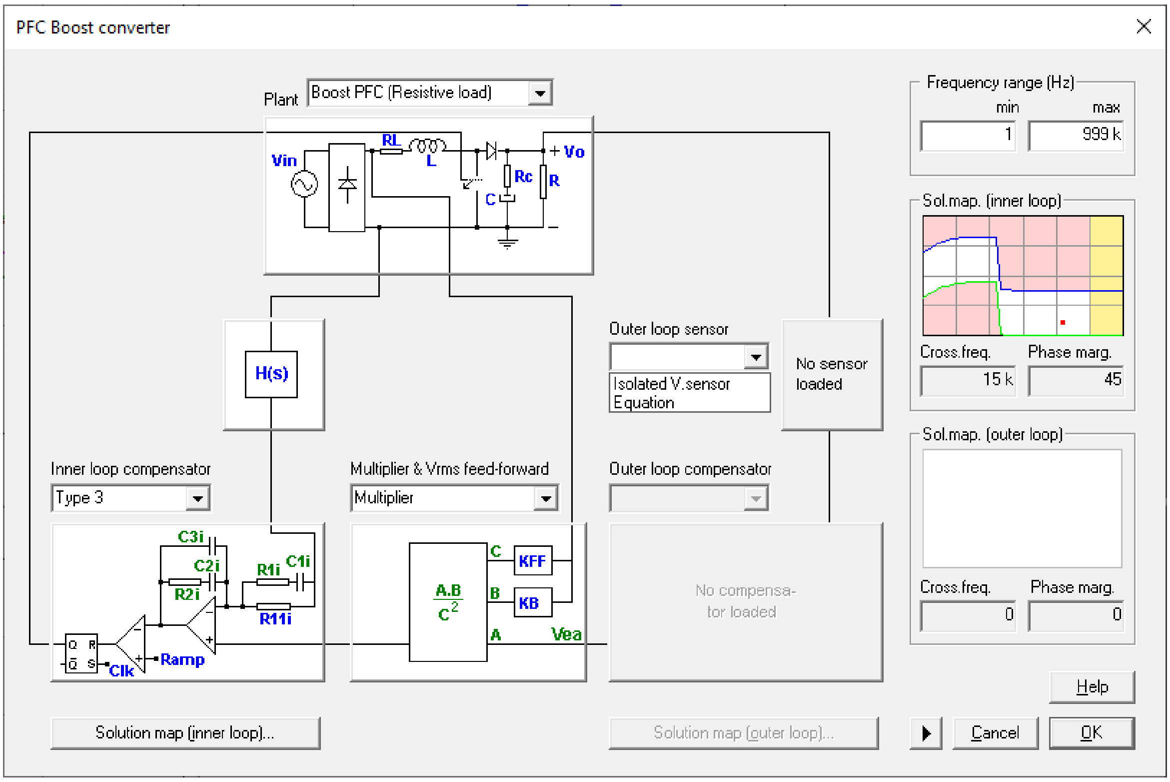
Once all the **inner loop** transfer functions have been defined, the crossover frequency and the phase margin must be selected. Under the name of Solution Map (only for predefined compensators), SmartCtrl provides the stable solution space in which all the possible combinations of crossover frequency and phase margin that lead to stable solutions are shown graphically. Just clicking on the "Solutions map (inner loop)" button the solution map corresponding to the inner loop is displayed.



The designer is asked to select the crossover frequency and the phase margin just by clicking within the white zone to continue.



Once the crossover frequency and the phase margin have been selected, the solution map will be shown on the right side of the PFC Boost converter input data window. If, at any time, the two aforementioned parameters need to be changed, just click on the inner loop solution map. (See next figure).

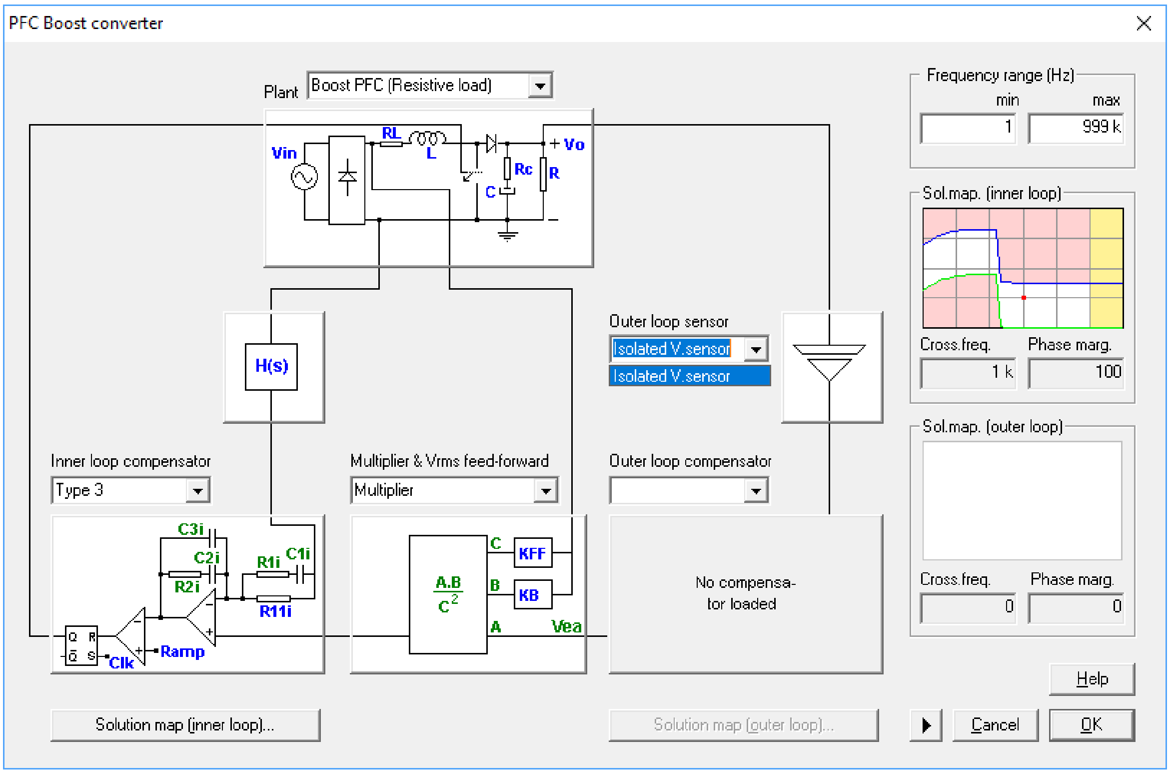


Now, the **outer loop** can be defined. First, the voltage sensor must be selected.

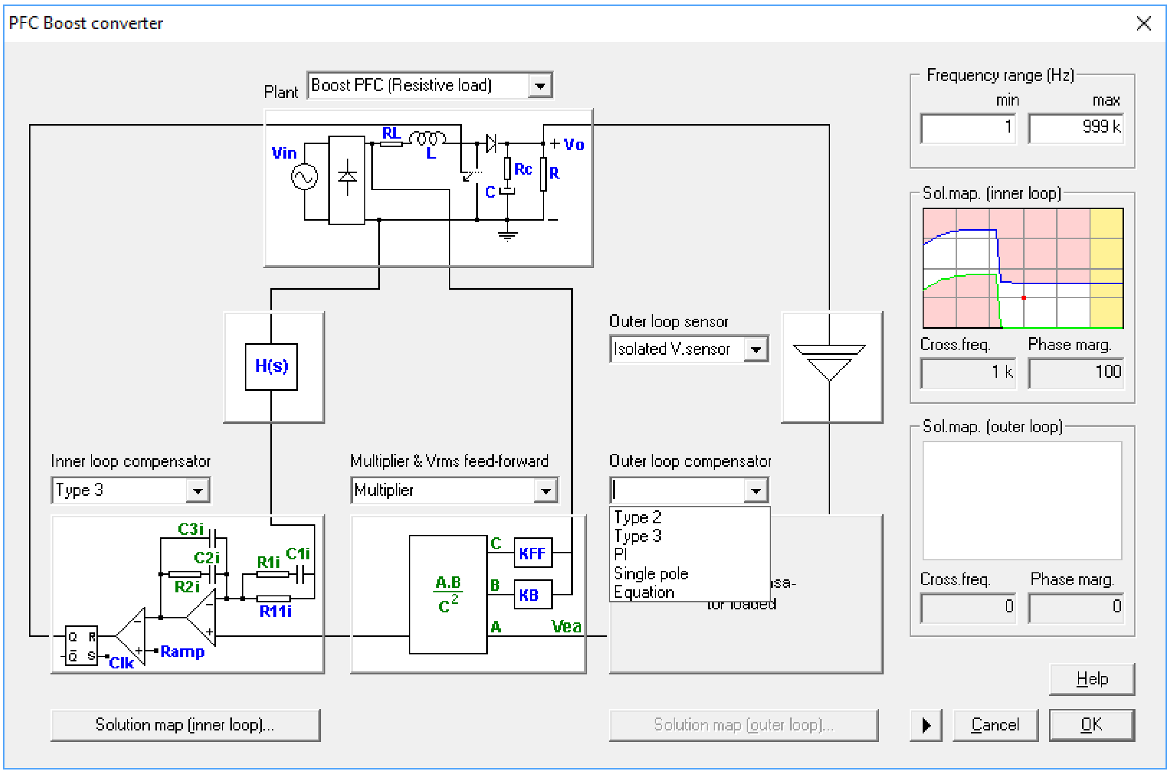
The voltage sensors available are the following:

For Multiplier option:
•**Isolated V sensor**
•**Equation Editor (User Defined Sensor)**

For UC3854A Multiplier option:
•**Voltage Divider**
•**Embedded Voltage Divider**
•**Equation Editor (User Defined Sensor)**



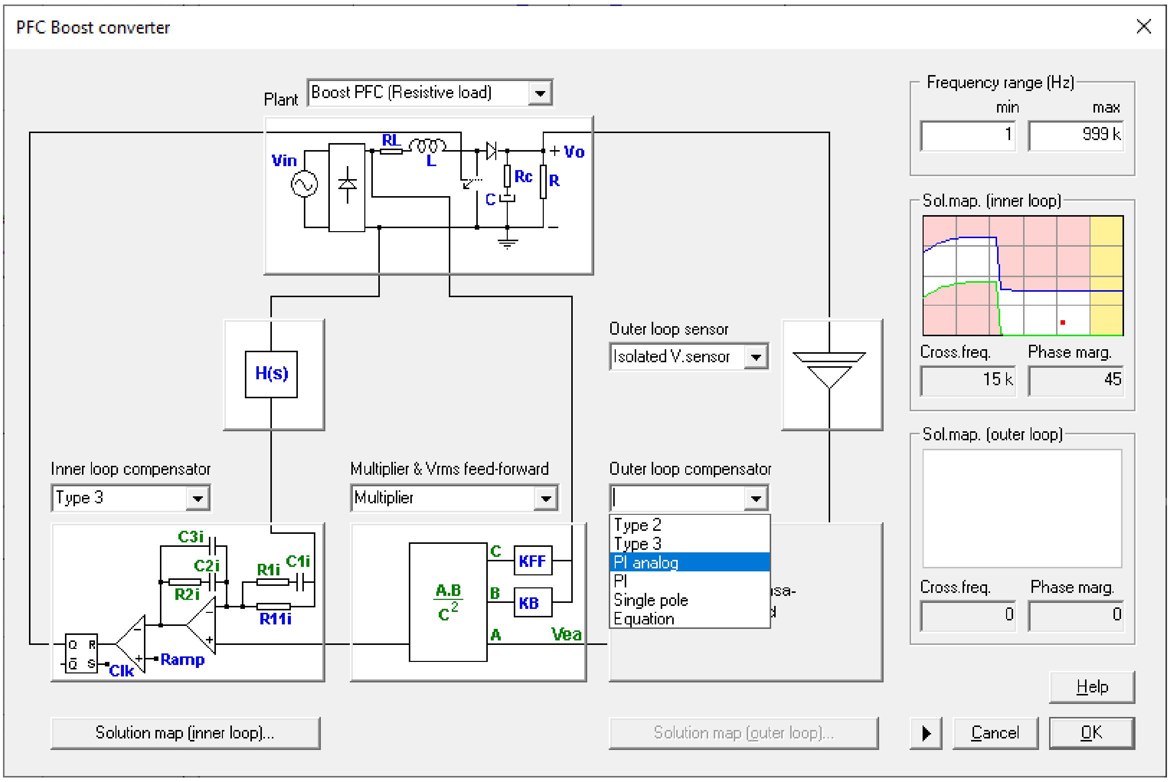
Next, the outer loop compensator must be selected.



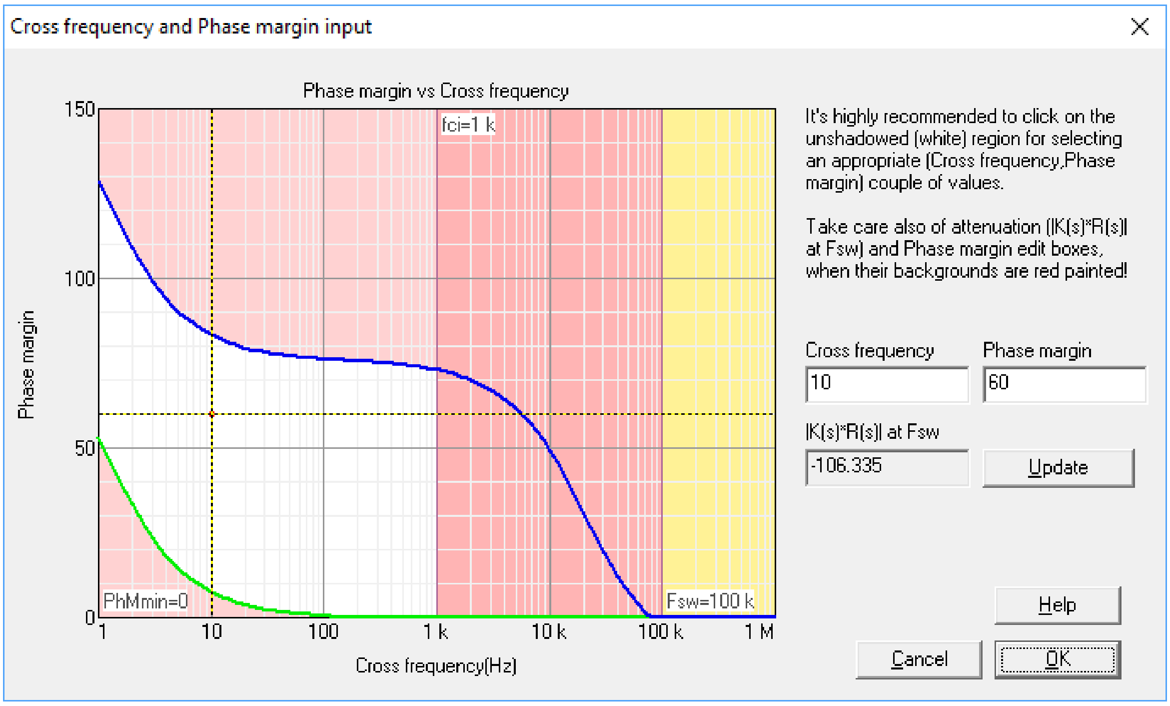
Outer Loop compensator types depending on the sensor previously selected:

For multiplier option:	For UC3854 multiplier option:		
	For Voltage Divider sensor:	**For Embedded Voltage Divider sensor:**	**For user defined sensor (Equation Editor):**
• Type 3 • Type 2 • PI • PI analog • Single Pole • User defined using Equation Editor	• Type 2 • PI • PI analog • Single Pole • User defined using Equation Editor	• Type 2 unattenuated • PI unattenuated • Single Pole unattenuated • User defined using Equation Editor	• Type 2 • Type 3 • PI • PI analog • Single Pole • User defined using Equation Editor

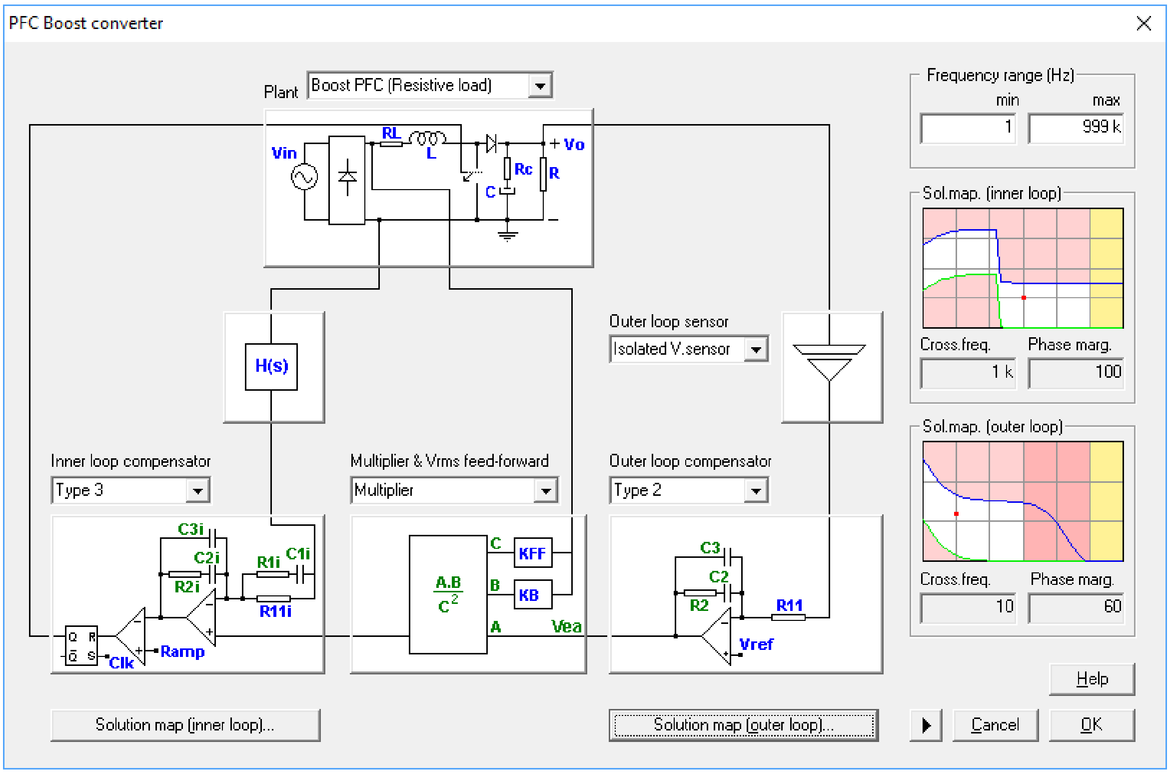
As well as in the case of the inner loop, the cross frequency and the phase margin must be selected. Also in this case, the solution map (only for predefined compensators) is available to help the selection of a stable solution.
Press the "Solution map (outer loop)" button and the solution map will be displayed. Then select a point just by clicking within the white area.



It should be remarked that, due to stability constraints, the crossover frequency of the outer loop cannot be greater than the crossover frequency of the inner loop. In order to prevent the selection of an outer loop fc greater than the inner loop one, a pink shadowed area has been included in the solutions map of the outer loop.



Once the crossover frequency and the phase margin have been selected, the solution map will be shown on the right side of the DC-DC average current control input data window. If, at any time, the two aforementioned parameters need to be changed, just click on the outer loop solution map. (See next figure)



Once everything is set, accept the selected configuration and confirm the design, the program will automatically show the performance of the system in terms of frequency response, line current shape... (See Graphic panel window for detailed information).

Once the design has been generated, two possible warning messages can appear in the solution map window:

· In the case of a single pole compensator in the outer loop, which is a typical compensator for power factor correctors, the gain at low frequency may be low. A warning appears when the estimated Vo (shown in the method panel) differs from the specified one in more than 10%.In these cases, a compensator with a higher gain at low frequency is recommended.

· The line current waveform is calculated assuming that the current loop follows perfectly well the reference generated by the outer loop. However, in some occasions there is a zero-cross distortion and the actual line current would differ from the one represented. In these cases, a warning message appears. The cross-frequency of the inner loop compensator should be increased to minimize this problem.

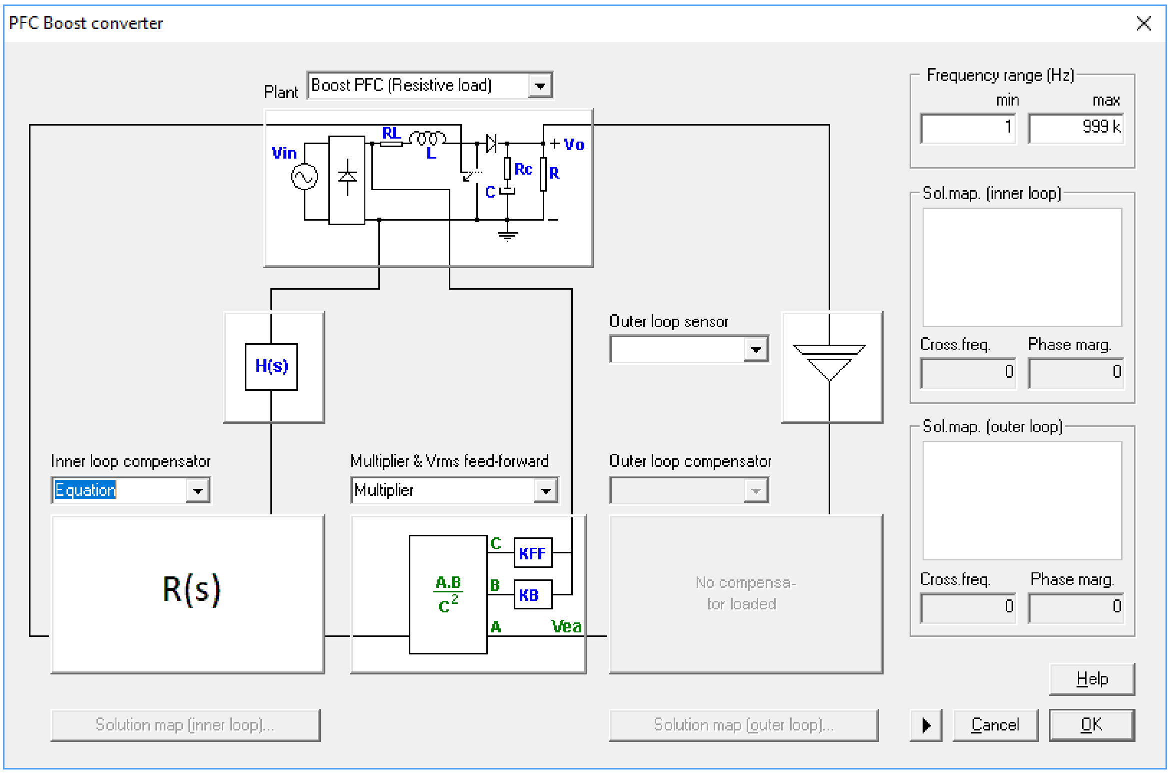
In the method panel, additional information is provided both for the inner loop and the outer loop:

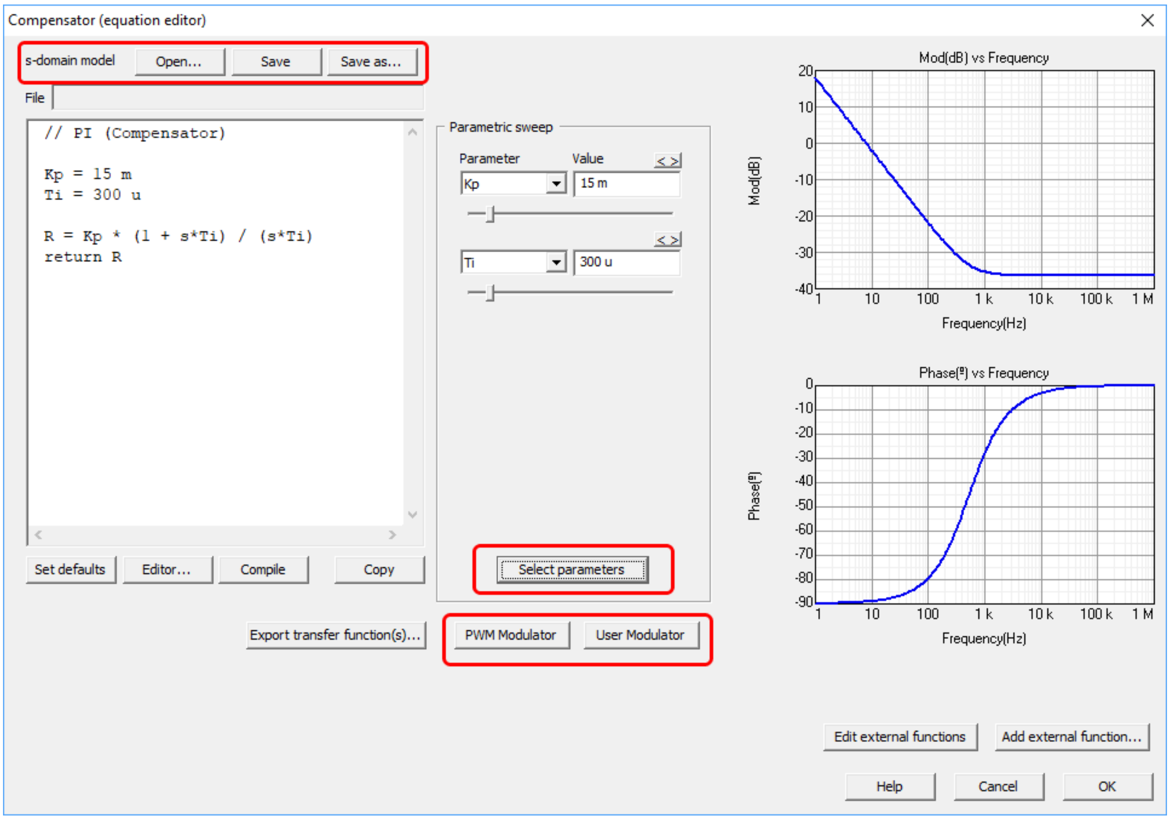
- Attenuation (fsw)(dB). This is the attenuation in dB achieved by the combination of the sensor and the compensator at the switching frequency. Since the reference for the inner loop is generated by the outer one, it must be enough to avoid making the system unstable.

•Attenuation (2fl)(dB) . This is the attenuation in dB achieved by the combination of the sensor and the compensator at twice the line frequency (100 Hz or 120 Hz). Since the reference for the inner loop is generated by the outer one, it must be enough to avoid making the system unstable.

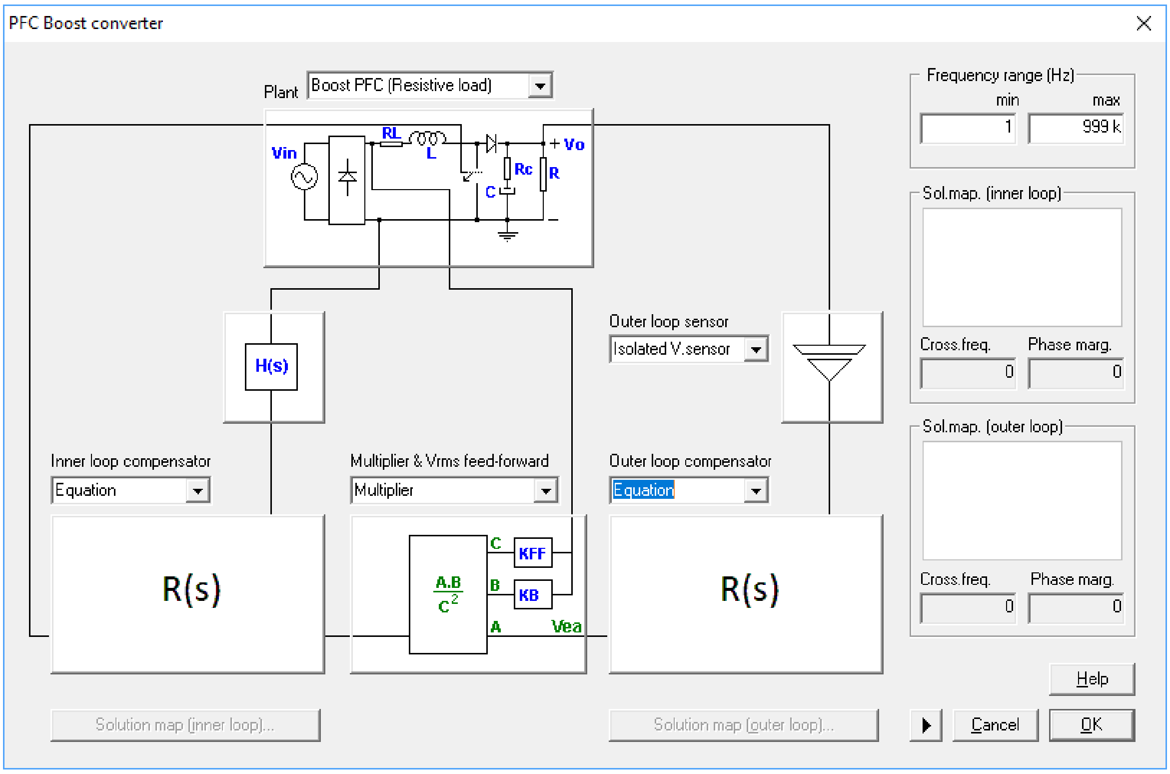
•Estimated Vo (V). This is the estimated output voltage of the converter. This parameter is important because, if the frequency gain of the open loop transfer function is not high enough, there will be a steady-state error and the estimated output voltage can be different from the specified output voltage. As mentioned above, if the estimated Vo (shown in the method panel) differs from the specified one in more than 10%, a warning will be displayed.

In case the user selects a **customer defined compensator** using the Equation Editor, just follow the steps explained in Compensator (Equation Editor)



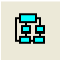


This option can be selected for both, inner and outer loops.



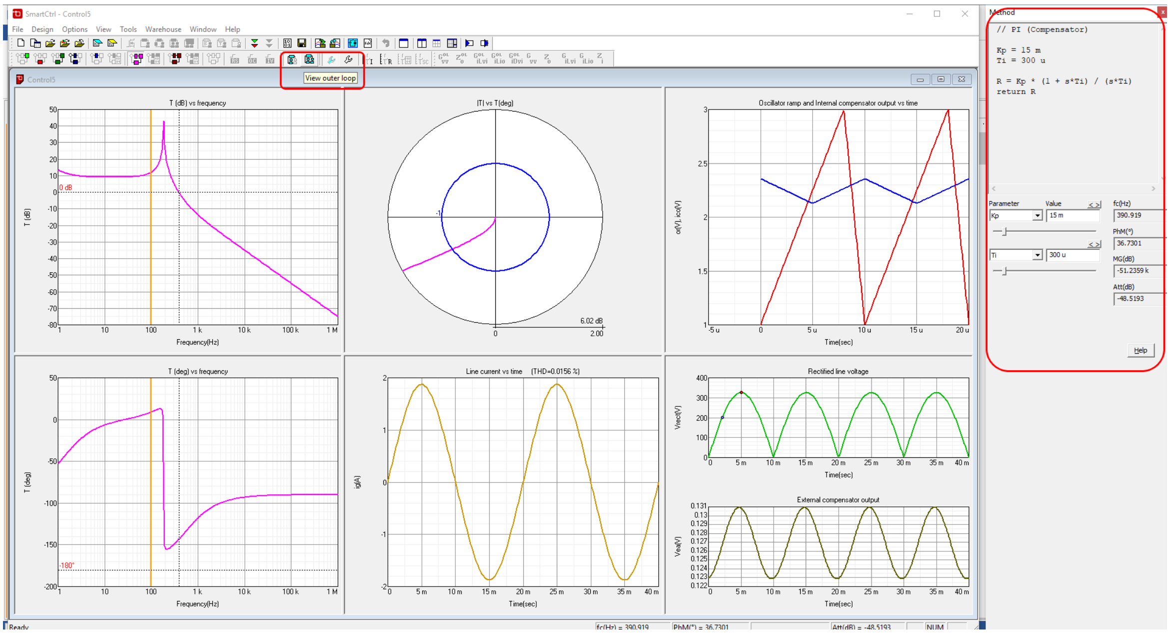
For customer defined compensator the solutions map will not be available; use the buttons in the view toolbar to change the graphic view between inner and outer loop and to adjust the inner and outer loop compensator values in the method Box.

 View inner loop

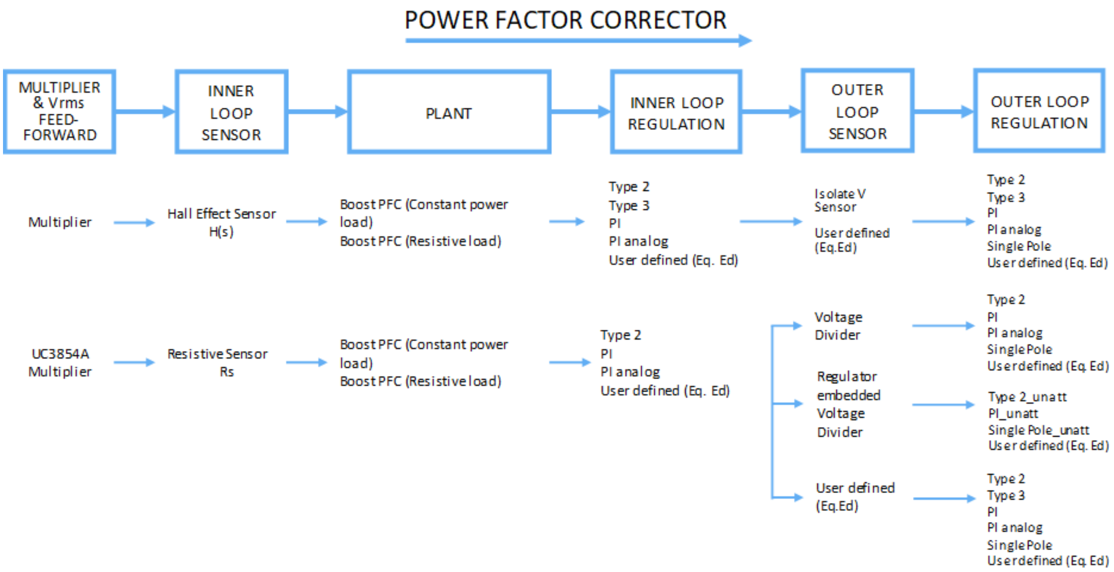
 View outer loop

 Launch inner method box / Display inner loop results

 Enables or disables the display of the compensator calculation method toolbox. Launch outer method box or Method box / Display outer loop results



Finally, the flowchart to generate the types of the power factor is the following:



1.4.5.1 Power stage

Navigation: SmartCtrl > Design a predefined topology > Power factor corrector >

Boost PFC power stage

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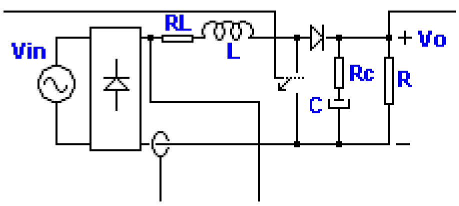
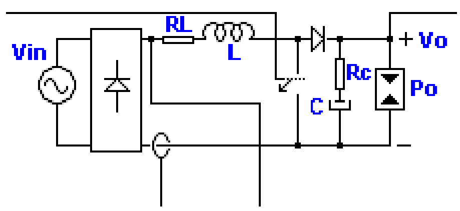
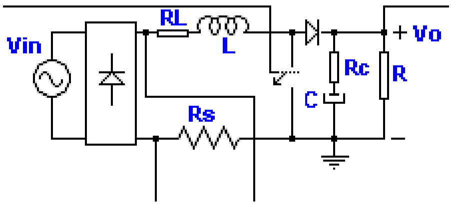
The Boost PFC is based on a double loop control scheme, and therefore the output voltage and the current through the inductor are sensed simultaneously. There are Four options for the plant, depending on the load and the multiplier:



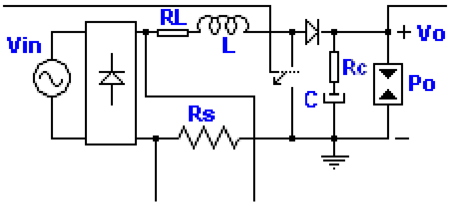
Generic multiplier + Boost PFC (Resistive load)



Generic multiplier + Boost PFC



UC3854A multiplier + Boost PFC (Resistive load)



UC3854A multiplier + Boost PFC (Constant power load)

The current loop is designed considering a piecewise linear model of the plant: using quasi-static assumption, the small signal model for each operating point is calculated as in a DC/DC boost converter.

The input data variables are listed and defined below:

Input data

V_{in}(rms)	Input Voltage (V)
R_L	Equivalent Series Resistor of the Inductance (Ohms)
L	Inductance (H)
Rc	Equivalent Series Resistor of the output capacitor (Ohms)
C	Output Capacitor (F)
V_o	Output Voltage (V)
R	Load Resistor (Ohms)
P_o	Output Power (W)
wta	Line angle(º). The current loop is designed considering the plant calculated for this operating point. This line angle is indicated as a red dot in the output panel that represents the **Rectified voltage and external compensator output**(See Graphic and text panels window for detailed information)
F_{SW}	Switching frequency (Hz)
Line frequency	Line frequency (Hz)

1.4.5.2 Graphic panels

Navigation: SmartCtrl > Design a predefined topology > Power factor corrector >

Graphic panels

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The window is divided in six different panels:
The graphic panels are:

- **Bode plot Module (dB)**
- **Bode plot Phase (º)**
- **Nyquist diagram**
- **Line current**
- **Oscillator ramp and internal compensator**
- **Rectified voltage and external compensator output**

Oscillator ramp and internal compensator

Navigation: SmartCtrl > Design a predefined topology > Power factor corrector > Graphic panels >

Oscillator ramp and internal compensator

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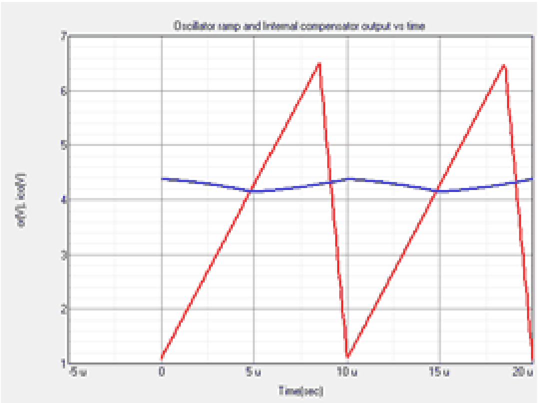
This graphic panel provides information about the output of the inner control compensator (blue line) compared to the oscillator ramp (red line). The output of the internal compensator is represented for the line angle corresponding to the maximum current ripple through the inductor. This line angle is identified by means of a blue dot in the Rectified voltage and external compensator output graphical panel.

This comparison can be useful to determine whether there could be oscillations. If the slopes of both functions are too similar, there could be more than one intersection per period.



Line current

Navigation: SmartCtrl > Design a predefined topology > Power factor corrector > Graphic panels >

Line current

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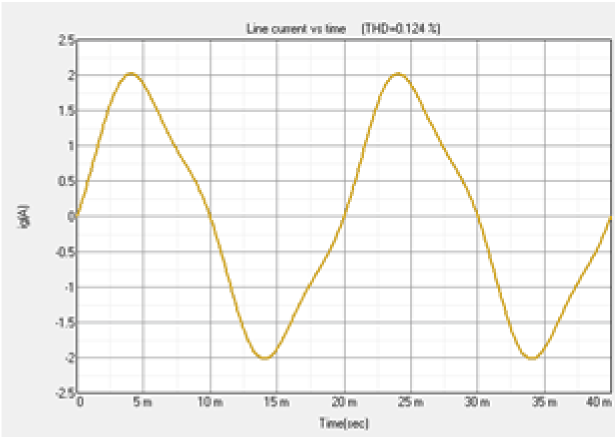
This graphic panel provides information about the line current and its harmonic distortion. The line current waveform is calculated assuming that the current loop follows perfectly the reference generated by the outer loop. However, in some occasions there is a zero-cross distortion and the actual line current would differ from the one represented. In these cases, a warning message would appear in the solution map window.



Rectified voltage and external compensator output

Navigation: SmartCtrl > Design a predefined topology > Power factor corrector > Graphic panels >

Rectified voltage and external compensator output

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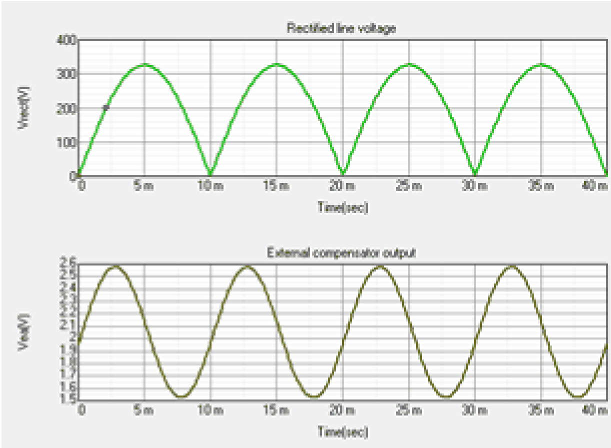
This graphic panel provides information about the external compensator output voltage. Its phase shift compared to the rectified voltage can be assessed. If the compensator output voltage has not an appropriate phase shift compared to the rectified voltage (reference), the line current distortionwill increase.

The current loop is designed considering a piecewise linear model of the plant.The current plant represented in the Bode plot panels (see Graphic panels window) corresponds to the operating point marked with a red dot in the rectified voltage. The small signal model for the plant is calculated as in a DC/DC boost converter for this operating point. This dot can be moved by clicking and dragging with the mouse, resulting in a variation of the operating point. As the dot changes its position, the Bode plot corresponding to the inner loop varies, as well as the attenuation information in the K-factor panel refreshes according to the indicated operating point.

The blue dot in the rectified voltage represents the operating point that corresponds to the maximum current ripple through the inductor. The gr aphics in the Oscillator ramp and internal compensator panel have been represented for this operating point.



1.4.5.3 Multipliers

Multiplier

Navigation: SmartCtrl > Design a predefined topology > Power factor corrector > Multipliers >

Multiplier

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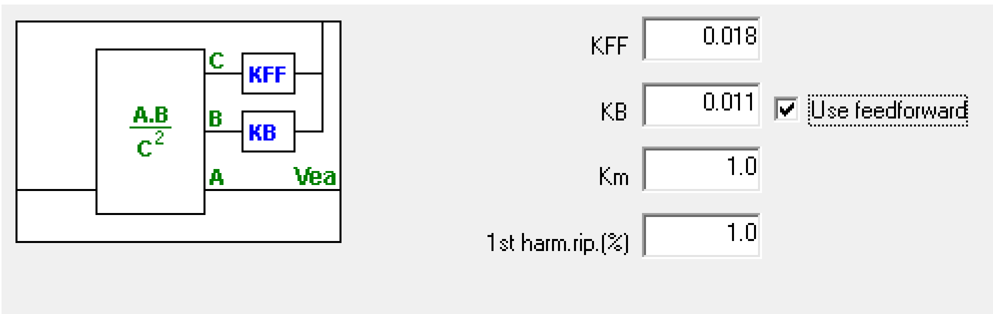
Using feedforward:



The **multiplier** has the following parameters:

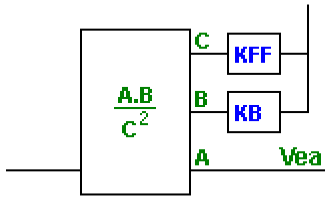
KB Gain of the current reference for the inner loop.

Km Multiplier gain.

And, when the use of feed-forward is selected:

KFF Gain of the feed-forward. It is the ration between the rms input voltage and the average input voltage to the multiplier.

1st harm.rip.(%) Ratio between the amplitude of the first harmonic of the rectified input voltage and its average value.



UC3854A multiplier

Navigation: SmartCtrl > Design a predefined topology > Power factor corrector > Multipliers >

UC3854A multiplier

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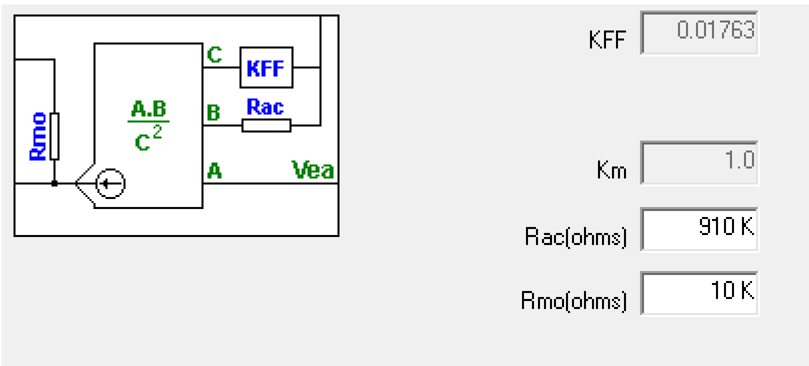


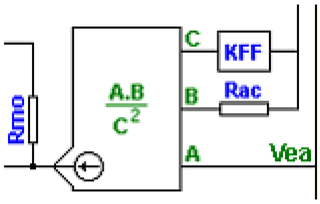
The **UC3854A multiplier** has the following parameters:

KFF Gain of the feed-forward. It is the ration between the rms input voltage and the average input voltage to the multiplier.

Km Multiplier gain.

Rac Resistance to introduce the current reference for the inner loop (Ohms)

Rmo Resistance to convert the multiplier output current into a voltage reference for the inner compensator (Ohms)



1.5 Desing a generic topology

Navigation: SmartCtrl >

Design a generic topology

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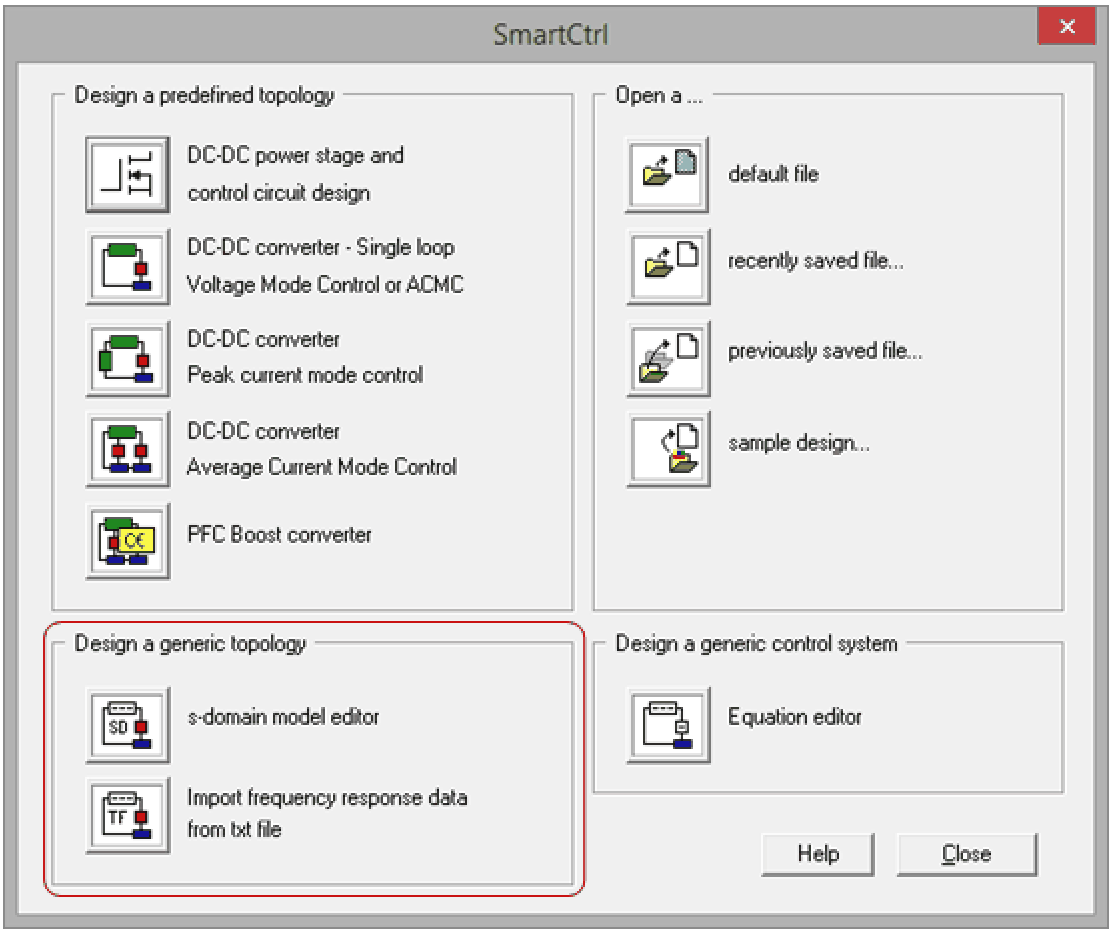
SmartCtrl not only helps the designer when a pre-defined power converter is considered, it also allows the design of the control loop of any generic converter.

To carry out the design of the control when the plant is not a pre-defined DC-DC converter, the plan must be provided either by means of an s-domain transfer function or importing the plant frequency response from a .txt file. Depending of the desired input method, the designer must select between:

s-domain model editor
Import frequency response data from a .txt file



1.5.1 s-domain model editor

Navigation: SmartCtrl > Desing a generic topology >

s-domain model editor

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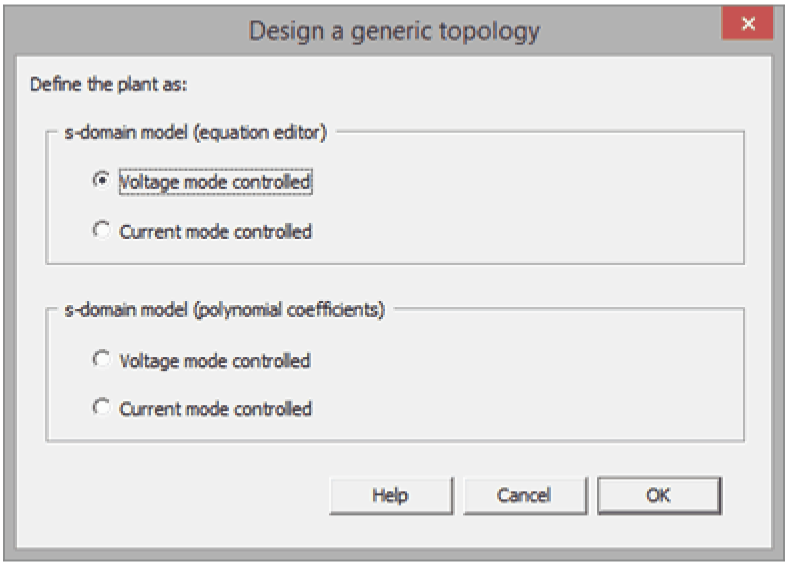
The s-domain model editor is available at:

The s-domain model editor provides two different options in order to define the s-domain transfer function plant:

•**s-domain model (equation editor)**
 •**s-domain model (polynomial coefficients)**

In both cases, the user must select the control strategy.



1.5.1.1 Import frequency response data from .txt file

Navigation: SmartCtrl > Desing a generic topology > s-domain model editor >

Import frequency response data from .txt file

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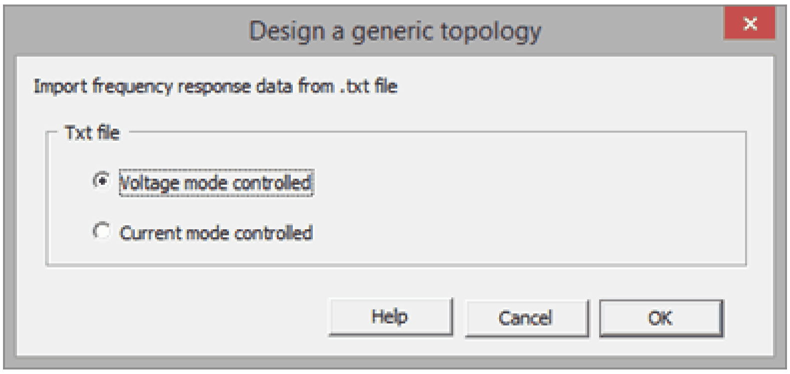
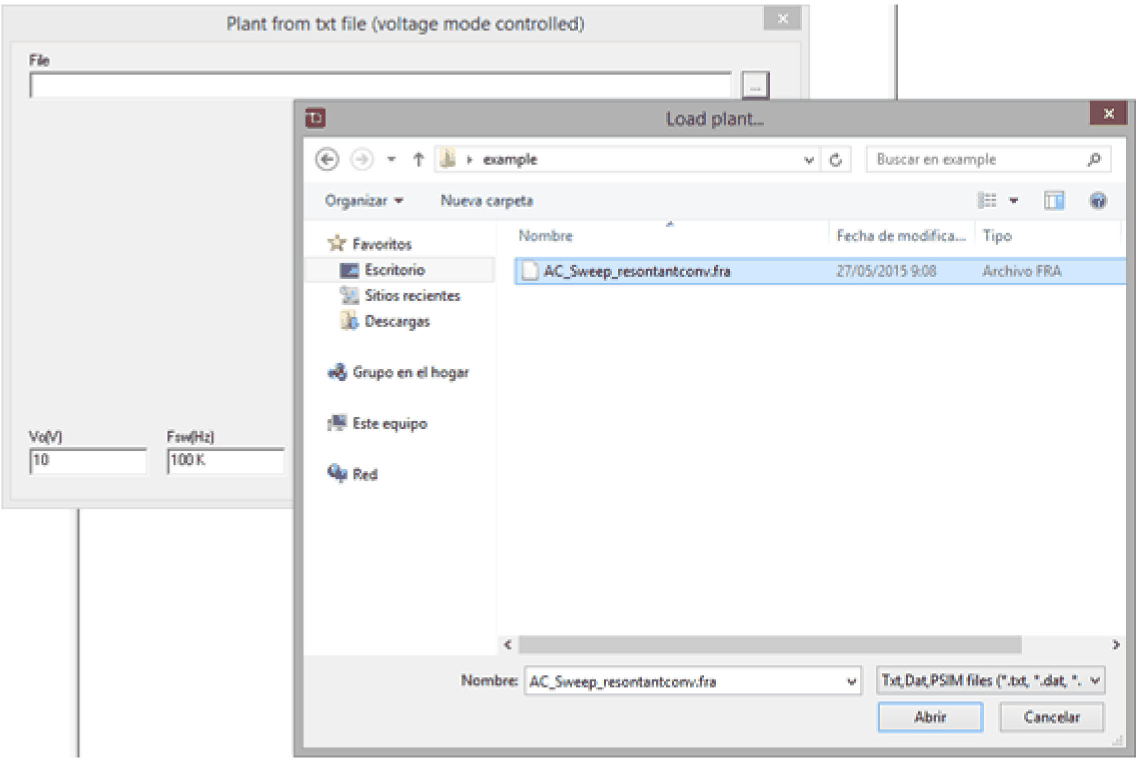
The "Import frequency response form a .txt file" is also available at:

SmartCtrl allows the designer to import his own transfer plant function and design an appropriate control loop. This feature is only available for single loop designs. To define the imported transfer function the user must specify the intended control type:

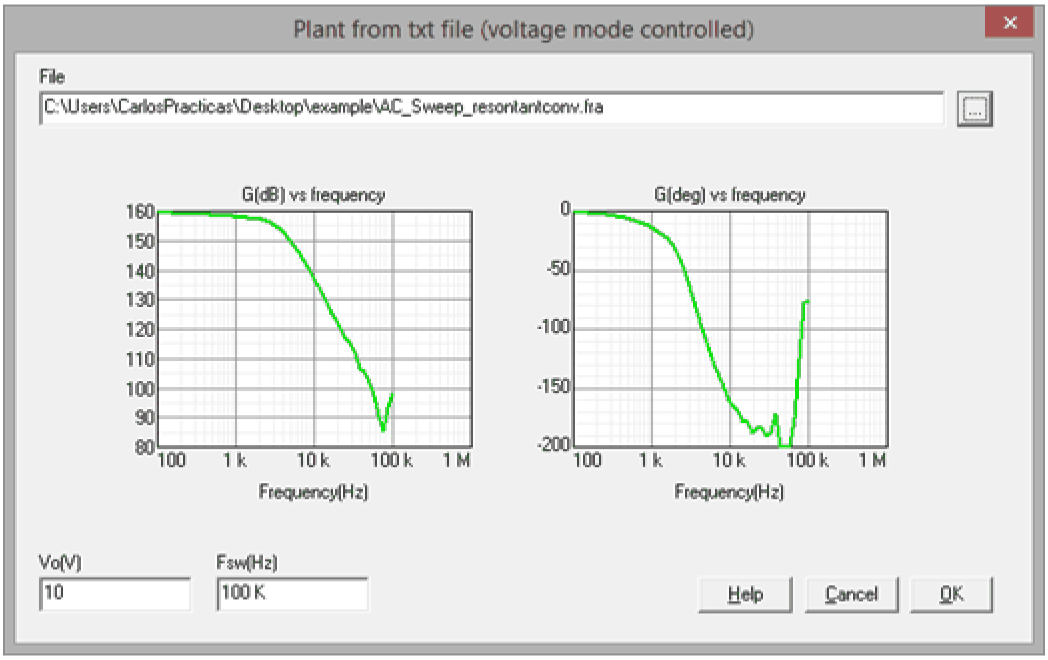


Take into account that, whether the imported plant is current mode controlled or voltage mode controlled, the single loop design process will be the same. The only difference is related to the available sensors, which are different for each case.

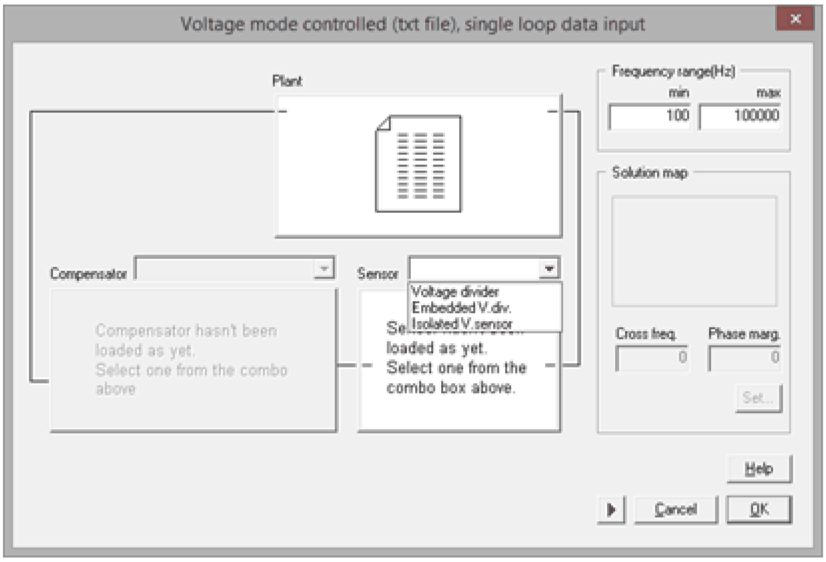
Once the control type has been selected, the file that contains the plant frequency response must be selected. SmarCtrl is able to load the following file formats: *.dat, *.txt, *.fra



Once the file has been selected, the data is loaded to SmartCtrl and the magnitude and phase are displayed as depicted in the next figure.



And some additional data such as the output voltage (only in voltage mode control) and the switching frequency must be specified.
Click OK to continue.
Depending upon it is a current mode controlled or voltage mode controlled, the available sensors are the following:



Voltage mode controlled

[Voltage divider]()

[Embedded Voltage Divider]()

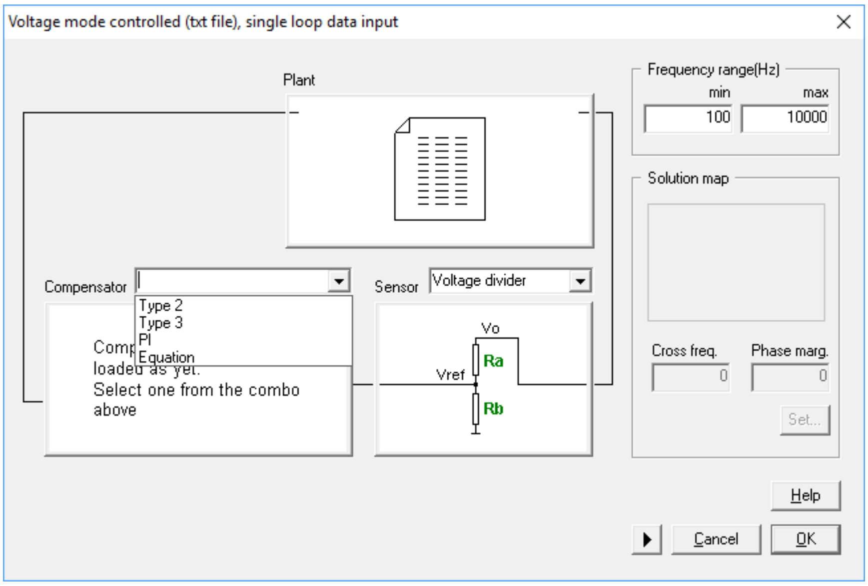
[Isolated V. sensor]()

Current mode controlled

[Current sensor]()

[Hall effect sensor]()

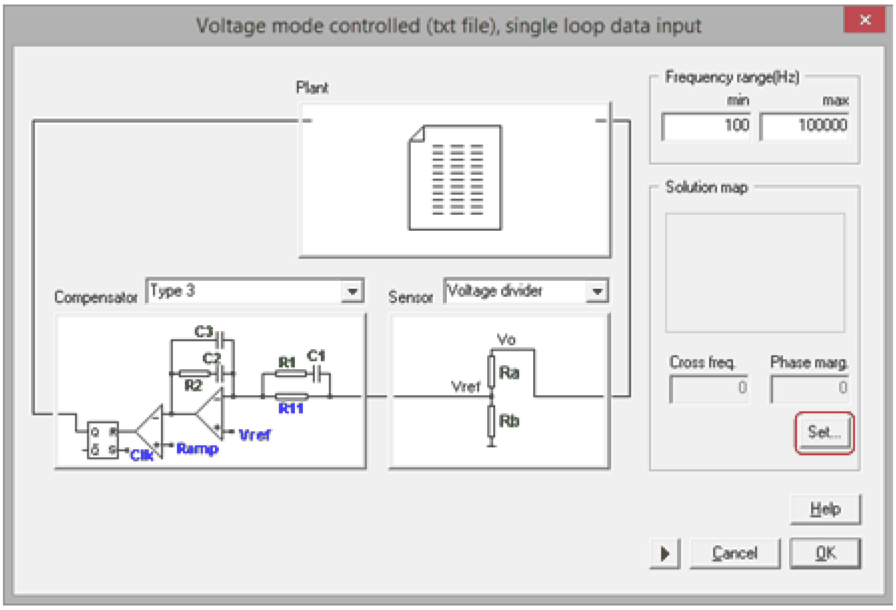
Finally,select the compensator.

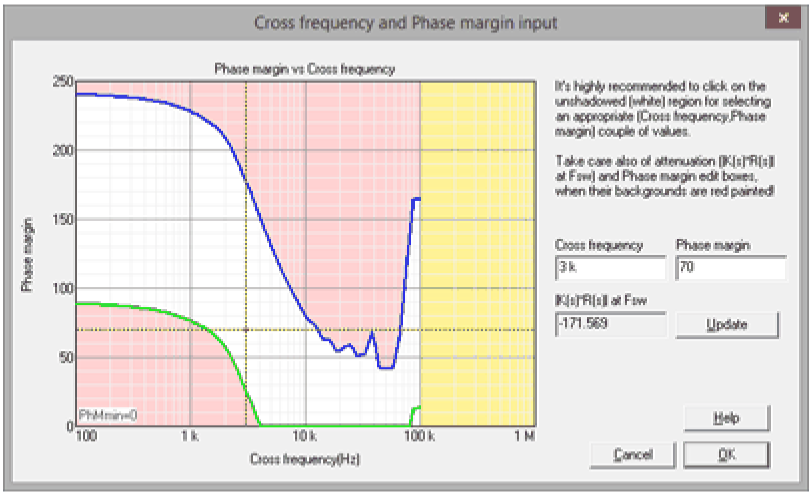


Compensator types:

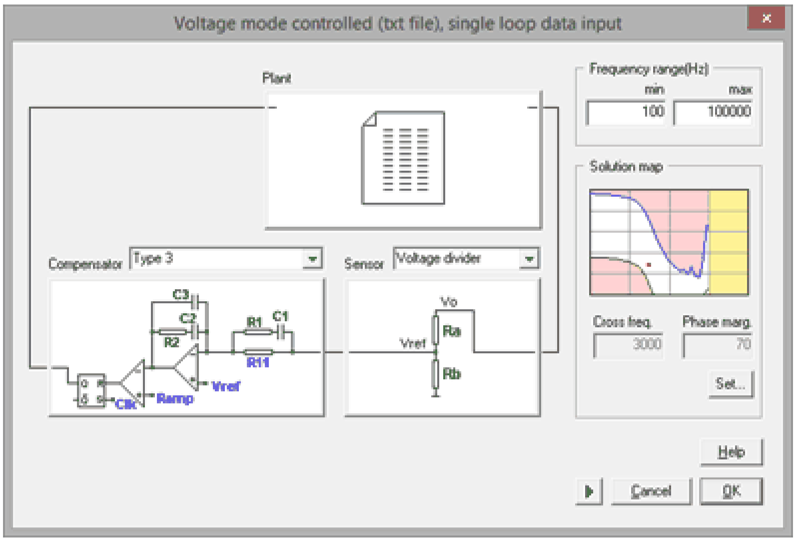
- •Type 3 Unattenuated
- •Type 2
- •Type 2 unattenuated
- •PI
- •PI unattenuated
- •Single Pole
- •Single Pole unattenuated
- •**Equation Editor**

Once the system has been defined, SmartCtrl calculates the **Solutions Map** (only for predefined compensators), in which it is shown graphically all the combinations of crossover frequency and phase margin that leads to stable solutions. To continue, click on set and the solutions map will be displayed. After that, select a point within the stable solutions area (white area) and then click OK.

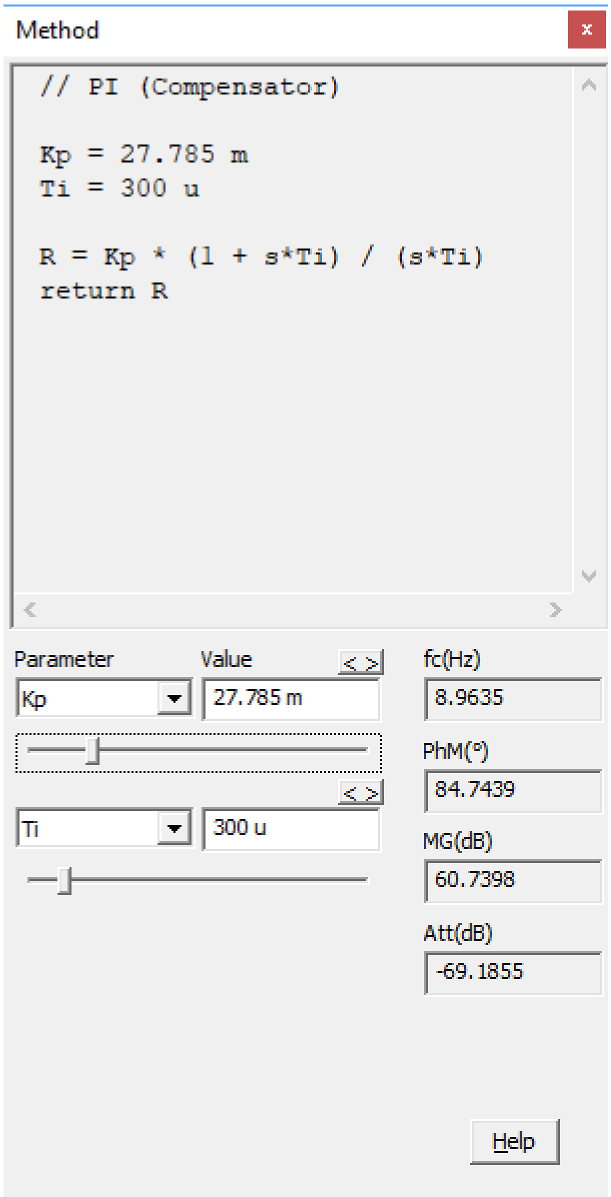




Now confirm the design and the program will automatically show the performance of the system in terms of frequency response, transient response. (See **Graphic and text panels** window for detailed information)



In case the user has selected a customized compensator using the equation editor, use the compensator parameter sweep available in the Method box instead of the solutions map.



1.5.1.2 s-domain model (equation editor)

Navigation: SmartCtrl > Desing a generic topology > s-domain model editor >

s-domain model (equation editor)

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The s-domain model editor (equation editor) provides two different options depending on whether the defined plant transfer function is intended for:

- Voltage mode control (VMC)
- Current mode control (CMC)

s-domain model (equation editor) VMC

Navigation: SmartCtrl > Desing a generic topology > s-domain model editor > s-domain model (equation editor) >

s-domain model (equation editor) VMC

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When the power converter is defined through its s-domain transfer function, the design procedure is as follow:

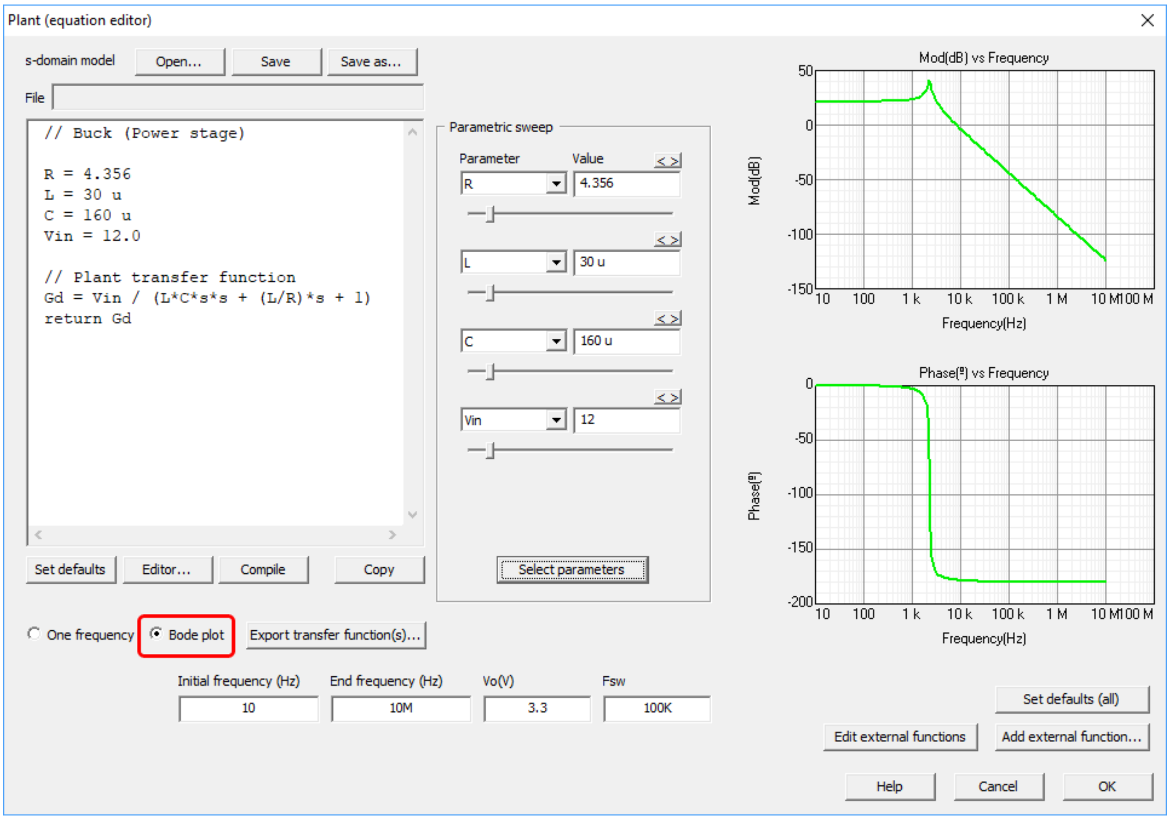
First, the user must define the s-domain transfer function of the plant, choosing amongst two different options:

- Import a previous design (click on open)
- Define a new transfer function (click on editor).

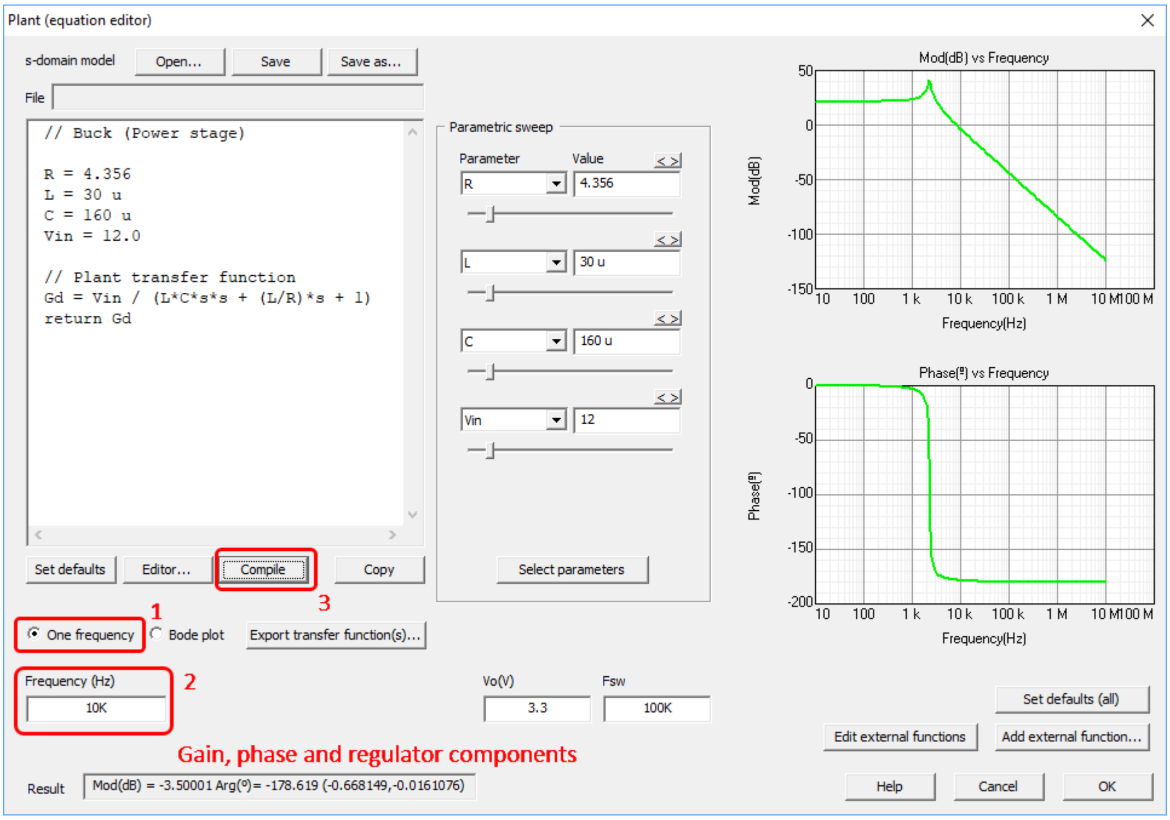
Once the equation has been introduced:

- Click on "Save" to save the mathematical equations in a text file with extension .tromod
- Click on "compile" to continue.
- If desired, the frequency response of the transfer function can be exported as a .txt file by clicking on "Export transfer function".

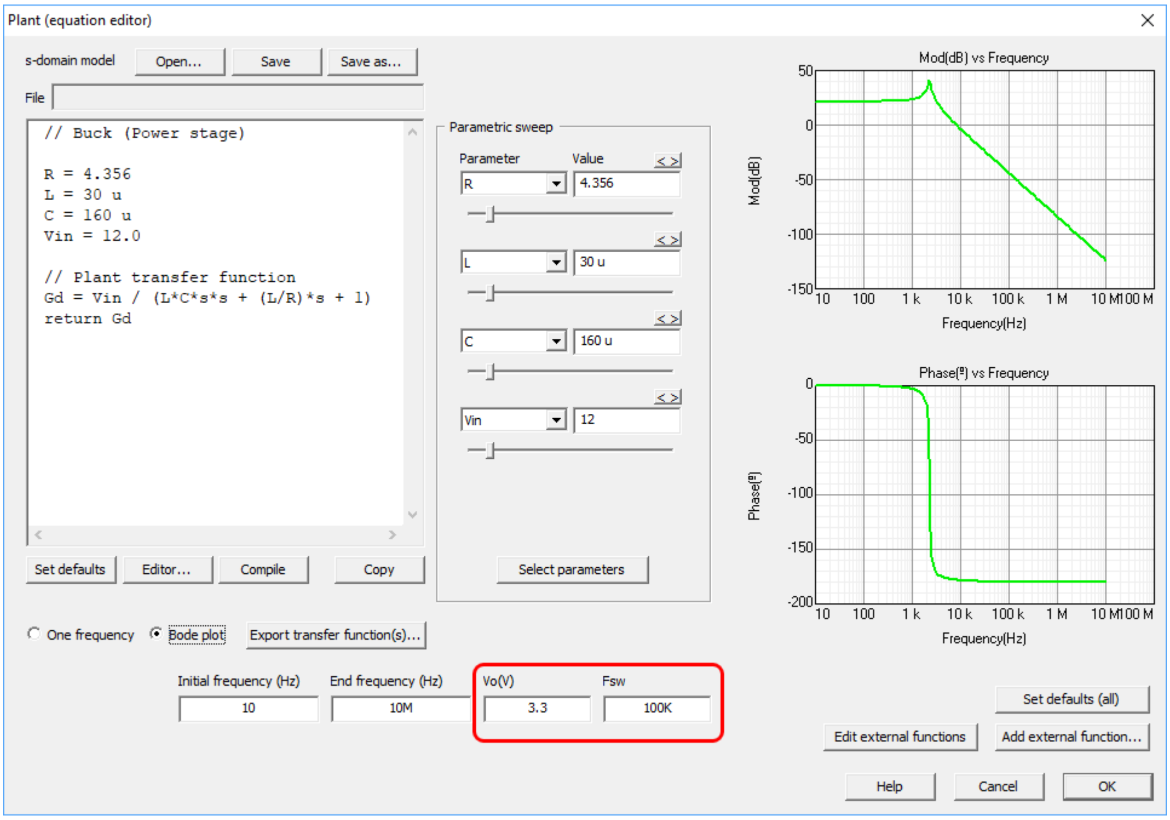
The option "Bode plot" is selected by default, the frequency response of the previously defined transfer function is shown on the right hand side panels.



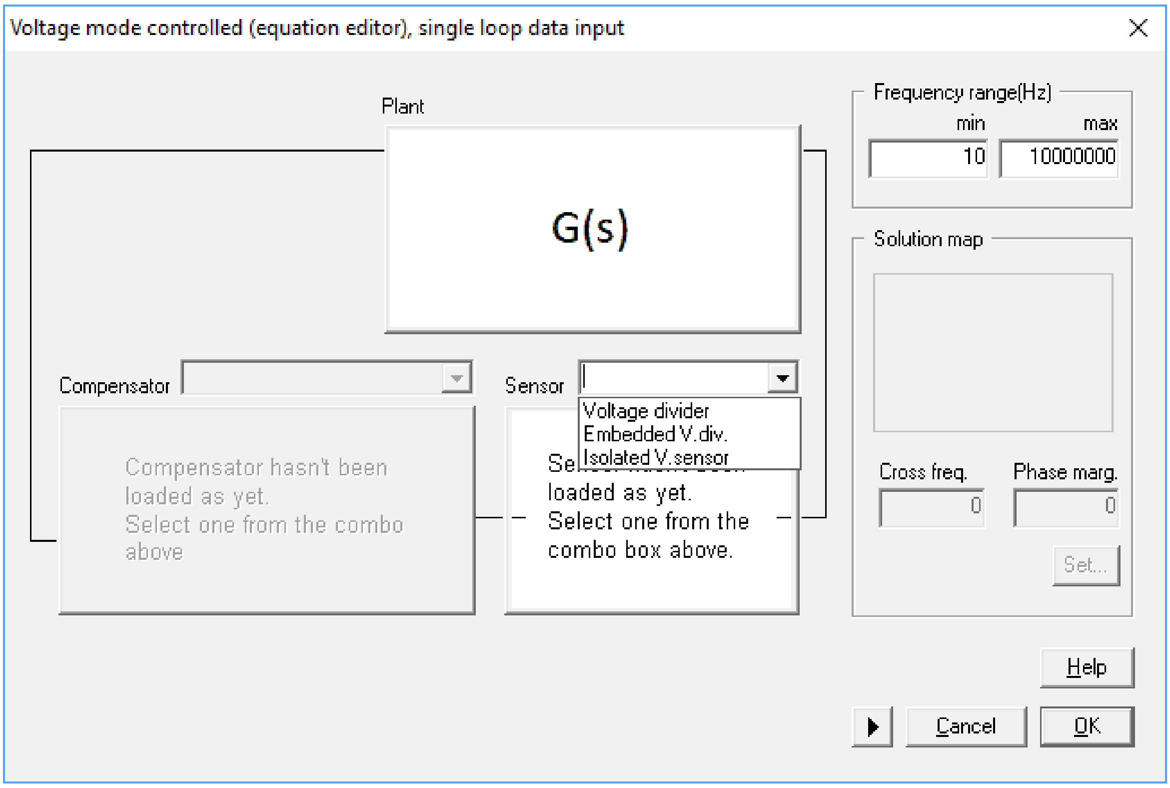
To check the gain, phase and rectangular components of the frequency response at a particular frequency, the option "One frequency" is provided.
As shown in the following figure: first select the option "one frequency", secondly specify the frequency and finally, click on compile and the gain, phase and rectangular components at the specified frequency are shown below.



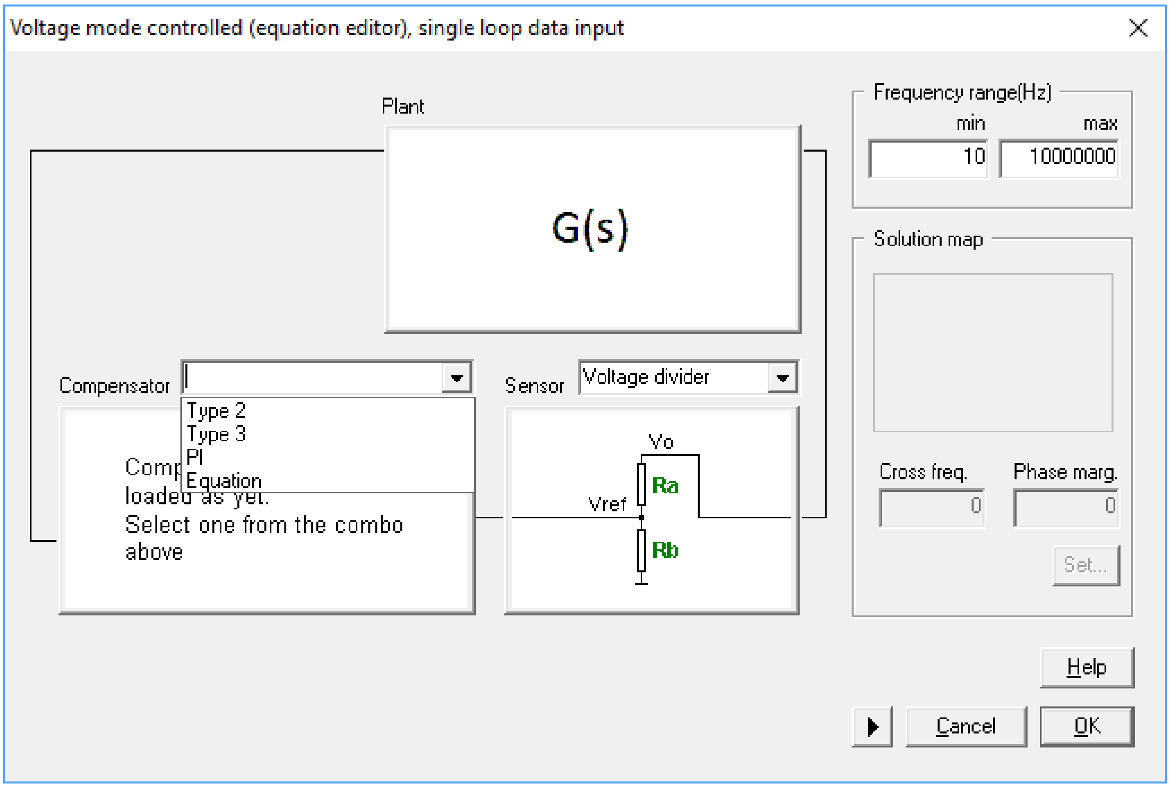
When the s-domain model is intended for Voltage Mode Control (VMC), then the output voltage and the switching frequency must be specified. As highlighted in the next picture:



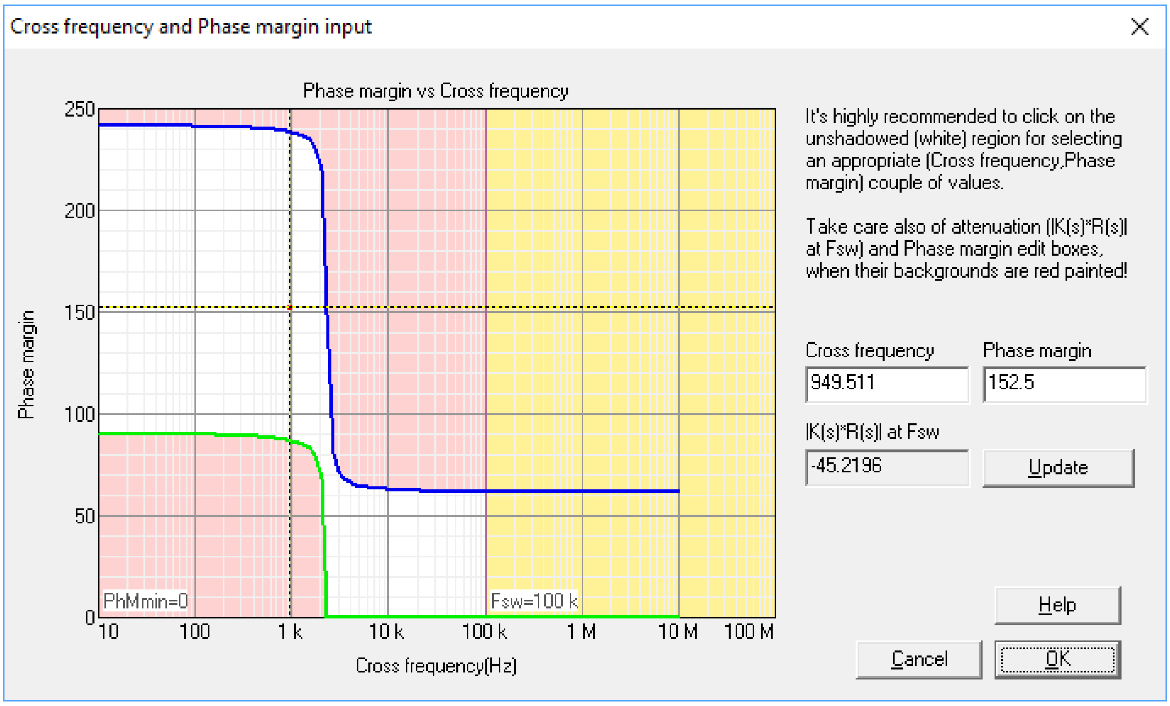
After that, select the sensor.

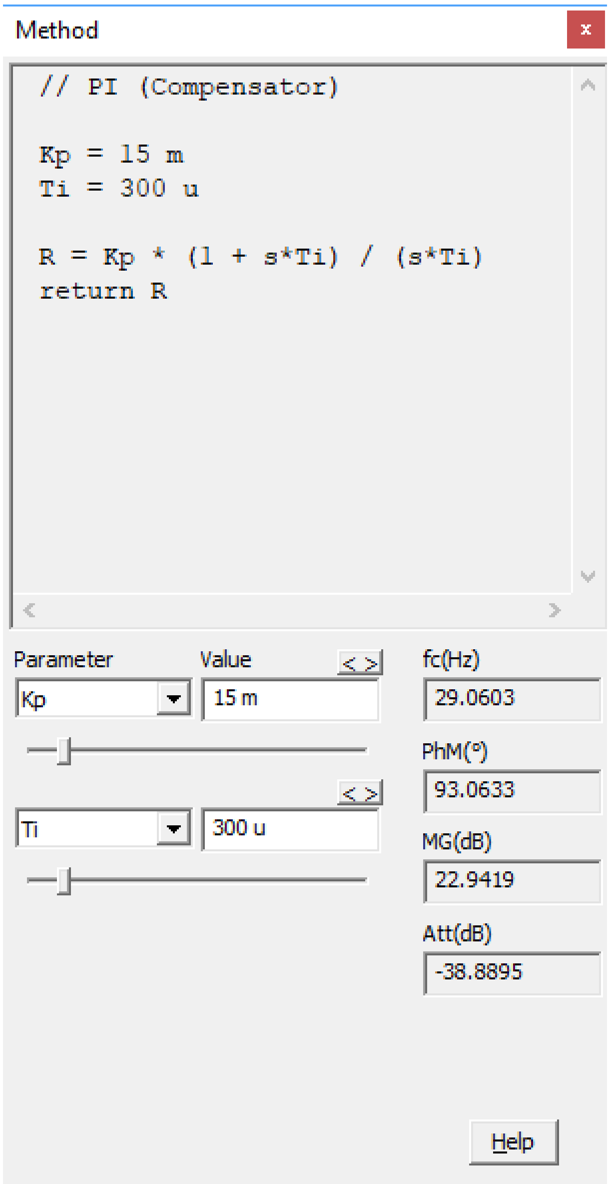


And then select the compensator, using the predefined options available or use the equation editor for a customized compensator.



Select the cross frequency and the phase margin on the Solutions Map for pre-defined compensators or use the Method box for the compensator parameter sweep .


Cross frequency and Phase margin input
Phase margin vs Cross frequency
250
200
150
100
50
0
Phase margin
PhMmin=0
Fsw=100 k
10
100
1 k
10 k
100 k
1 M
10 M
100 M
Cross frequency(Hz)
It's highly recommended to click on the unshadowed (white) region for selecting an appropriate (Cross frequency,Phase margin) couple of values.
Take care also of attenuation (|K(s)*R(s)| at Fsw) and Phase margin edit boxes, when their backgrounds are red painted!
Cross frequency
949.511
Phase margin
152.5
|K(s)*R(s)| at Fsw
-45.2196
Update
Help
Cancel
OK



s-domain model (equation editor) CMC

Navigation: SmartCtrl > Desing a generic topology > s-domain model editor > s-domain model (equation editor) >

s-domain model (equation editor) CMC

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When the power converter is defined through its s-domain transfer function, the design procedure is as follow:

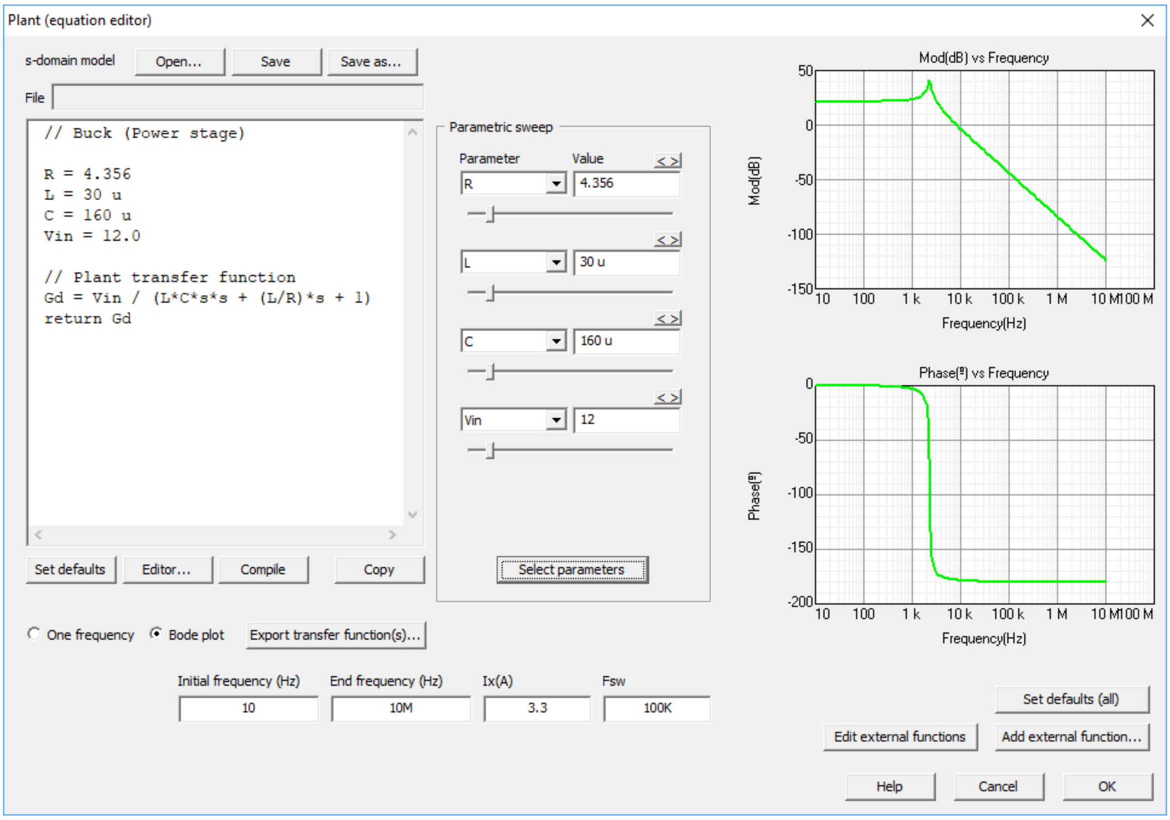
First, the user must define the s-domain transfer function of the plant, choosing amongst two different options:

· Import a previous design (click on open)
· Define a new transfer function (click on editor).

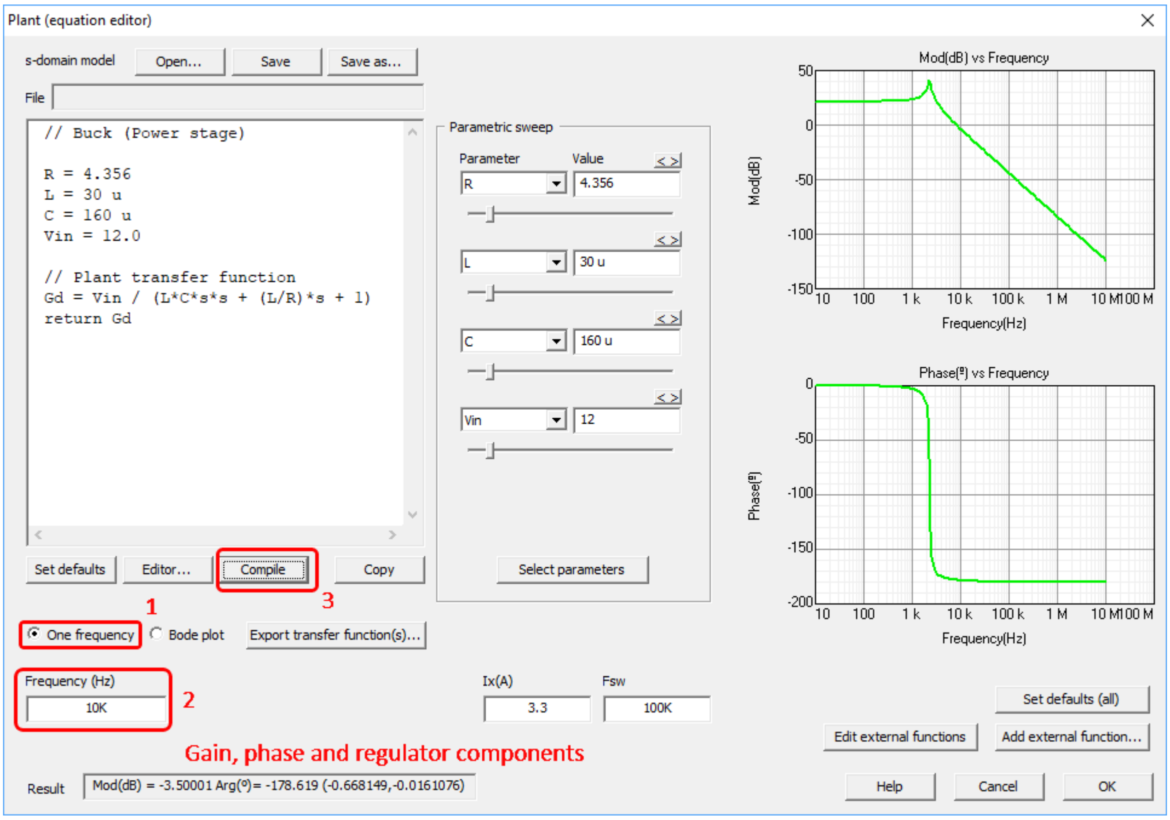
Once the equation has been introduced:

· Click on "Save" to save the mathematical equations in a text file with extension .tromod
· Click on "compile" to continue.
· If desired, the frequency response of the transfer function can be exported as a .txt file by clicking on "Export transfer function".

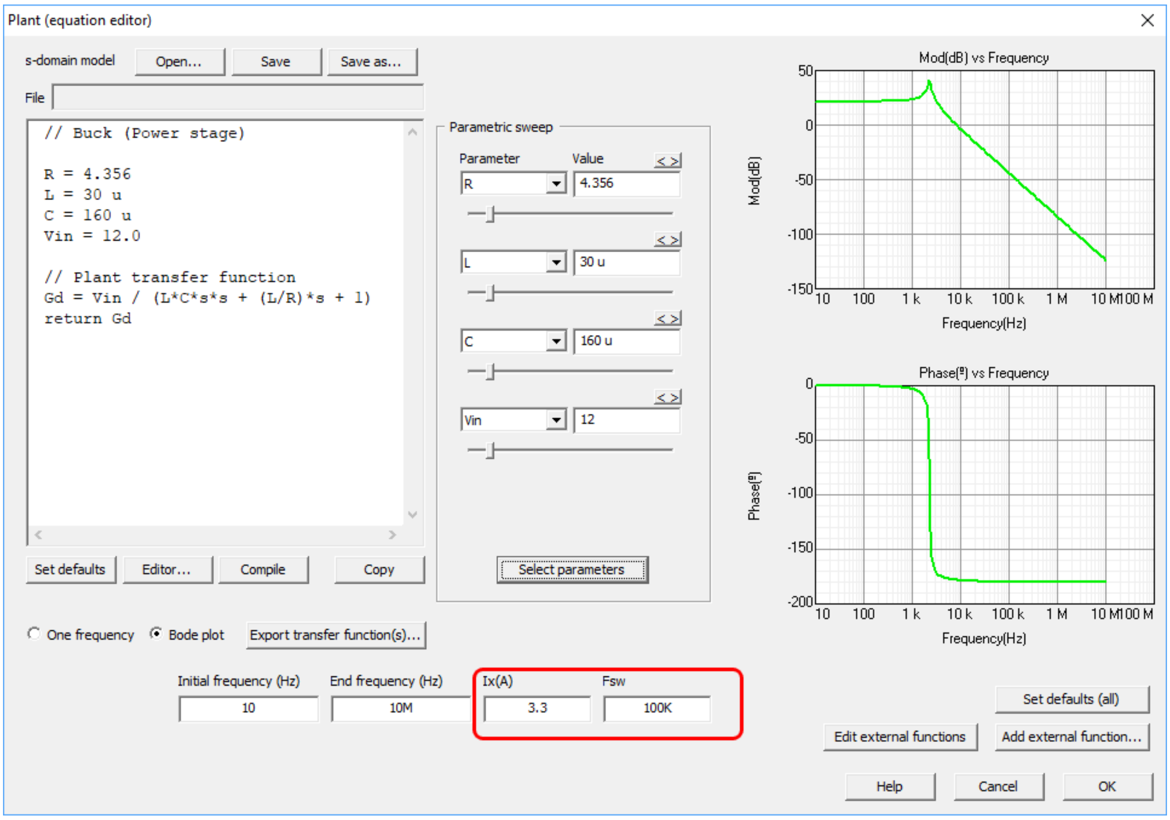
The option "Bode plot" is selected by default, the frequency response of the previously defined transfer function is shown on the right hand side panels.



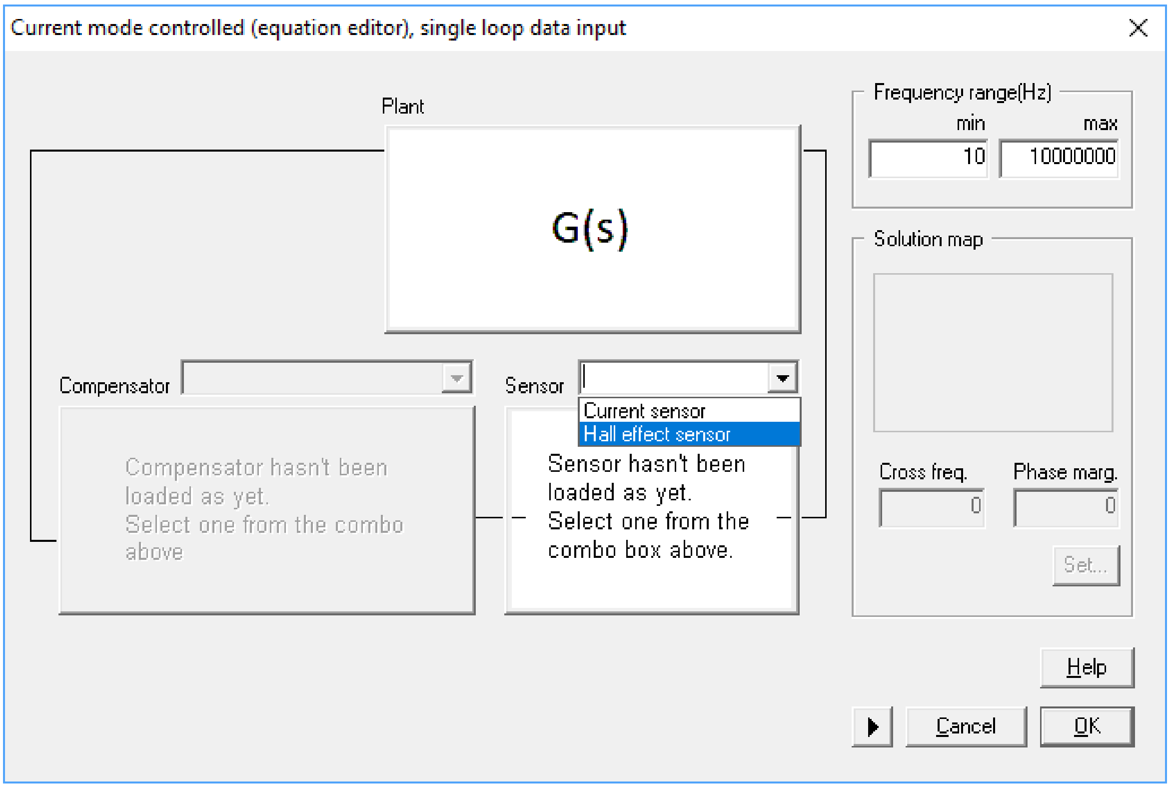
To check the gain, phase and rectangular components of the frequency response at a particular frequency, the option "One frequency" is provided. As depicted in the following figure: first "one frequency" must be selected, secondly the frequency should be specified and finally, click on compile and the gain, phase and rectangular components at the specified frequency are shown below.



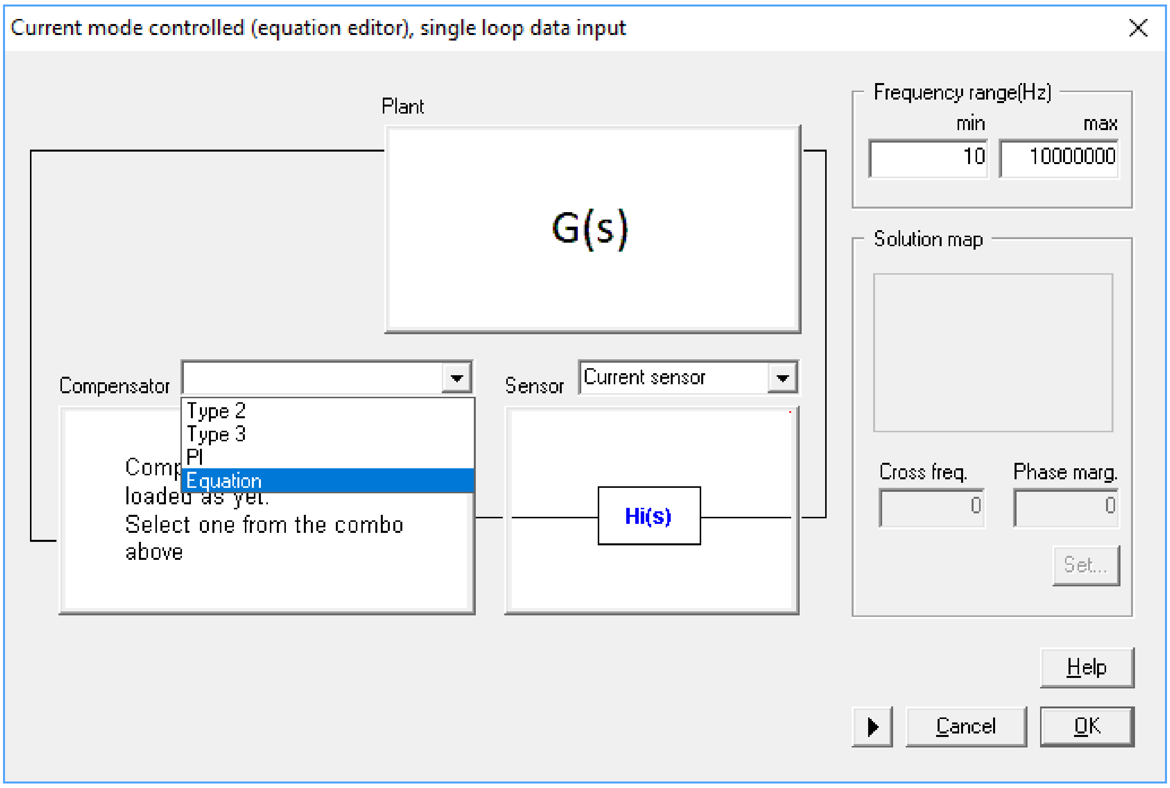
When the s-domain model is intended for Current Mode Control (CMC), then the current to be controlled value and the switching frequency must be specified. As highlighted in the next picture:



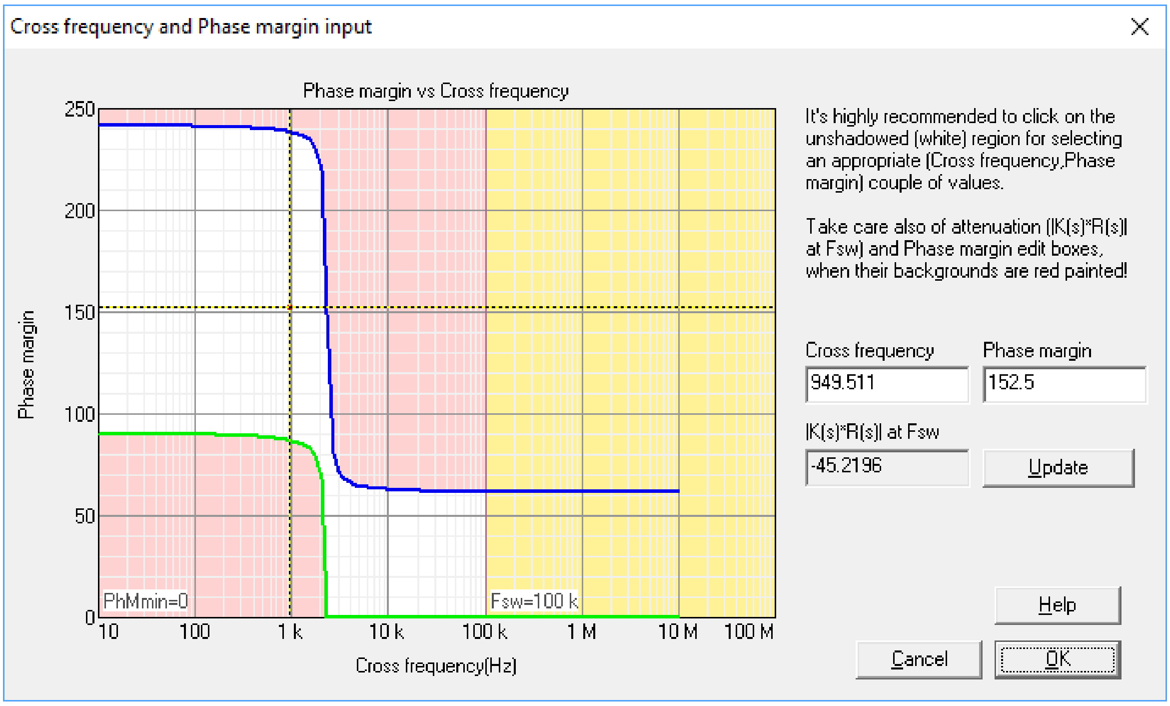
After that, select the sensor.

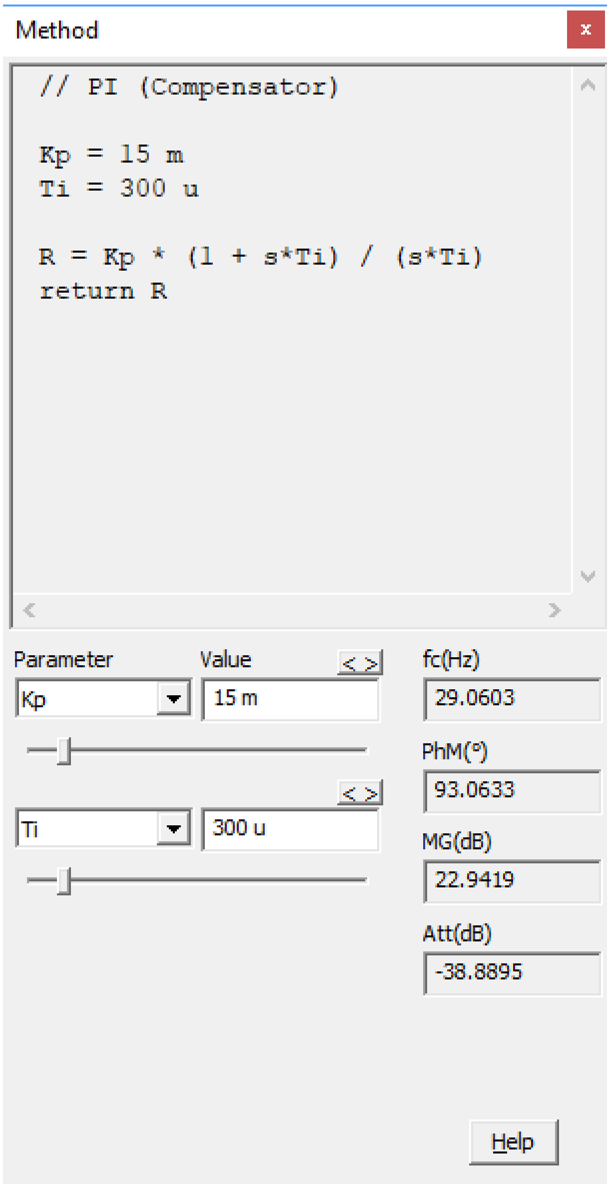


And then select the compensator, using the predefined options available or use the equation editor for a customized compensator.



Select the cross frequency and the phase margin on the Solutions Map for pre-defined compensators or use the Method box for the compensator parameter sweep .


Cross frequency and Phase margin input
Phase margin vs Cross frequency
Phase margin
Cross frequency(Hz)
PhMmin=0
Fsw=100 k
It's highly recommended to click on the unshadowed (white) region for selecting an appropriate (Cross frequency,Phase margin) couple of values.
Take care also of attenuation (|K(s)*R(s)| at Fsw) and Phase margin edit boxes, when their backgrounds are red painted!
Cross frequency
949.511
Phase margin
152.5
|K(s)*R(s)| at Fsw
-45.2196
Update
Help
Cancel
OK



1.5.1.3 s-domain model (polynomial coefficients)

Navigation: SmartCtrl > [Desing a generic topology](#) > [s-domain model editor](#) >

s-domain model (polynomial coefficients)

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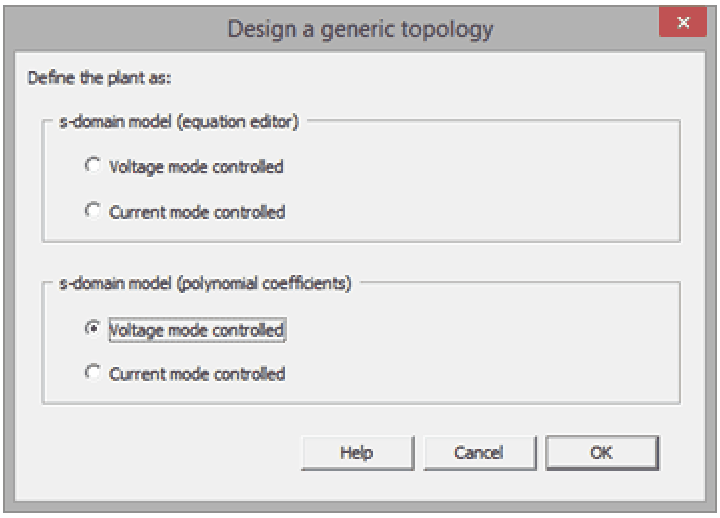
SmartCtrl offers the possibility of describing the data of the plant introducing the coefficients of its transfer function. This feature is only available for single loop designs, and two options are available:

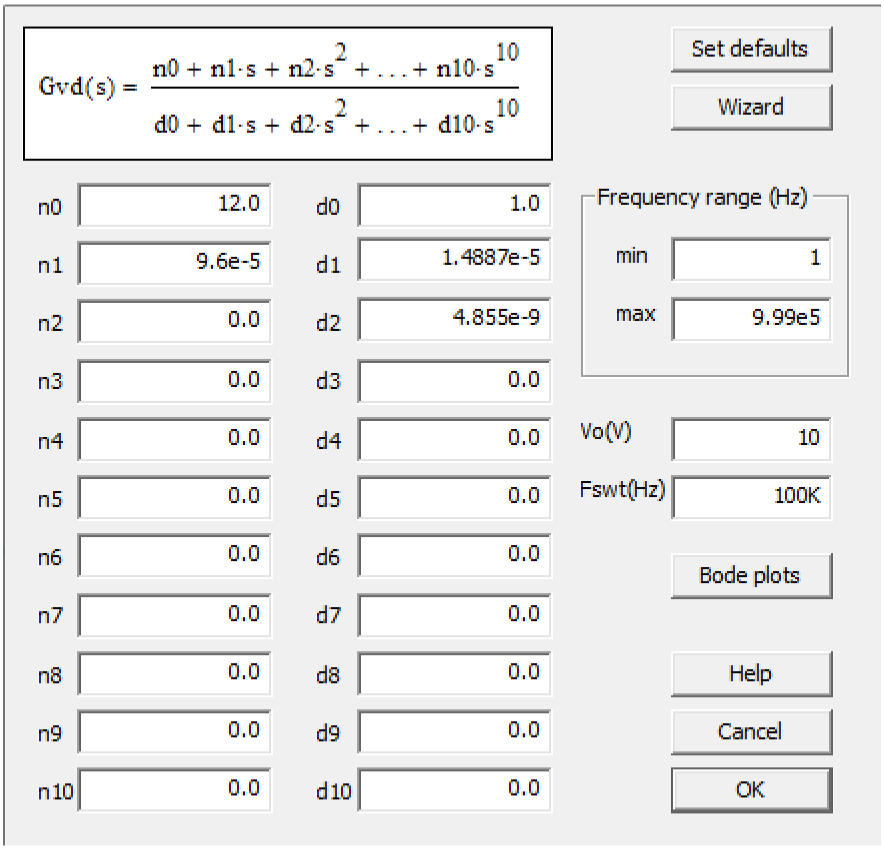
Voltage mode controlled (Shift+L)

Current mode controlled (Shift+U)



The coefficients of the s-domain transfer function have to be introduced. The maximum order of the transfer function is 10. The numerator coefficients are n0 to n10 and the denominator coefficients are d0 to d10.

It is also possible to introduce the transfer function data by using the option **Plant wizard**.
Some additional data must be specified:
The frequency range (minimum frequency and maximum frequency) to consider in Hertz.
The switching frequency (Fsw) in Hertz.
The desired output voltage (Vo) in Volts. (Only if the plant is voltage mode controlled).



By clicking View bodes it is possible to visualize the frequency response (magnitude and phase) that corresponds to the introduced transfer function in the selected frequency range.

Plant wizard

Navigation: SmartCtrl > Desing a generic topology > s-domain model editor > s-domain model (polynomial coefficients) >

Plant wizard

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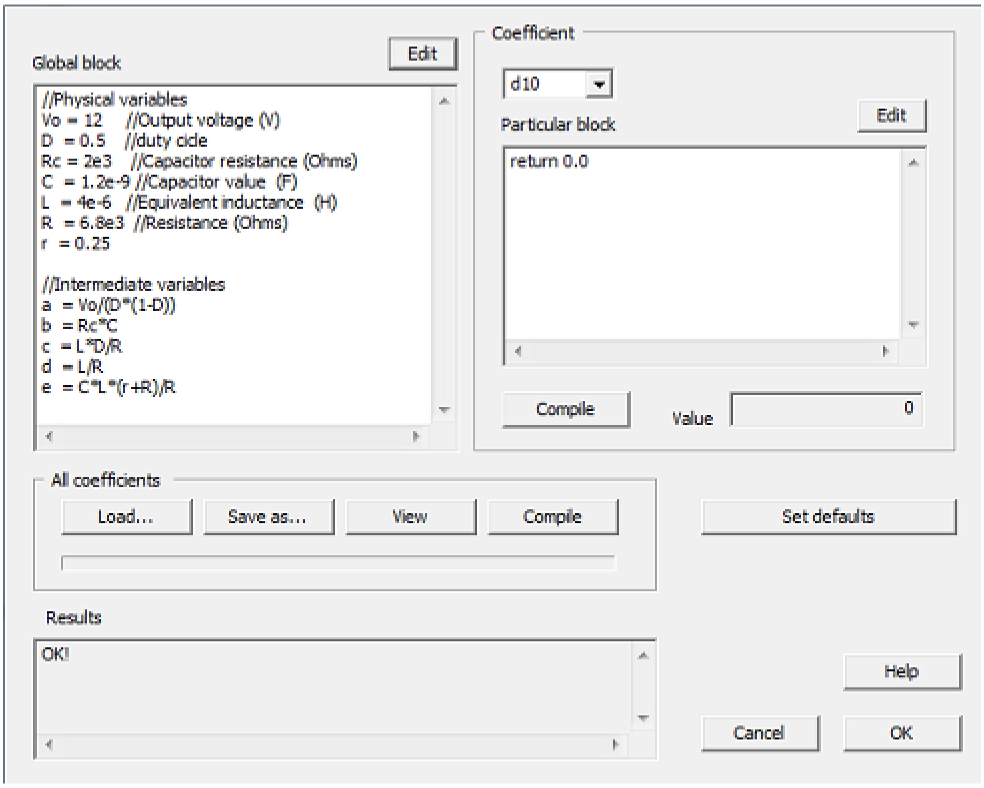
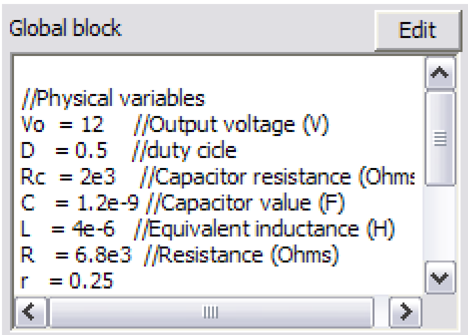
The plant wizard is an assistant that allows to introduce every coefficient of the transfer function (n0,n1,,n10, d0, d1,,d10) as a symbolic expression.



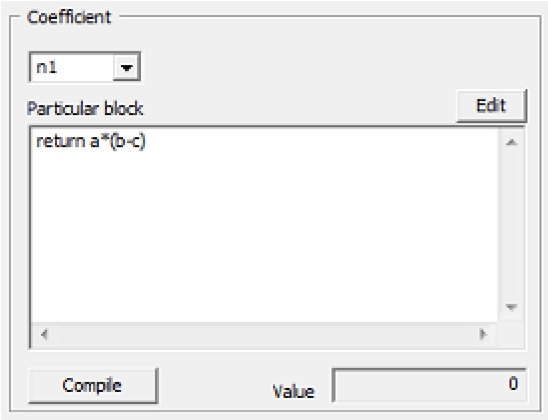
Global block

The Global block corresponds to the definition of the variables and expressions that are common for most coefficients of the transfer function. By clicking on the button Edit, a new edition box is opened (Edit box), which helps the user to introduce the data and the equations with the appropriate format.



Coefficients block

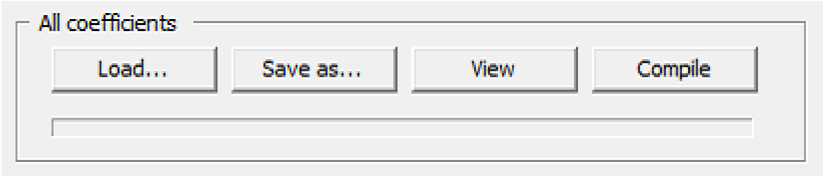
The Coefficients block corresponds to the expressions to calculate the coefficient selected in the combo box. These equations can use the global variables defined in the Global block or new ones can be defined that will be available only locally for the selected coefficient.
By clicking on the button Edit, a new edition box is opened (Edit box), which helps the user to introduce the data and the equations with the appropriate format.



Once the equations have been introduced, it is recommended to click the button Compile. This way, the numerical value of the coefficient is calculated by means of the mathematical expression in the return assignment, considering all the variables previously assigned both in the Global block and the Coefficients block.
If the compilation is successful, the numerical value of the selected coefficient will be displayed in the Value box. Otherwise an error message will appear.

Syntax of the Global block and the Coefficients block:
1. There are two types of instructions: assignment and return.
2. Only one instruction per line is permitted (whether it is assignment or return).
3. Blank lines are allowed.
4. The syntax of the assignment statements is: Var = Expr, where 'Var' is the name of a variable and 'Expr' represents a mathematical expression.
5. Regarding the variable names in the assignments:
a. They must begin with an alphabetic character.
b. They can consist of alphabetic or numeric characters, or underscore.
c. The names sqrt, pow, return and PI are reserved names that cannot be used as variable names.
6. Regarding the mathematical expressions:
a. Algebraic expressions are expressions where valid operators are +, -, *, /.
b. Expressions can use the function sqrt(a), which calculates the square root of a, and the function pow(a, b), which calculates 'a' raised to 'b'.
c. Expressions can use grouping parentheses.
7. The syntax of the return statements is: return Expr, where 'Expr' represents a mathematical expression.
8. The overall block can only contain assignment statements.
9. In the Coefficients block, each coefficient can have assignment statements, but it is mandatory to have at least one return statement, which will always be the last instruction in the block. This return statement defines the mathematical value of that particular coefficient.
10. Comments can be included as annotations made by the designer in order to make the text readable. Comments start with the delimiter doble slash // and continue until the end of the line. These annotations are ignored by the compiler.

All coefficients block
In the block All coefficients, some commands can be executed that affect all coefficients:



•Compile: the numerical values of all the coefficients are calculated. If an error occurs, a message will be displayed.
•Save as: the contents of the Global block and the Coefficients block are stored in a file with extension .trowfun.
•Load: the data stored in the files with extension .trowfun is loaded. Therefore, the Global block and the Coefficients block will be updated with the loaded information.
•View: the content of the Global block and the Coefficients block, as well as the numerical value of the coefficients, is displayed in a new window.

Results box and OK button

All the warning messages are displayed in the Results edit box.

Once the OK button in pressed, all the coefficients are automatically recalculated. If an error occurs, a warning message will be displayed. If the calculation is successful, the coefficient values are displayed in the Plant from s-domain transfer function window.

1.6 Design a generic control system

Navigation: SmartCtrl >

Design a generic control system

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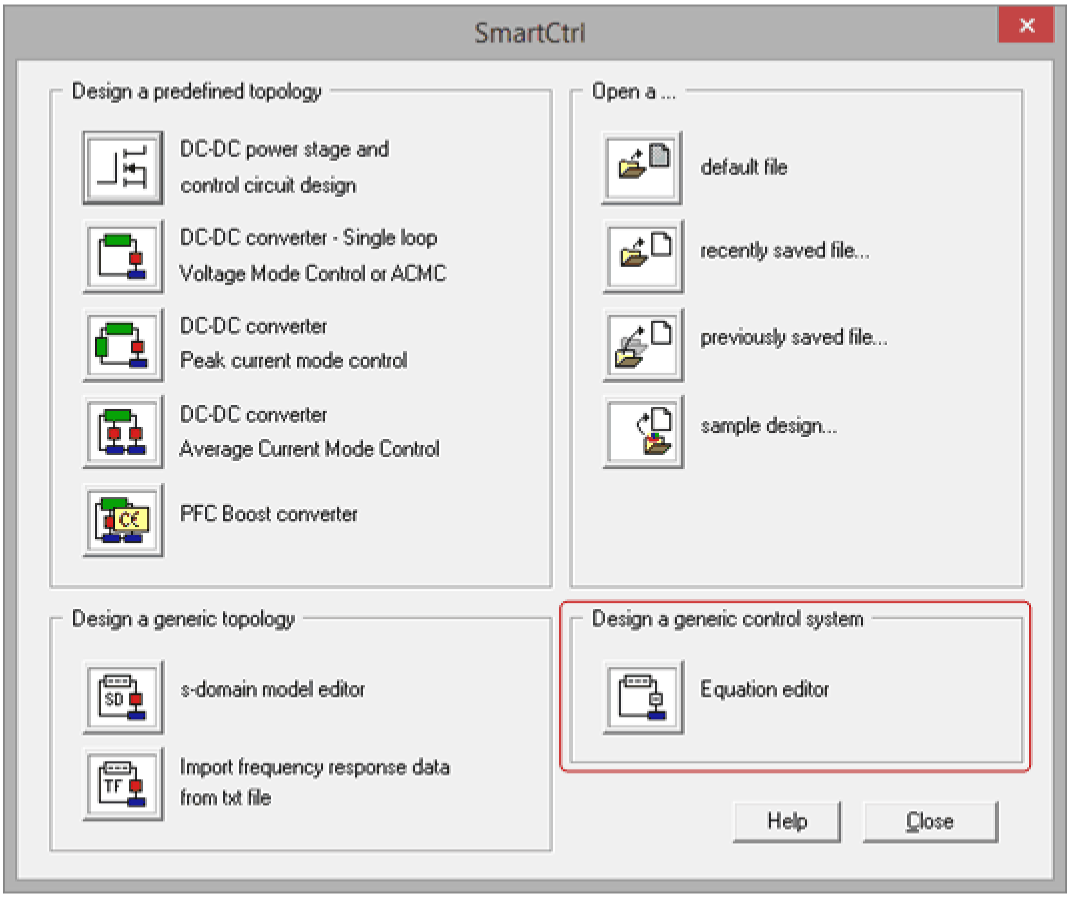
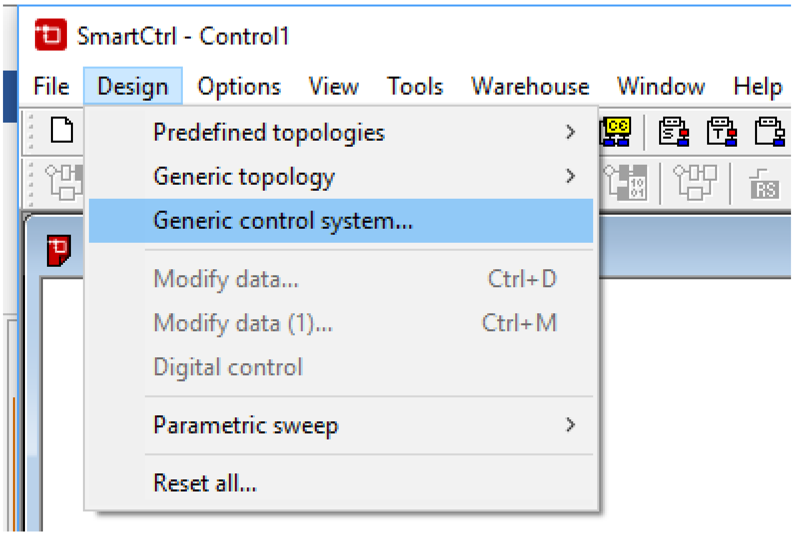
SmartCtrl allows the design of a generic control system regardless the nature of the system, since it is possible to define the whole system with the equation editor.

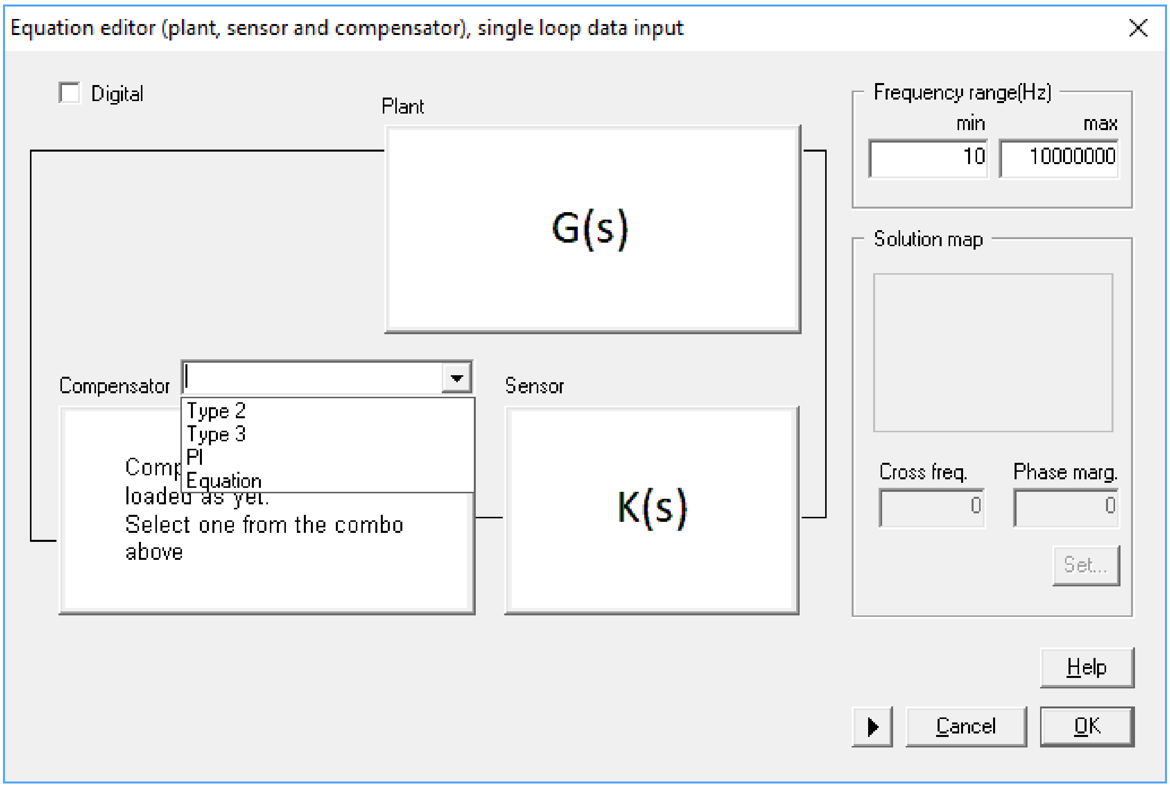


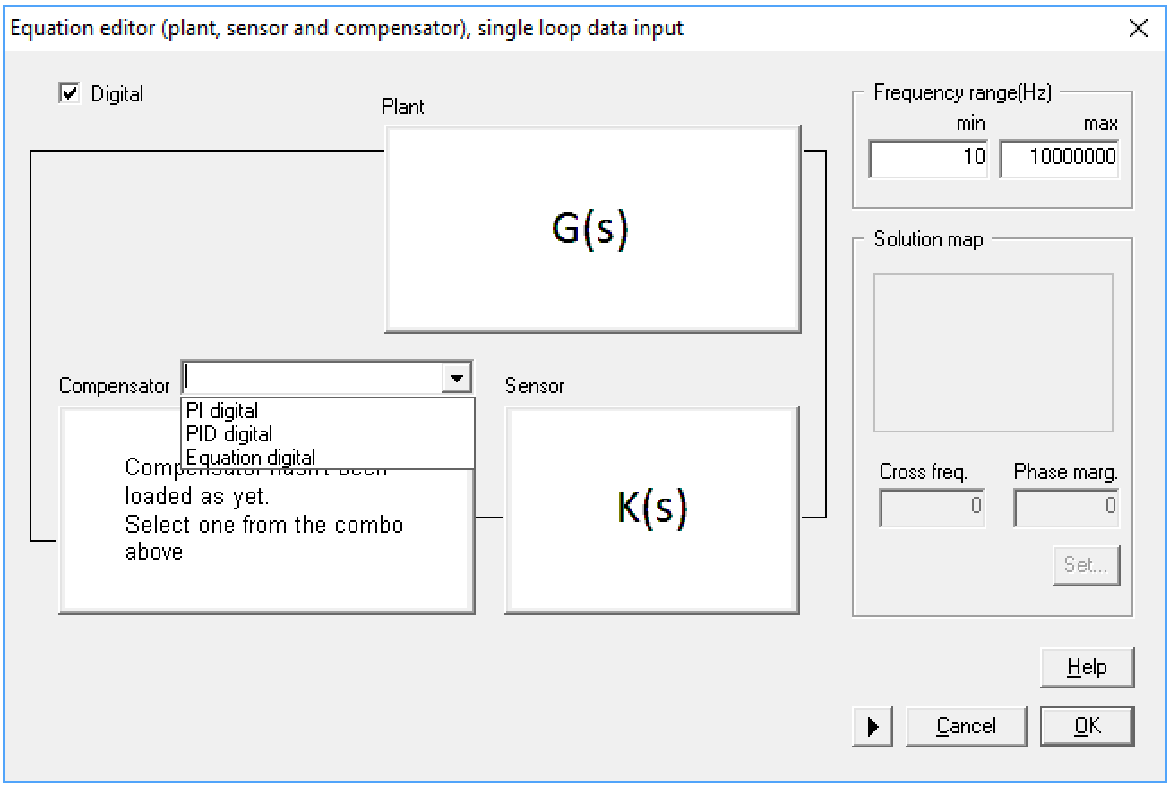
It is also available at:



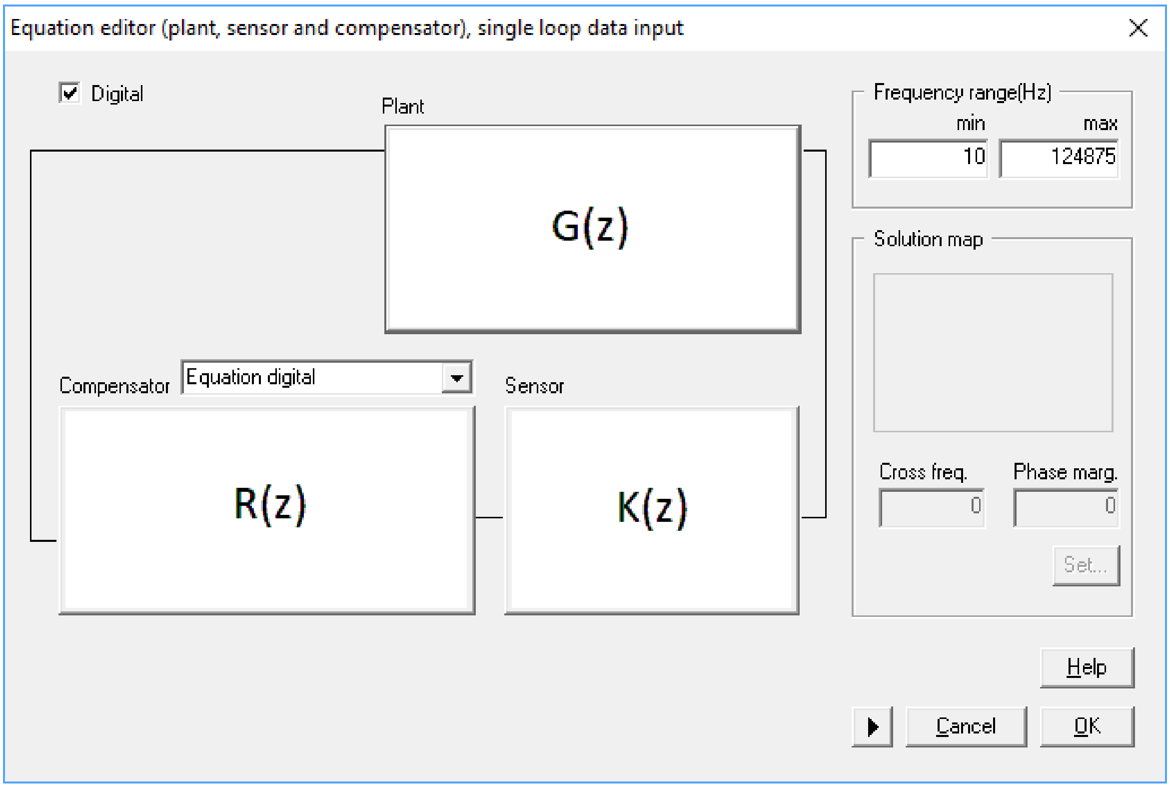
In order to design a generic control system, the definition of all the system components transfer functions is needed:

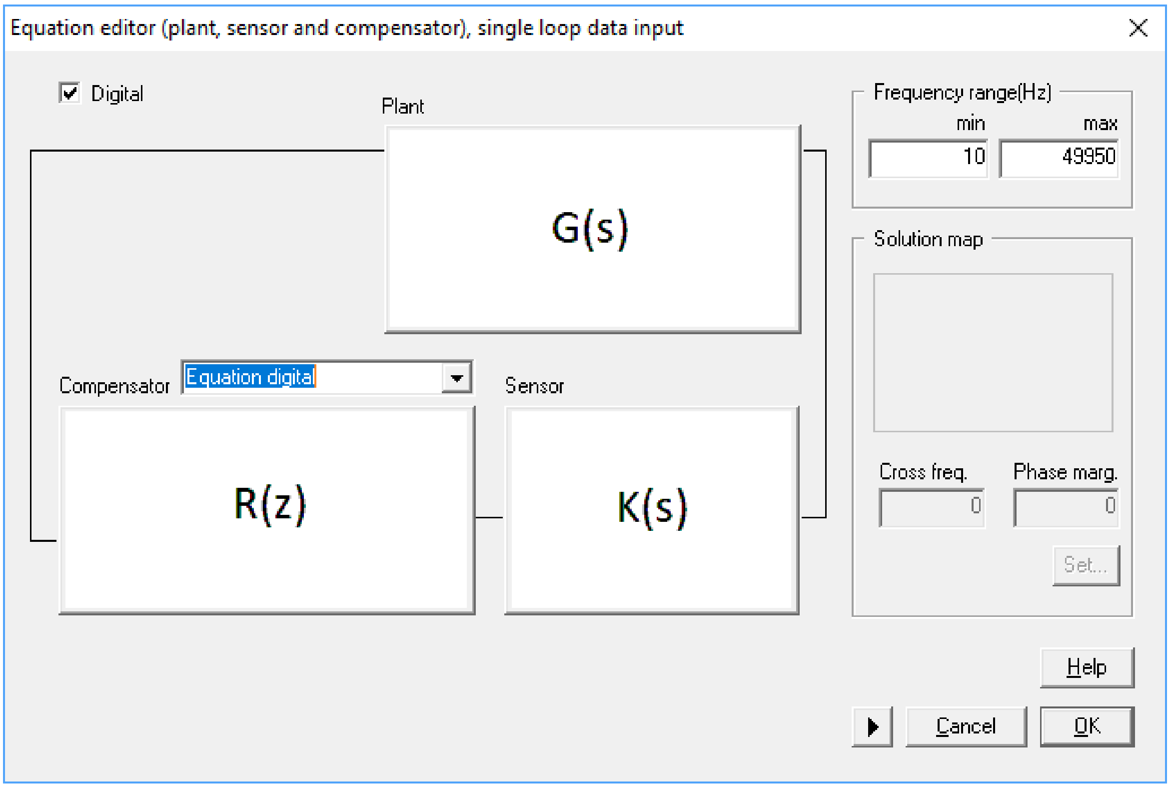
1. First the definition of the plant transfer function through the equation editor.
2. Secondly, the definition of the sensor transfer function, also through the equation editor.
3. And finally, the compensator can be selected from the predefined list to complete the definition of the system components, or customer defined using the equation editor (compensator transfer function). Please, consider in this point if the compensator is going to be designed **analog or digital,** because the options in the compensator drop-down menu will be different.


Equation editor (plant, sensor and compensator), single loop data input
Digital
Plant
G(s)
Frequency range(Hz)
min
max
10
10000000
Solution map
Compensator
Type 2
Type 3
PI
Equation
Select one from the combo
above
Sensor
K(s)
Cross freq.
Phase marg.
0
0
Set...
Help
Cancel
OK

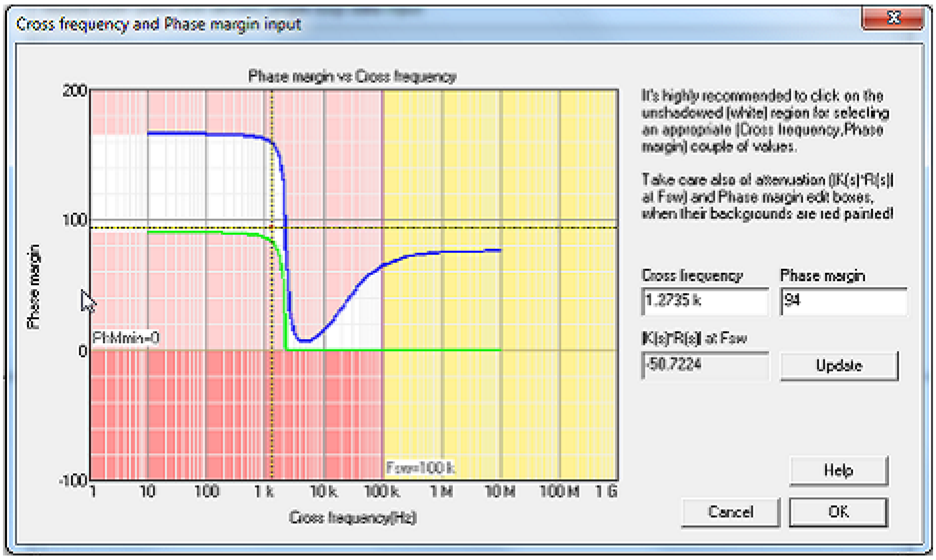

Equation editor (plant, sensor and compensator), single loop data input
Digital
Plant
G(s)
Frequency range(Hz)
min
max
10
10000000
Solution map
Compensator
PI digital
PID digital
Equation digital
loaded as yet.
Select one from the combo
above
Sensor
K(s)
Cross freq.
Phase marg.
0
0
Set...
Help
Cancel
OK

The Equation editor allows the user to work in S domain or directly in Z domain. Plant, sensor and compensator can be defined in Z Domain (Z Z Z) or Multidomain Operation, mixing S S Z or any possible combination.





The **Solutions Map** will help the user to select the phase margin and the crossover frequency, only when using a compensator from the predefined models.



1.6.1 Plant (equation editor)

Navigation: SmartCtrl > Design a generic control system >

Plant (equation editor)

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First, the user must define the transfer function of the plant, in **s-domain or in z-domain**, choosing between two different options:

Import a previous design (click on open)

Define a new transfer function (click on editor).

Additionally, there is a predefined s-domain transfer function that can be loaded by clicking on "set defaults".

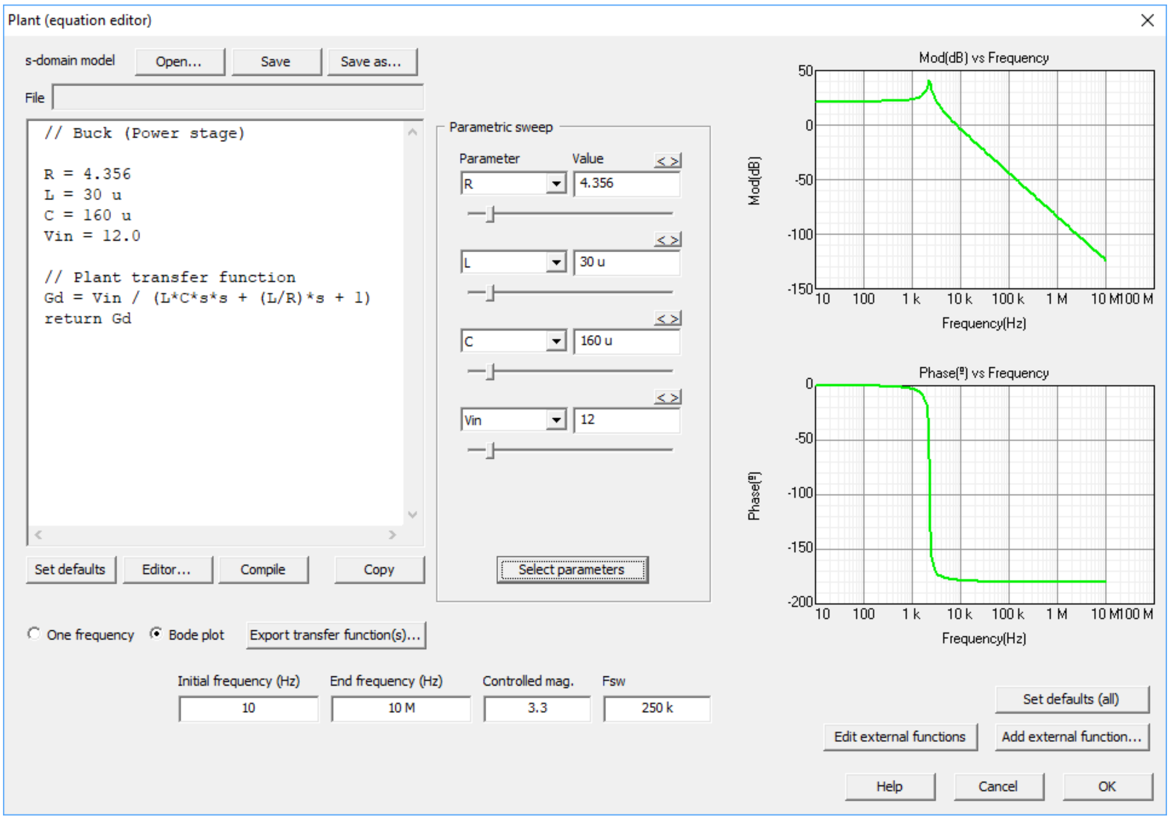
Once the equation has been introduced:

Click on "Save" to save the mathematical equations in a text file with extension .tromod

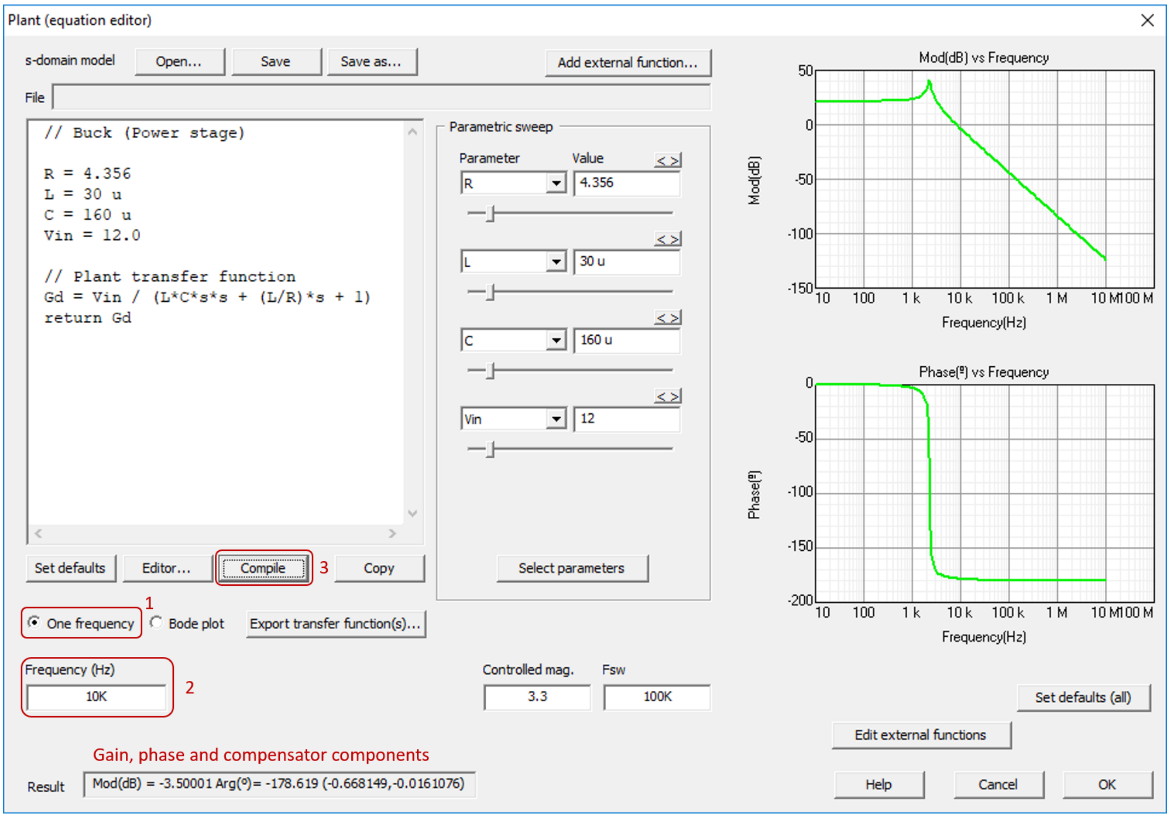
Click on "compile" to continue Bode plot will appear on the right side of the window.

If desired, the frequency response of the transfer function can be exported as a .txt file by clicking on "Export transfer function".

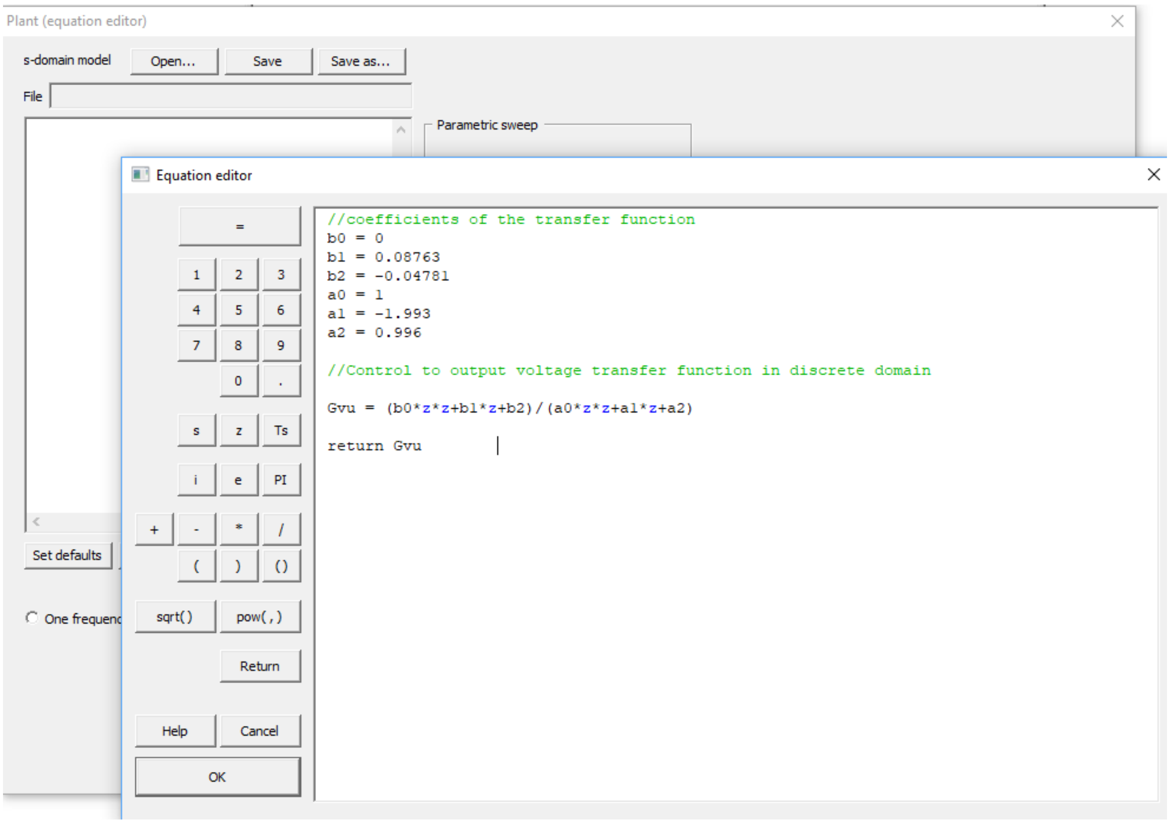
Working in S-domain or in Z-domain, "Bode plot" option is selected by default, the frequency response of the previously defined transfer function is shown on the right hand side panels.



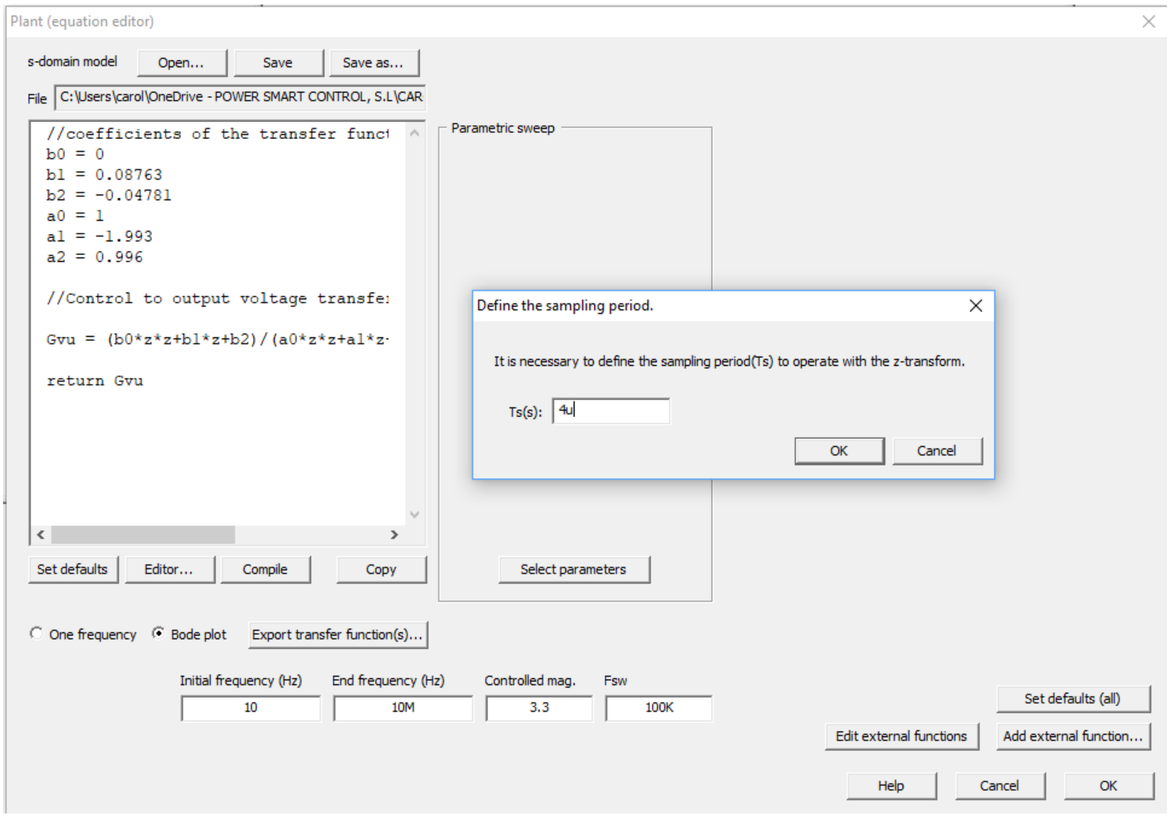
To check the gain, phase and rectangular components of the frequency response at a particular frequency, the option "One frequency" is provided. As depicted in the following figure: first **"one frequency"** must be selected, secondly the frequency should be specified and finally, click on compile and the gain, phase and rectangular components at the specified frequency are shown below.



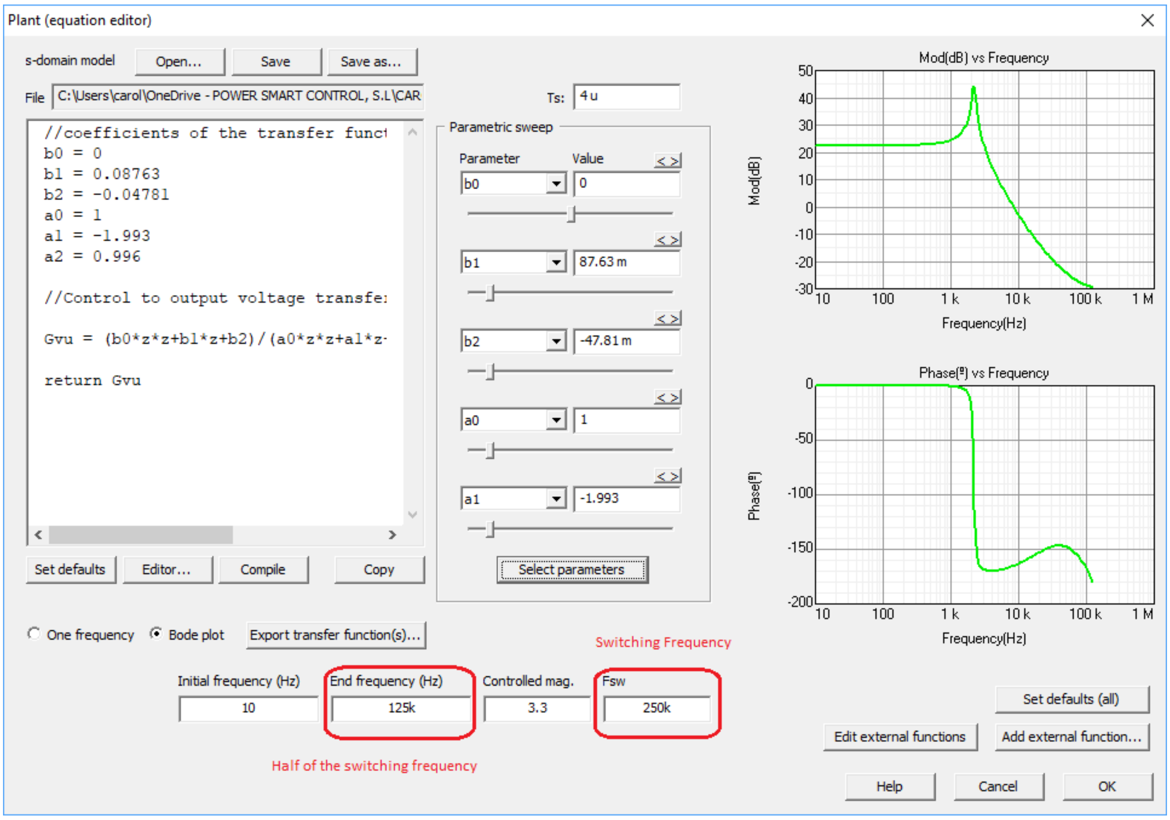
In case the user define the plant transfer function in **Z-domain** it is necessary to enter the sampling period (Ts).
If we define a new transfer function using the Editor:



Once we click on "compile", SmartCtrl will request the user to define the sample period, Ts.



After the user inserts the switching frequency, in the "end frequency" box the user should enter the Nyquist rate that corresponds to half of the switching frequency.



If the **"Select parameters"** button is clicked, the program detects the numerical parameters and allows the user to vary them with the sliders that appear in the figure above, in this way the frequency response can be analyzed as the parameters are varied.

1.6.2 Sensor (equation editor)

Navigation: SmartCtrl > Design a generic control system >

Sensor (equation editor)

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The transfer function of the sensor can be defined in **s-domain or in z-domain**, choosing between two different options:

Import a previous design (click on open)

Define a new transfer function (click on editor).

Additionally, there is a predefined transfer function that can be loaded by clicking on "set defaults".

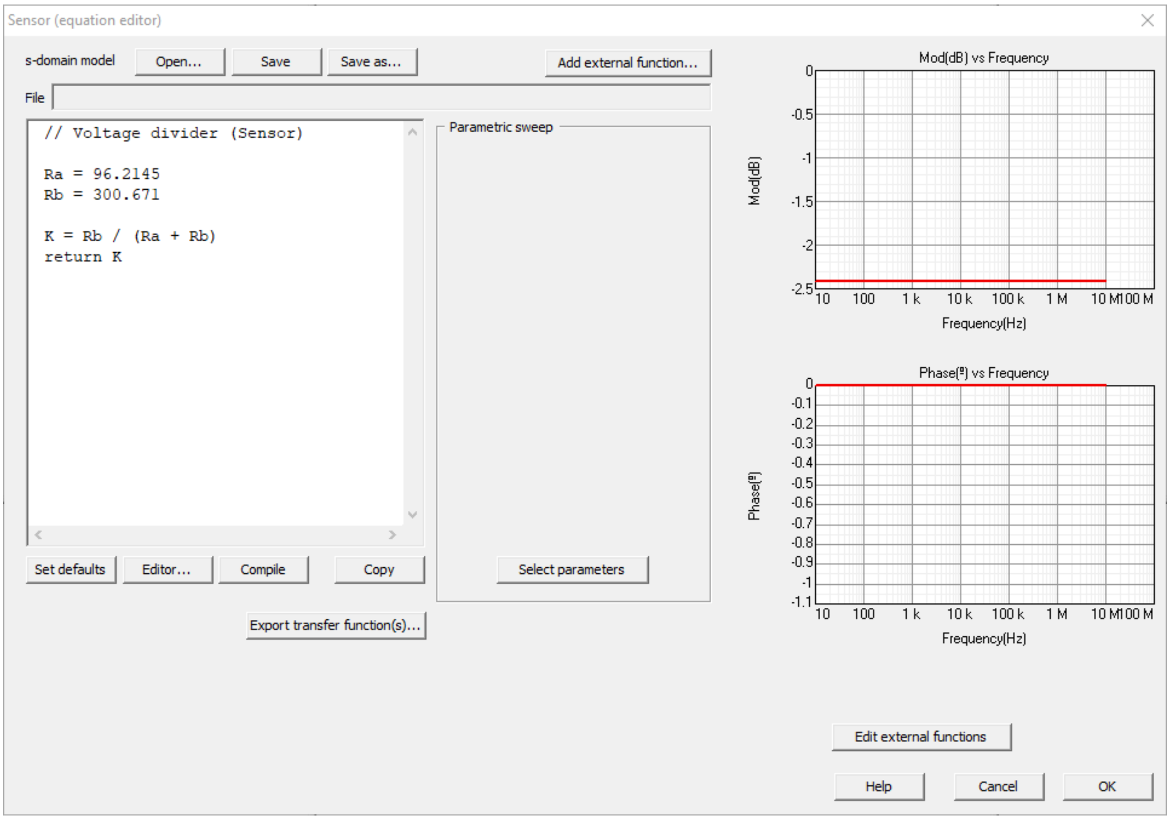
Once the equation has been introduced:

Click on "Save" to save the mathematical equations in a text file with extension .tromod

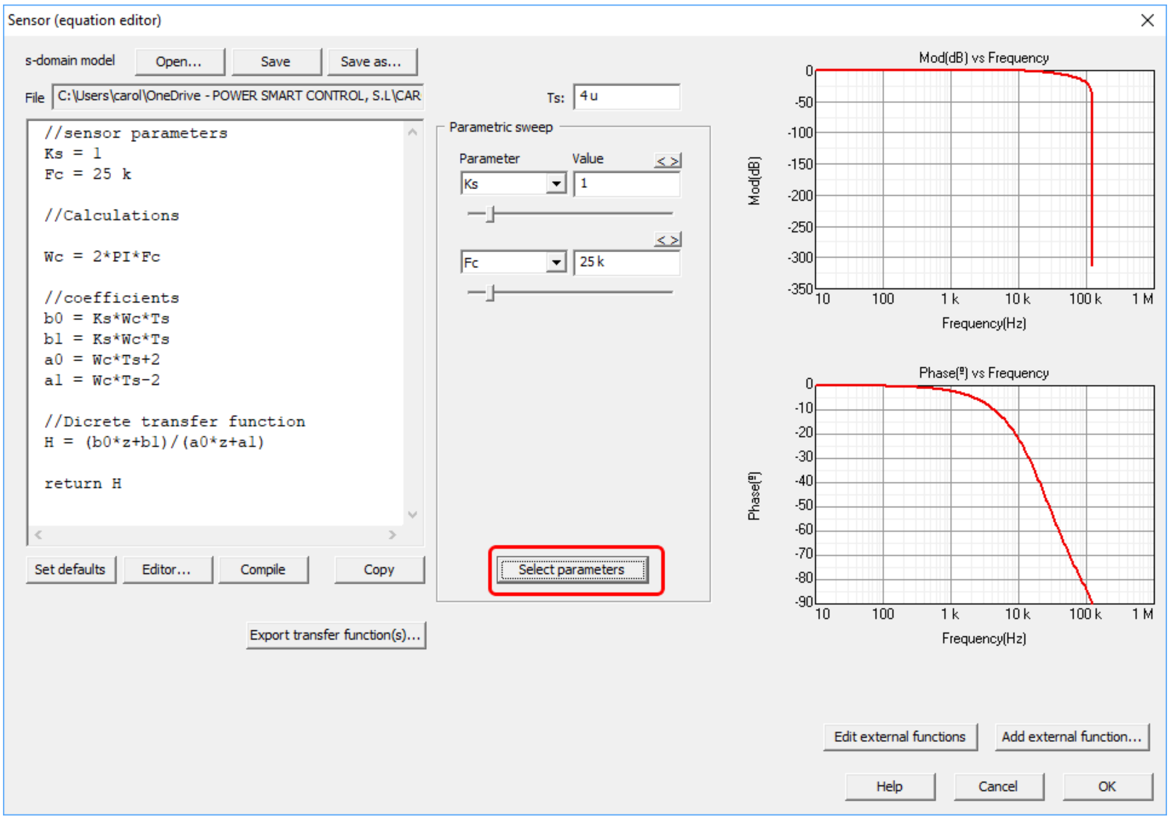
Click on "compile" to continue Bode plot will appear on the right side of the window.

If desired, the frequency response of the transfer function can be exported as a .txt file by clicking on "Export transfer function".

Working in S-domain or in Z-domain, the frequency response of the defined transfer function is shown on the right hand side panels.



Working in **Z-domain**, the sampling period that appears in the figure below, it is the same defined in the plant section. If the user wants to change the value of Ts, it can be done in this part of the design or later, since it will be updated for all the sections (Plant, Sensor and Compensator).



If the **"Select parameters"** button is clicked, the program detects the numerical parameters and allows the user to vary them with the sliders that appear in the figure above, in this way the frequency response can be analyzed as the parameters are varied.

1.6.3 Compensator (equation editor)

Navigation: SmartCtrl > Design a generic control system >

Compensator (equation editor)

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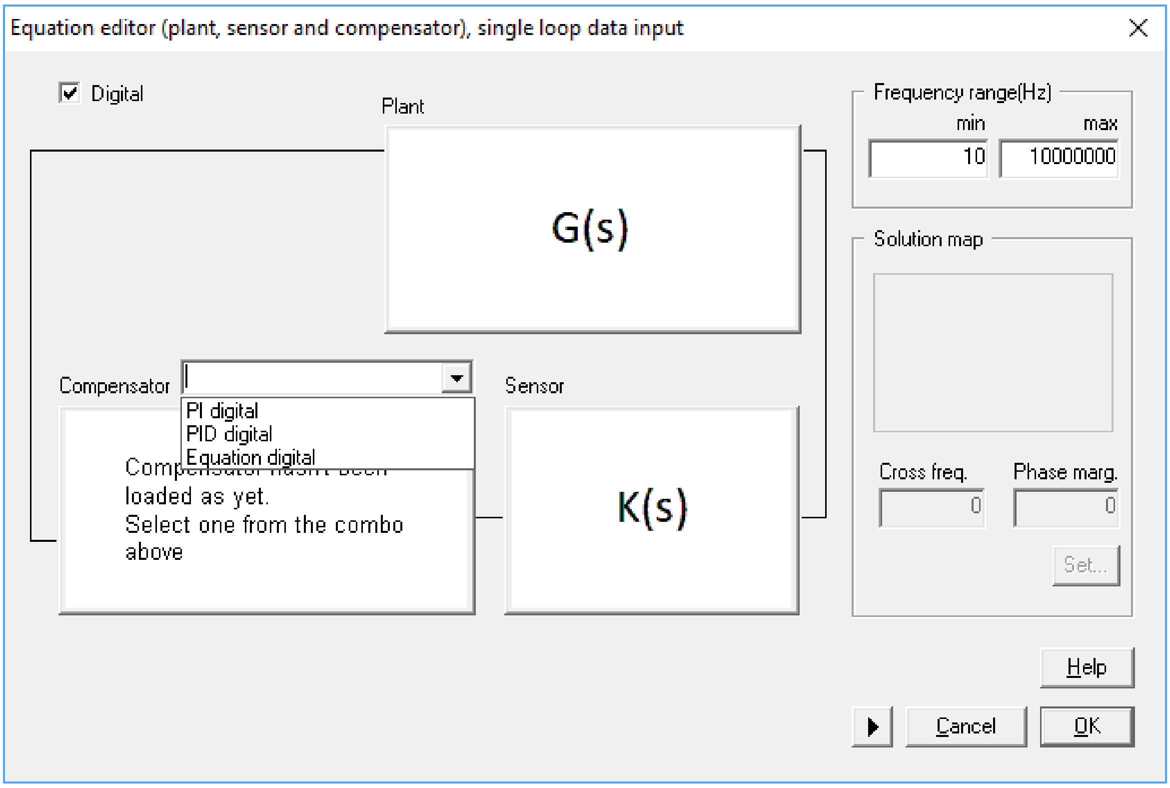
When designing a generic control system, the compensator can be selected among different predefined options or it can be customer designed in S-domain or in Z-domain.

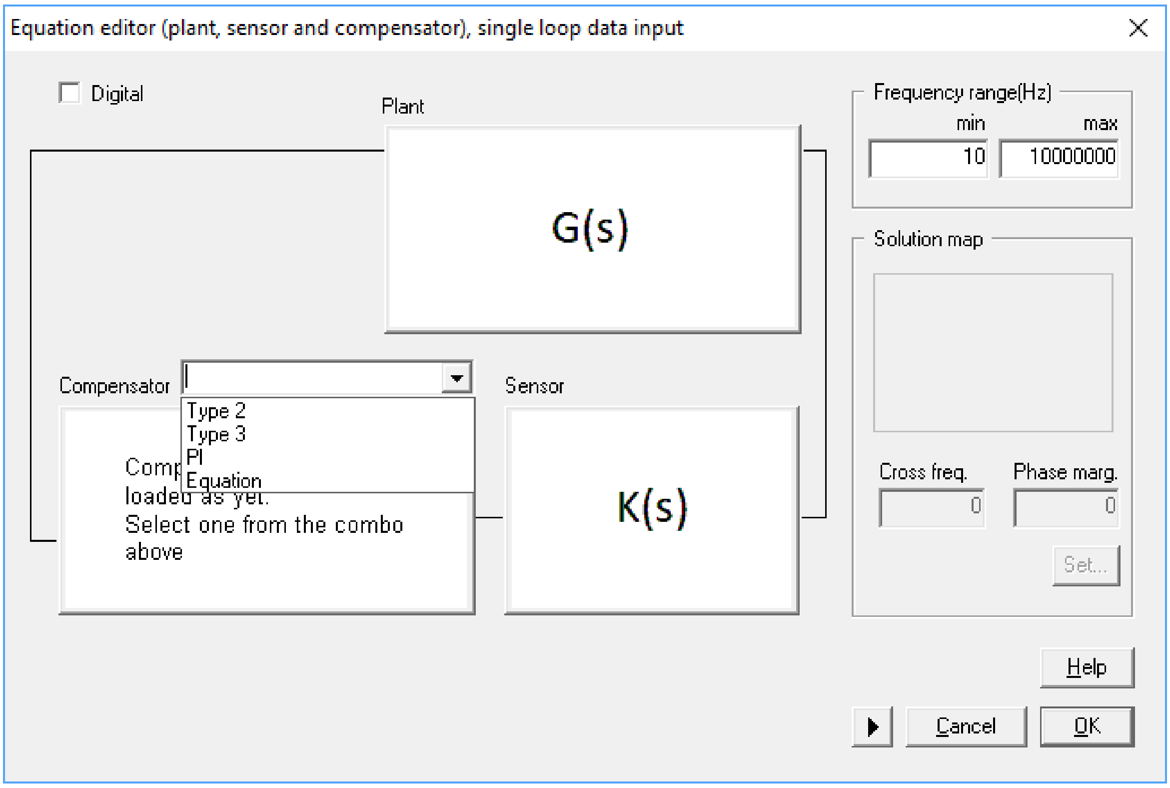
The following analog compensators are available:

- Type 2
- Type 3
- PI
- Customer defined using the Equation editor

The following digital compensators are available:

•PI Digital
•PID Digital
•Customer defined using the Equation editor





Once the option "Equation" or "Equation Digital" has been selected for the compensator definition just follow next steps.

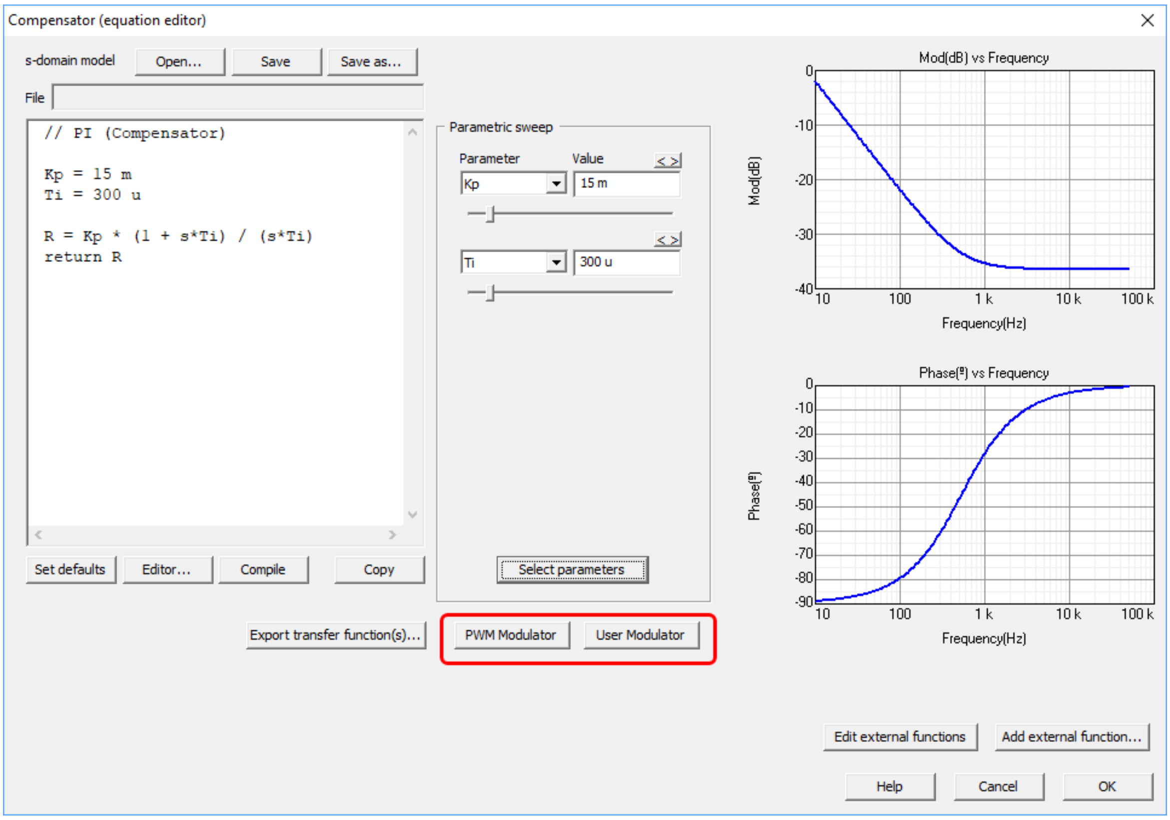
The transfer function of the user defined compensator can be defined choosing between two different options:

- Import a previous design (click on open)
- Define a new transfer function (click on editor).
- Additionally, there is a predefined transfer function that can be loaded by clicking on "set defaults".

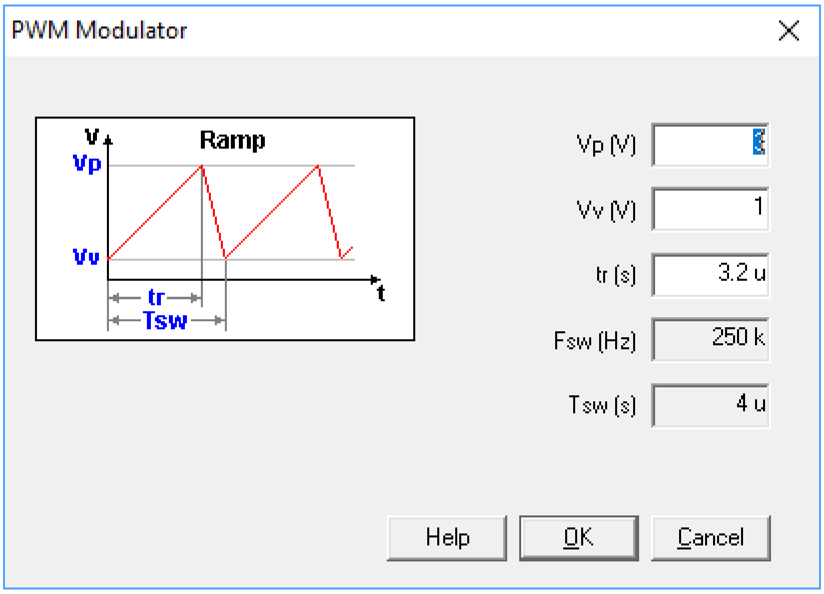
Once the equation has been introduced:

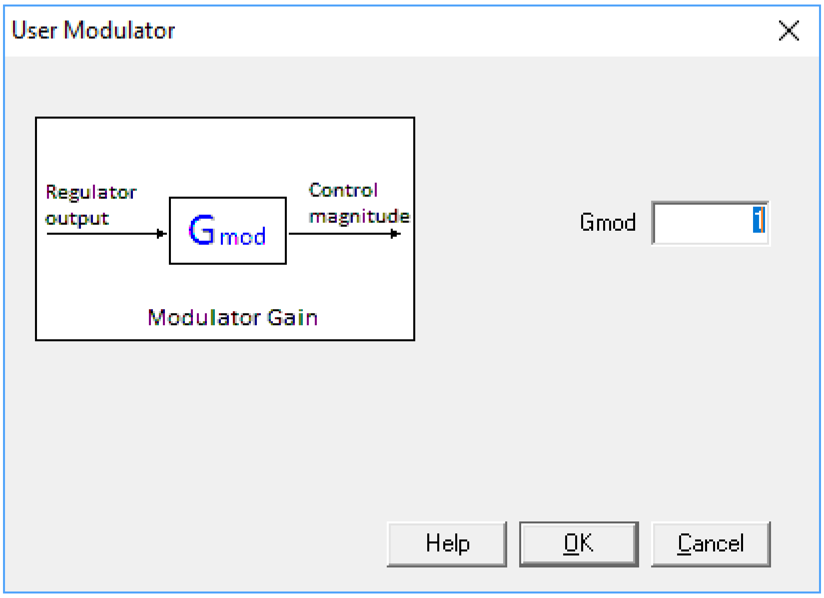
- Click on "Save" to save the mathematical equations in a text file with extension .tromod
- Click on "compile" to continue Bode plot will appear on the right side of the window.
- If desired, the frequency response of the transfer function can be exported as a .txt file by clicking on "Export transfer function".

Working in **S-domain**, the frequency response of the previously defined transfer function is shown on the right hand side panels.

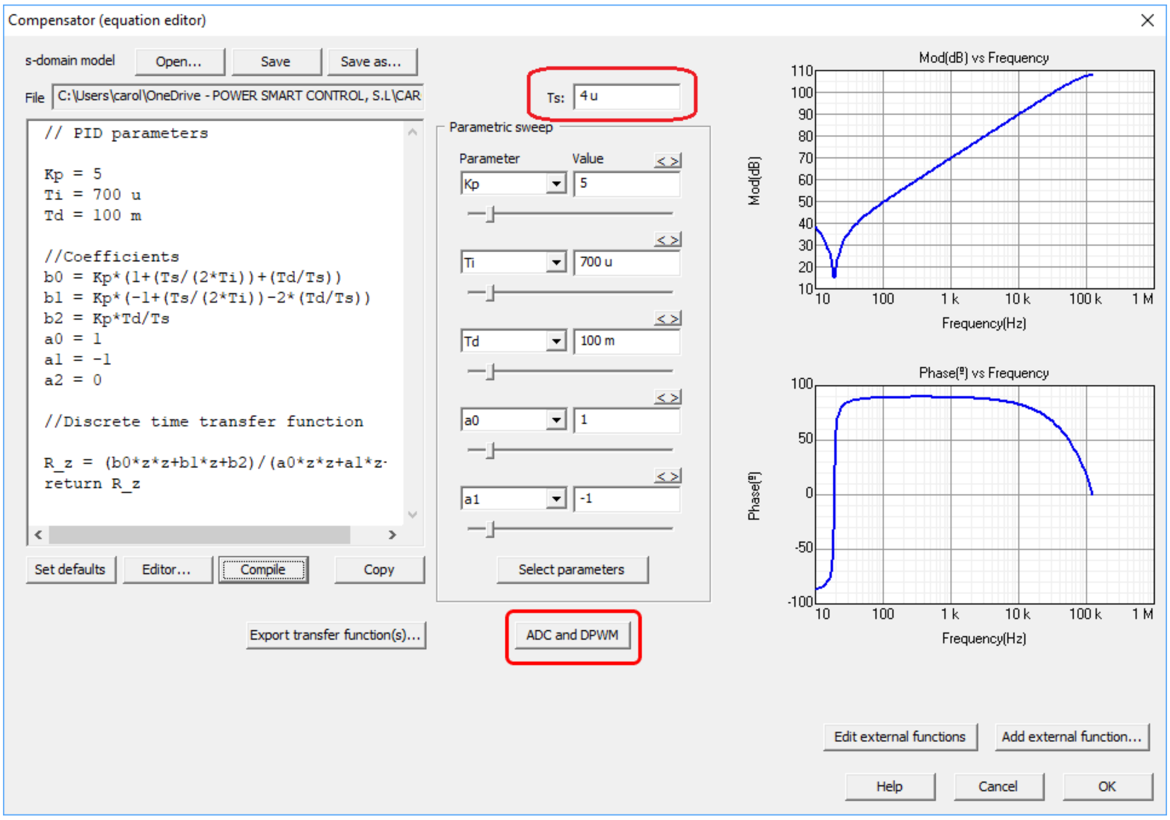


For **analog user defined compensator** note that the user should define here the [PWM Modulator] parameters or [User defined Modulator gain].



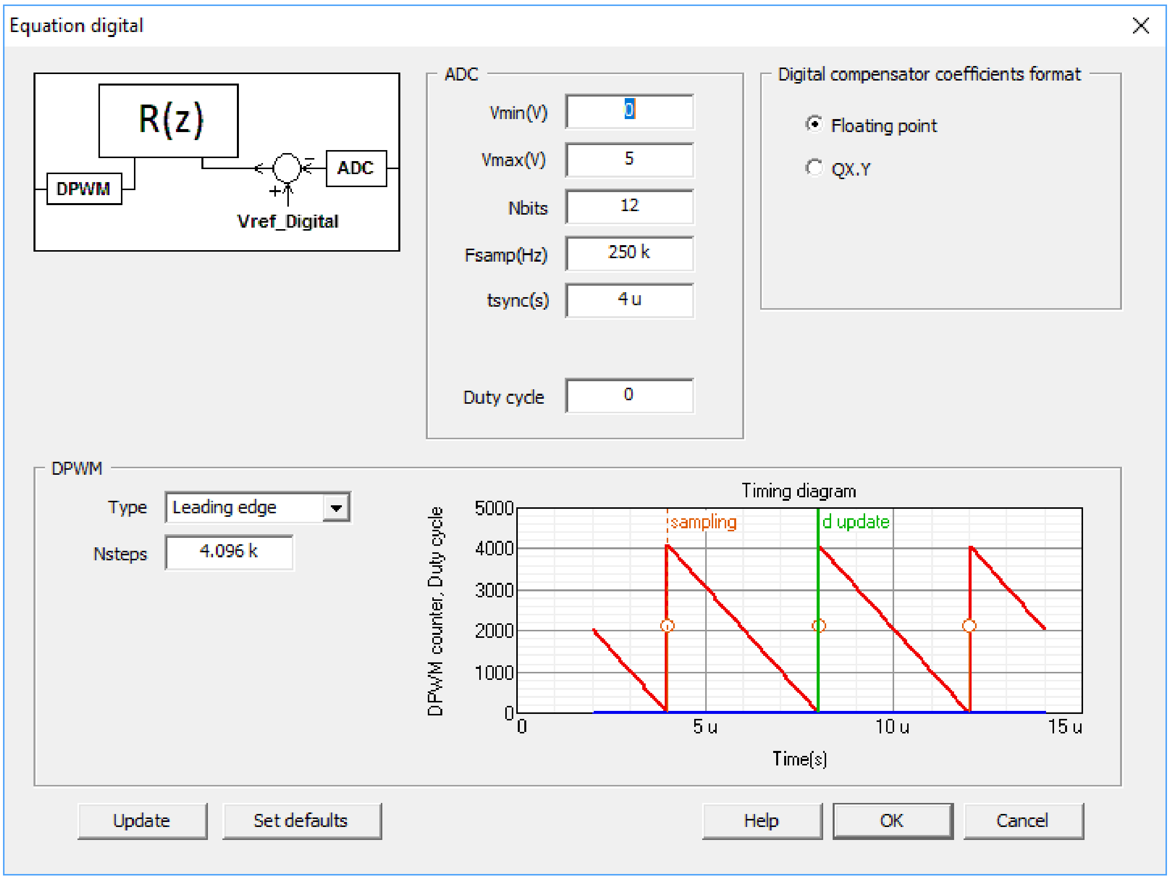


Working in **Z-domain**, the sampling period that appears in the figure below, it is the same defined in the plant and in the sensor section (in case of using z-domain discrete functions for both). If the user wants to change the value of **Ts**, it can be done in this part of the design or later, since it will be updated for all the sections (Plant, Sensor and Compensator).

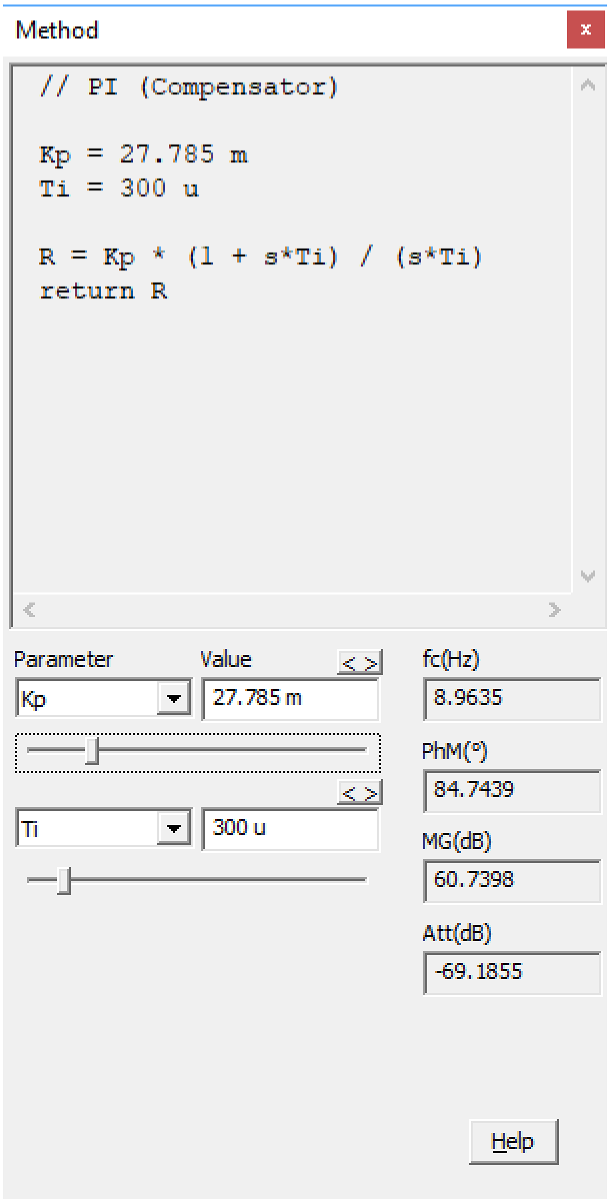


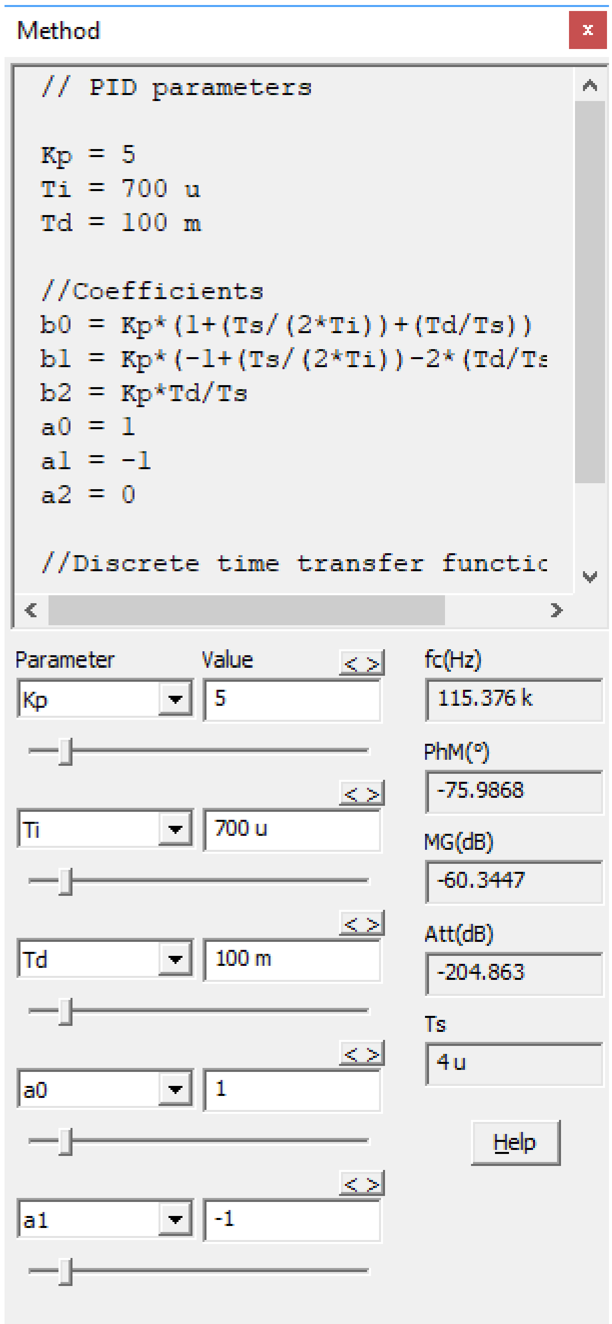
If the **"Select parameters"** button is clicked, the program detects the numerical parameters and allows the user to vary them with the sliders that appear in the figure above, in this way the frequency response can be analyzed as the parameters are varied.

Working in Z-domain, if the digital delay was not considered in the transfer function that was determined above, it is important to enter it in the **"ADC and DPWM"** option to review the default parameters, more information in Digital Control.



For user defined compensators, in S-domain or in Z-domain, using the equation editor, the solutions map is not available, use the compensator parameter sweep available in the Method box instead.


Method
// PI (Compensator)
Kp = 27.785 m
Ti = 300 u
R = Kp * (1 + s*Ti) / (s*Ti)
return R
Parameter
Value
Kp
27.785 m
Ti
300 u
fc(Hz)
8.9635
PhM(º)
84.7439
MG(dB)
60.7398
Att(dB)
-69.1855
Help



1.7 DC-DC Plants

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DC-DC Plants

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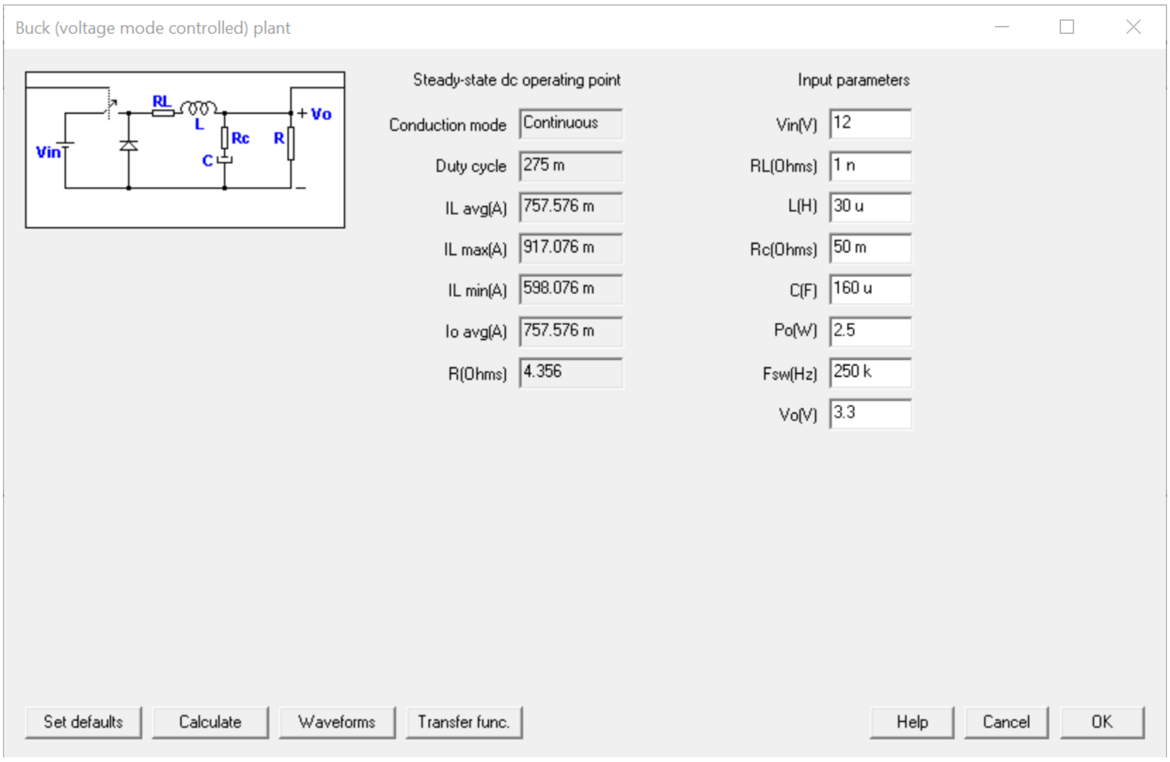
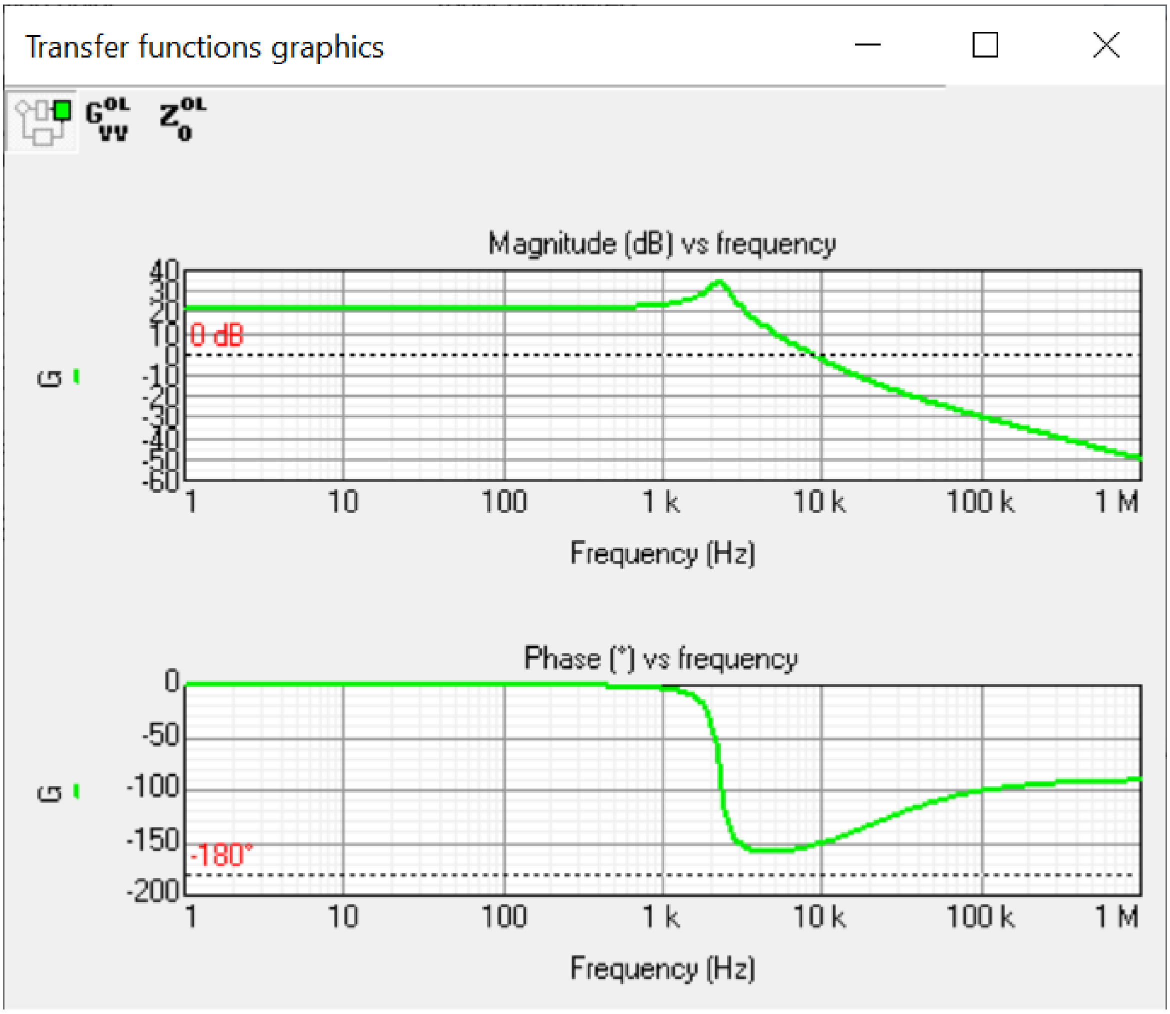
For every DC-DC converter, the input data window allows the user to select the desired input parameters and also provides useful information such as the steady state dc operating point, waveforms and the transfer function.
For any of the considered DC-DC topologies, the input data correspond to the white shadowed boxes, and the additional information provided by the program will be shown in the grey shadowed boxes.

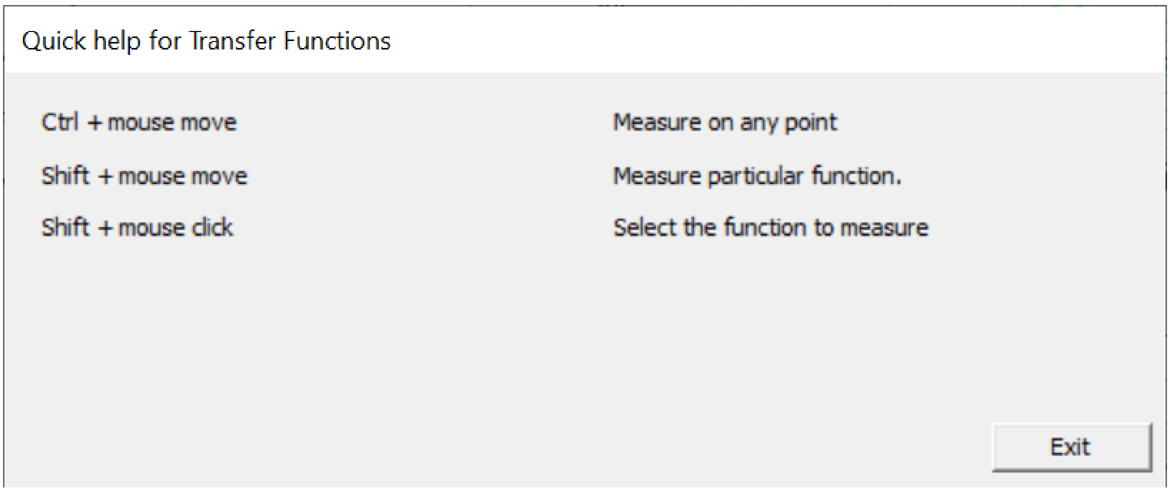
Let´s consider any of the available converters. In the following picture it can be seen that the parameters which define the steady-state dc operating point are shown in grey as they are calculated parameters. Depending on the topology considered in each case, some of them will be input data and some others will be output data.



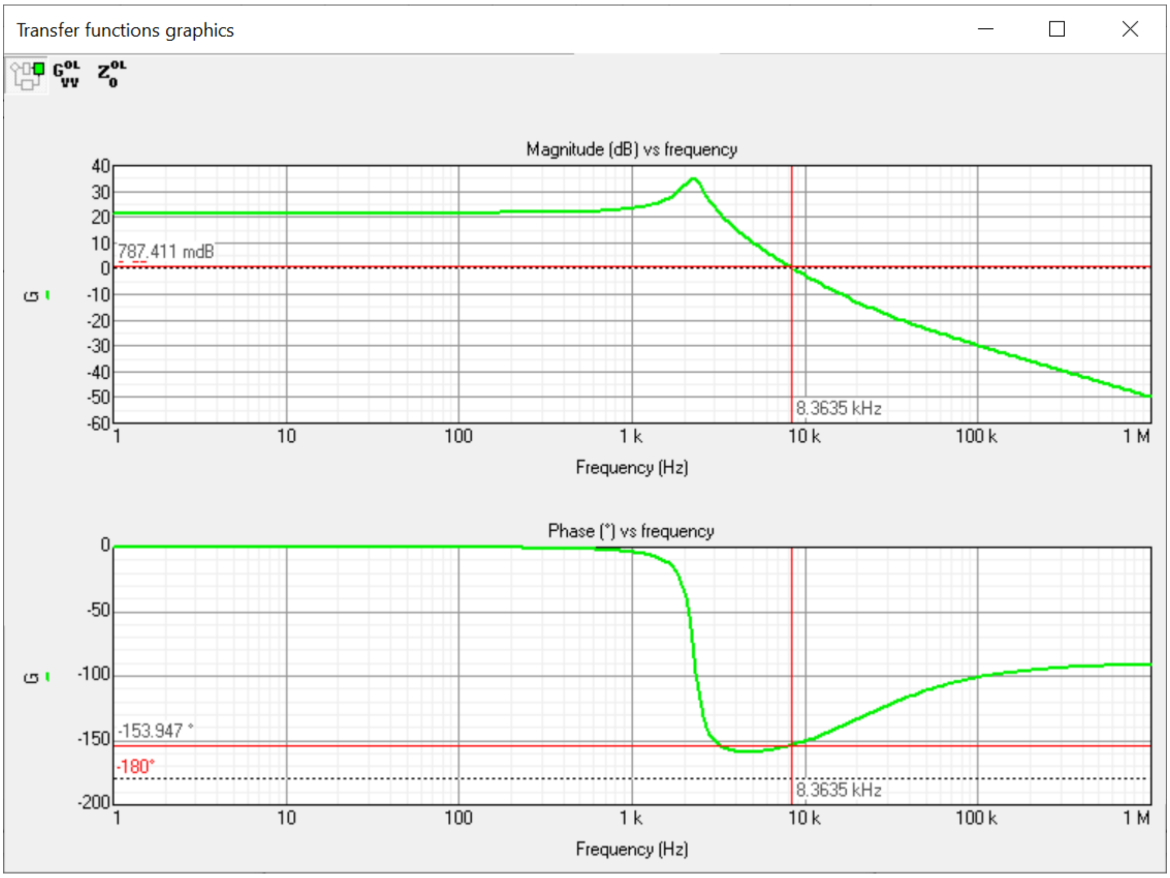
Selecting the "**Transfer func**." button the user gets the transfer functions in open loop available for the topology:



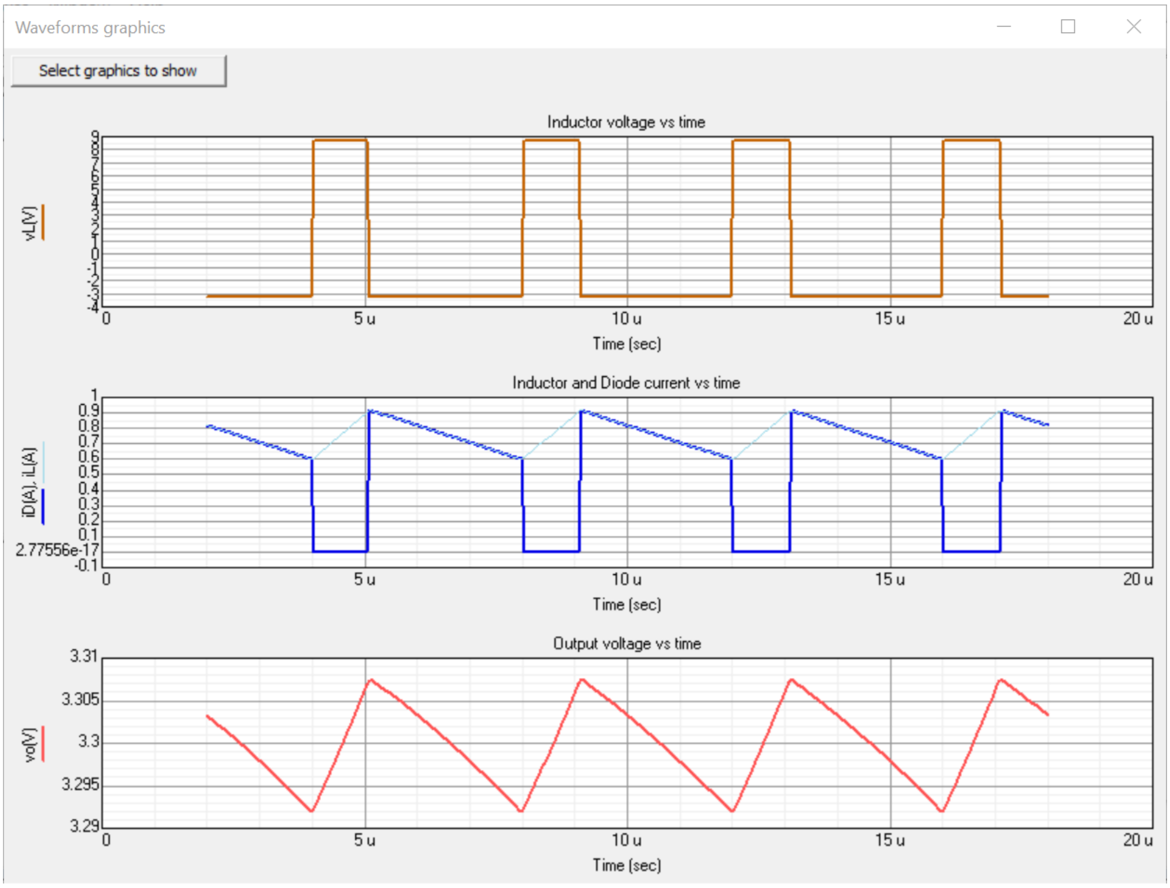
Right clicking on the Transfer Functions graphics panel, the user can access a quick help menu shown below.



The Transfer function graphics panel is resizable and with the user can measure any point with the cursors.



Selecting the "**Waveforms**" button the user gets the main waveforms in open loop available for the topology:



Right clicking on the Waveforms panel, the user can access a quick help menu showing how to manage the cursors, the same functionality as in the Transfer Function Graphics panel.
These options are available for all the available plants.

The **DC-DC available plants** are the following:
[Buck]
[Boost]
[Buck-Boost]
[Flyback]
[Forward]
- [Phase Shifted Full Bridge (VMC RL)]
- [Phase Shifted Dual Active Bridge (VMC RL - V1 to V2)]
- [Phase Shifted Dual Active Bridge (VMC ERL - V1 to V2)]
- [Phase Shifted Dual Active Bridge (CS ERL - V1 to V2)]

1.7.1 Buck

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Buck

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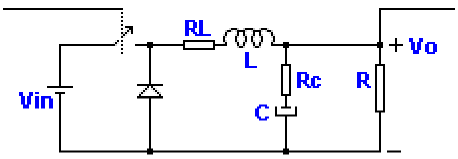
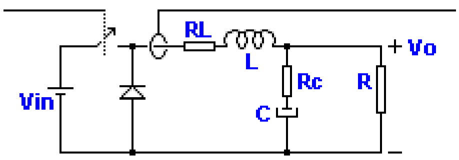
When a single loop control scheme is used, the magnitude to be controlled in a buck converter can be either the output voltage or the inductance current. If the control technique is a peak current mode control, the current is sensed in the inductor, as shown in the table. The schematics are shown below:

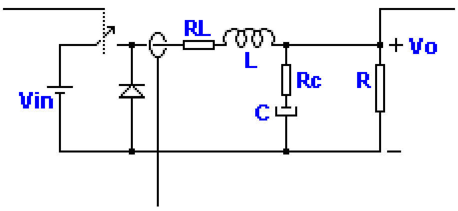


Voltage Mode Controlled Buck



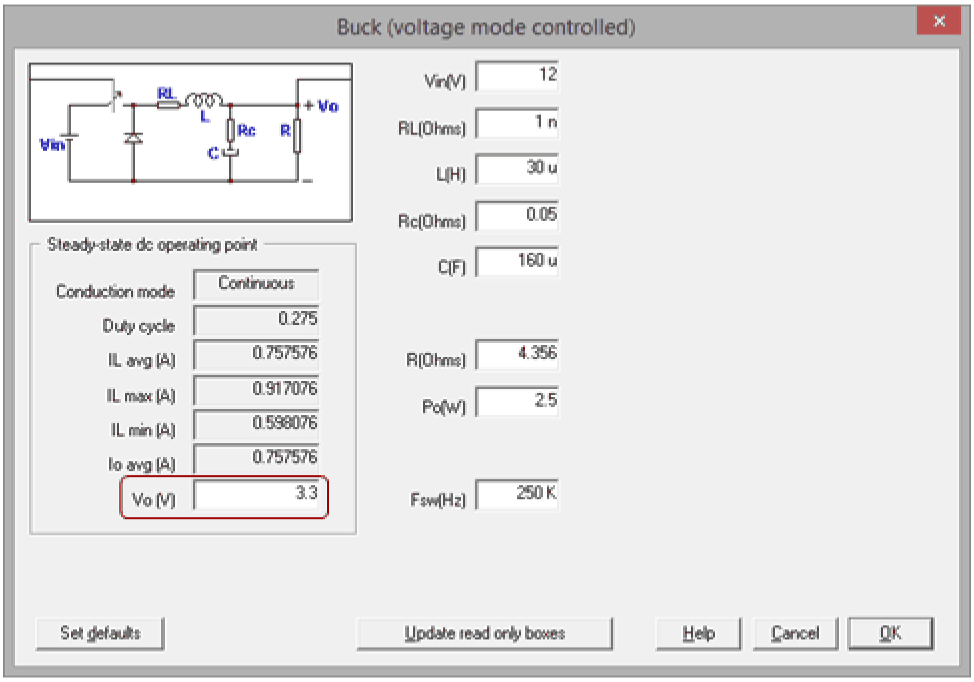
L-Current Sensed Buck
Peak current mode control

In the case of an **average current control scheme**, two magnitudes must be sensed simultaneously, a current and the output voltage. The resultant buck scheme is the following:

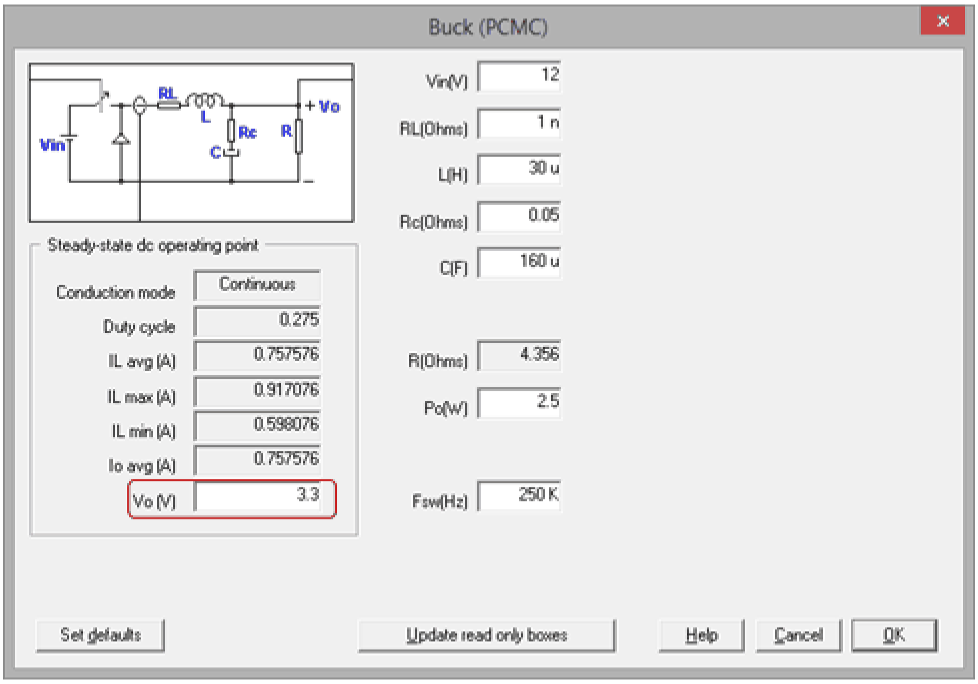


Buck (LCS-VMC)

The **input data window** allows the user to select the desired input parameters and provides useful information such as the **steady state dc operating point**. This information is placed right below the converter image.
Two examples of the input data window are shown below, in each of them, the white shadowed boxes correspond to the input data boxes while the grey shadowed ones correspond to the additional information provided by the program.
Please, note that the input data is different in case of a voltage controlled plant (output voltage is an input) or a current controlled plant (in this case the current to be controlled is the input data). An example of the input data windows is provided below:



Input Data Window of a Voltage Mode Controlled Buck
Input Data Window of a Peak Current Mode Control.



Input Data Window of a Current Mode Controlled Buck

The parameters shown in the input data windows are defined below:

Steady-state dc operating point

Conduction Mode It can be Continuous or Discontinuous

Duty Cycle t_{on}/T of the active switch
IL avg Inductance average current (A)
IL max Maximum value of the inductance switching ripple (A)
IL min Minimum value of the inductance switching ripple (A)
Io avg Output average current (A)
Vo Output voltage (V)

Other parameters of the converter

V_{in} Input Voltage (V)
R_L Equivalent Series Resistor of the Inductance (Ohms)
L Inductance (H)
R_c Equivalent Series Resistor of the output capacitor (Ohms)
C Output Capacitor (F)
R Load Resistor (Ohms)
P_o Output Power (W)
F_{SW} Switching frequency (Hz)

1.7.2 Boost

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Boost

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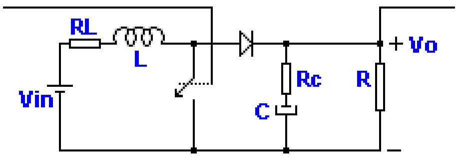
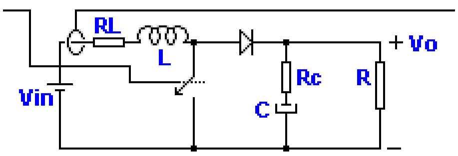
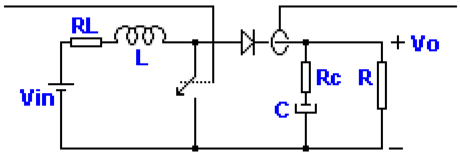
There are three possible magnitudes to be controlled in the boost converter when a **single loop control scheme** is selected. This is the output voltage, the inductor current and the diode current. The corresponding schematics are the following:



Voltage Mode Controlled Boost Converter

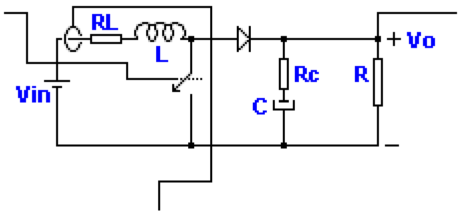


L-current sensed Boost Converter



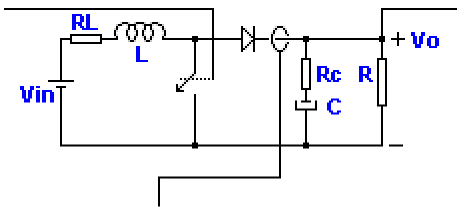
Diode Current Sensed Boost Converter

In the case of a **peak current mode control (PCMC)**, the output voltage and a current must be sensed simultaneously.

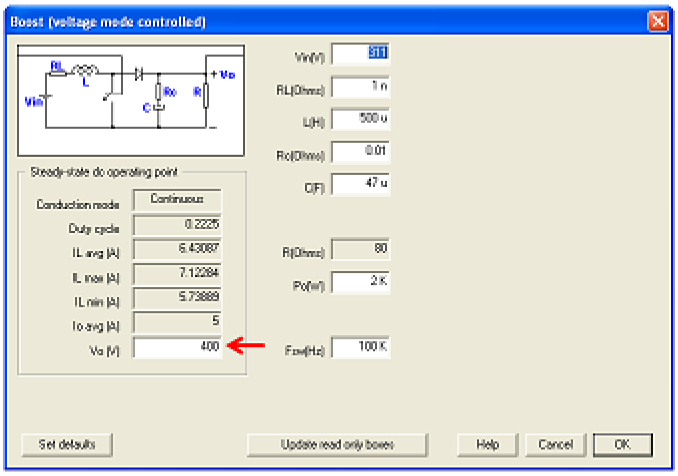


Boost (PCMC)

In the case of an average current control scheme, the output voltage and a current must be sensed simultaneously. The available plants for an average current mode control are included below:

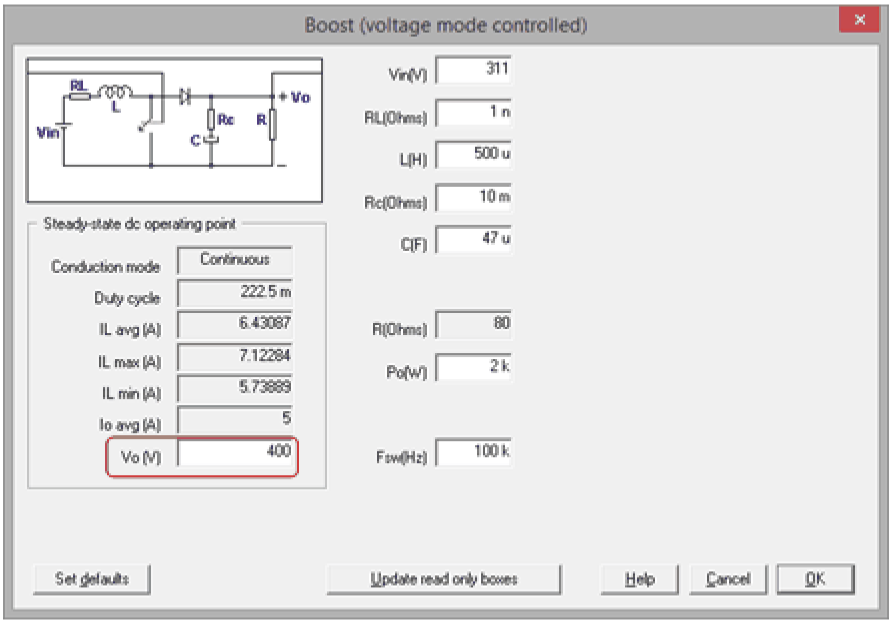


Boost (LCS-VMC)

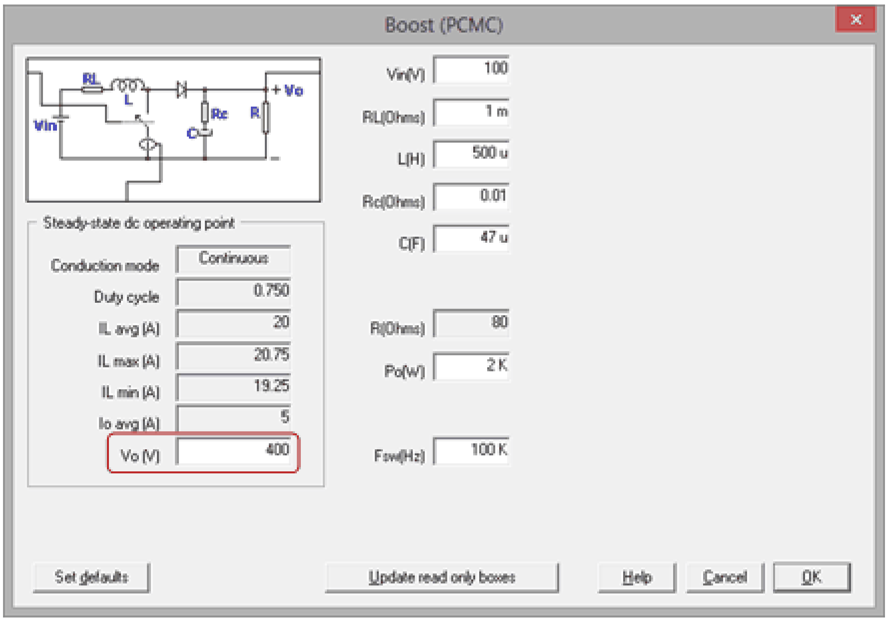


Boost (DCS-VMC)

The **input data window** allows the user to select the desired input parameters and provides useful information such as the **steady state dc operating point**. This information is placed right below the converter image.
Two examples of the input data window are shown below, in each of them, the white shadowed boxes correspond to the input data boxes while the grey shadowed ones correspond to the additional information provided by the program.
Please, note that the input data is different in case of a voltage controlled plant (output voltage is an input) or a current controlled plant (in this case the current to be controlled is the input data). An example of the input data windows is provided below:



Input Data Window of a Voltage Mode Controlled Boost and of a Peak Current Mode Control.



Input Data Window of a Current Mode Controlled Boost

The parameters shown in the input data windows are defined below:

Steady-state dc operating point

Conduction Mode It can be Continuous or Discontinuous
Duty Cycle t_{on}/T of the active switch
IL avg Inductance average current (A)
IL max Maximum value of the inductance switching ripple (A)
IL min Minimum value of the inductance switching ripple (A)
Io avg Output average current (A)
Vo Output voltage (V)

Other parameters of the converter

V_{in} Input Voltage (V)
R_L Equivalent Series Resistor of the Inductance (Ohms)
L Inductance (H)
R_c Equivalent Series Resistor of the output capacitor (Ohms)
C Output Capacitor (F)
R Load Resistor (Ohms)
P_o Output Power (W)
F_{SW} Switching frequency (Hz)

1.7.3 Buck-boost

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Buck-boost

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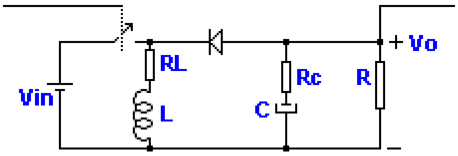
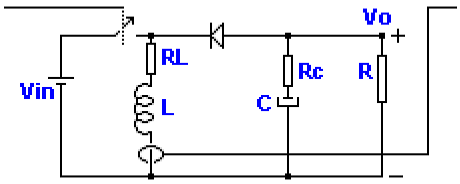
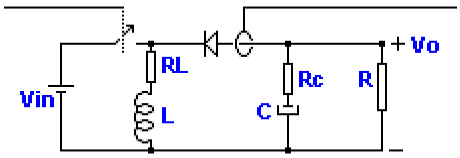
In a **single loop** control scheme there are three possible magnitudes to be controlled in the buck-boost converter. This is the output voltage, the inductor current and the diode current. The respective schematics are the following:



Voltage Mode Controlled Buck-Boost Converter

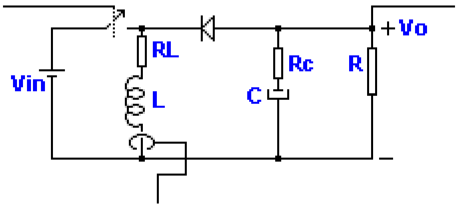


L-current sensed Buck-Boost Converter



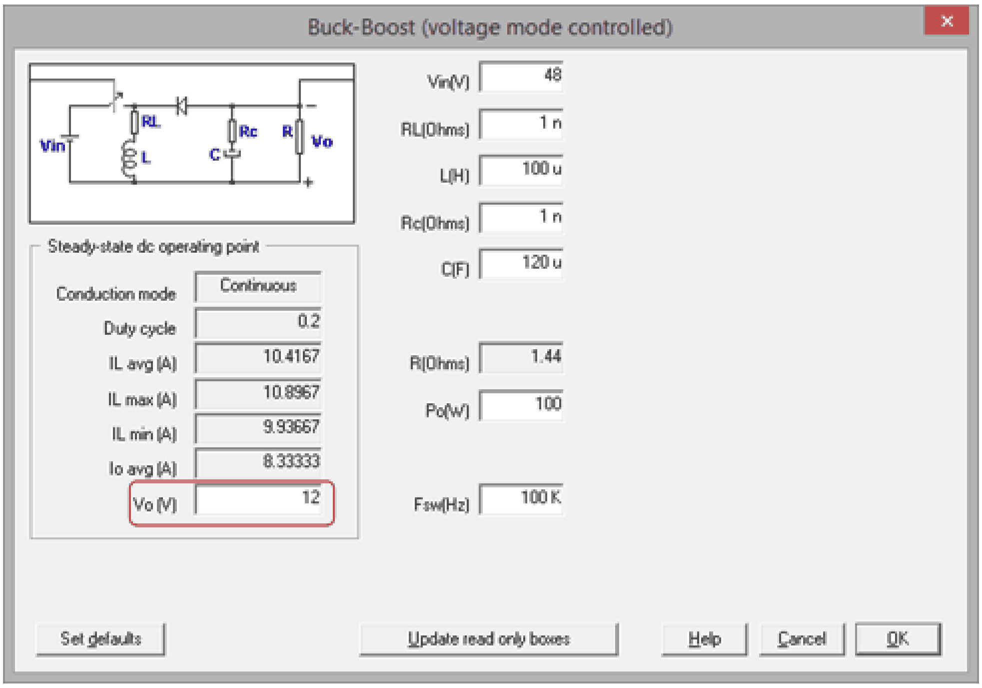
Diode Current Sensed Buck-Boost Converter

In the case of a **average current mode** control scheme and the case of **peak current mode control (PCMC)**, the magnitudes sensed are the output voltage and the L current.

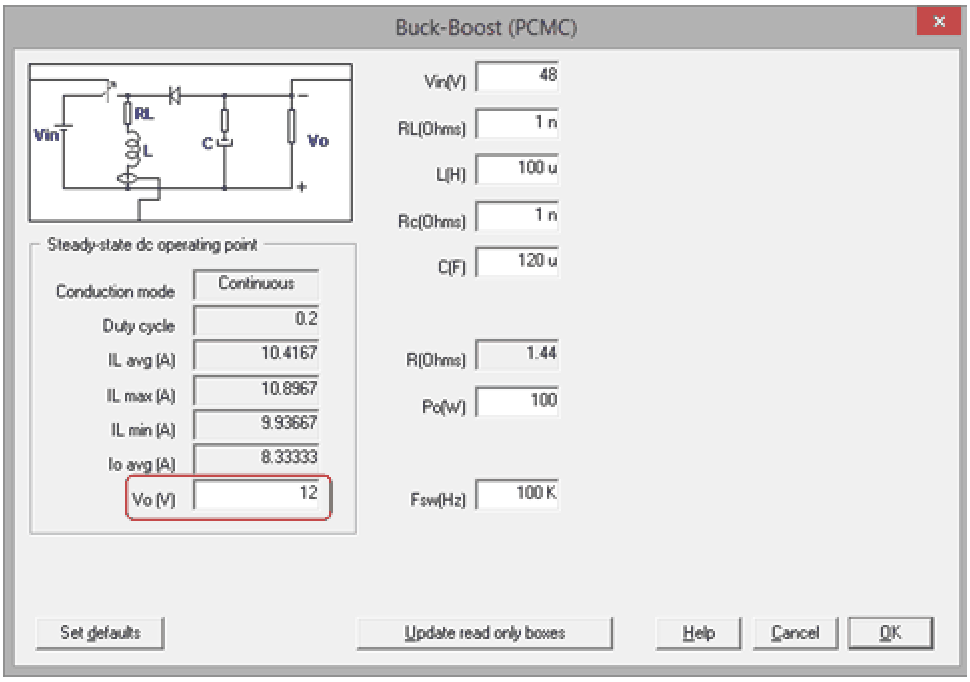


Buck-Boost (LCS-VMC)
Buck-Boost (PCMC)

The **input data window** allows the user to select the desired input parameters and provides useful information such as the **steady state dc operating point**. This information is placed right below the converter image.
Two examples of the input data window are shown below, in each of them, the white shadowed boxes correspond to the input data boxes while the grey shadowed ones correspond to the additional information provided by the program.
Please, note that the input data is different in case of a voltage controlled plant (output voltage is an input) or a current controlled plant (in this case the current to be controlled is the input data). An example of the input data windows is provided below:



Input Data Window of a Voltage Mode Controlled Buck-Boost and for a Buck-Boost with a Peak Current Mode Control



Input Data Window of a Current Mode Controlled Buck-Boost

The parameters shown in the input data windows are defined below:

Steady-state dc operating point

Conduction Mode It can be Continuous or Discontinuous

Duty Cycle t_{on}/T of the active switch
IL avg Inductance average current (A)
IL max Maximum value of the inductance switching ripple (A)
IL min Minimum value of the inductance switching ripple (A)
Io avg Output average current (A)
Vo Output voltage (V)

Other parameters of the converter

- V_{in} Input Voltage (V)
- R_L Equivalent Series Resistor of the Inductance (Ohms)
- **L** Inductance (H)
- R_c Equivalent Series Resistor of the output capacitor (Ohms)
- **C** Output Capacitor (F)
- **R** Load Resistor (Ohms)
- P_o Output Power (W)
- F_{SW} Switching frequency (Hz)

1.7.4 Flyback

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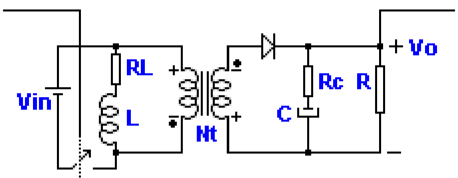
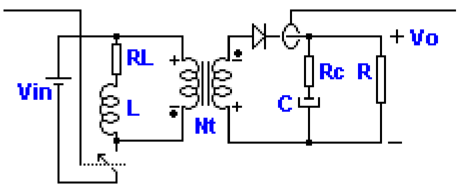
Flyback Previous Top Next

In a **single loop** control scheme, the magnitude to be controlled in a Flyback converter can be either the output voltage or the diode current. Both possibilities have been included in SmartCtrl. The schematics are shown below:

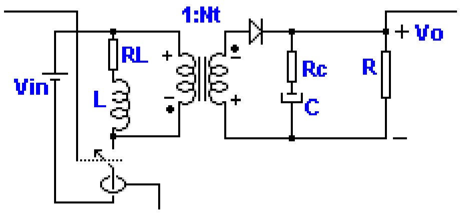


Voltage Mode Controlled Flyback



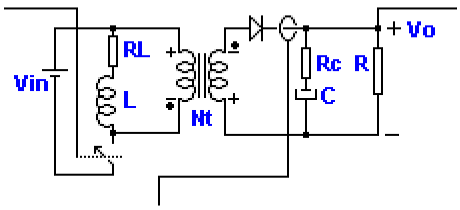
Diode Current Sensed Flyback

In the case of a **peak current mode control** scheme (PCMC), the magnitudes sensed are the output voltage and the MOSFET's current.



Flyback (PCMC)

In the case of a **average current mode** control scheme, the magnitudes sensed are the output voltage and the diode current.

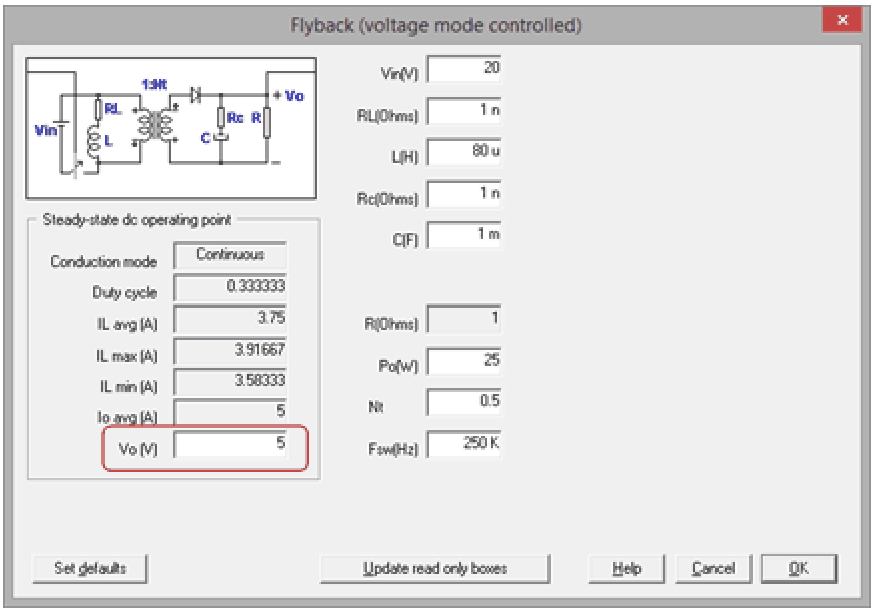


Flyback (DCS-VMC)

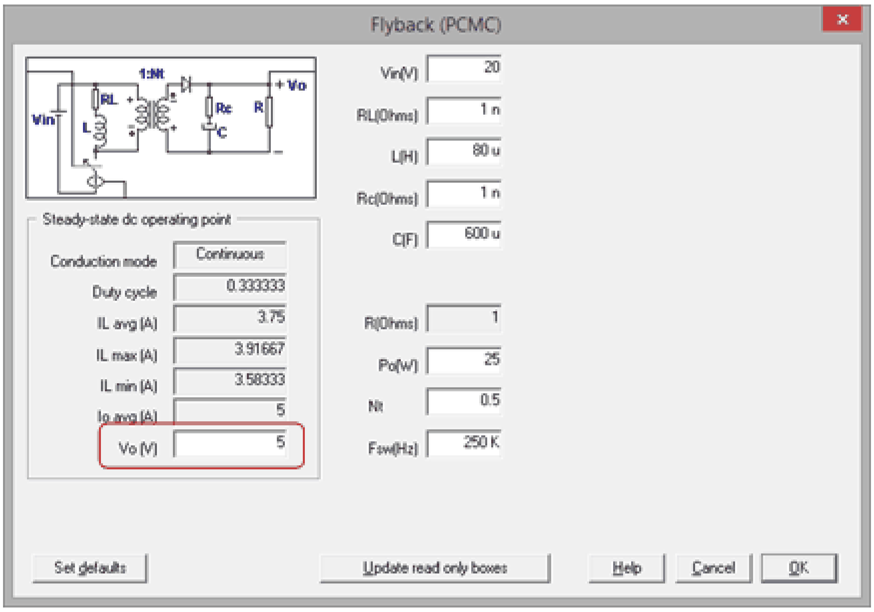
The **input data window** allows the user to select the desired input parameters and provides useful information such as the **steady state dc operating point**. This information is placed right below the converter image.

Two examples of the input data window are shown below, in each of them, the white shadowed boxes correspond to the input data boxes while the grey shadowed ones correspond to the additional information provided by the program.

Please, note that the input data is different in case of a voltage controlled plant (output voltage is an input) or a current controlled plant (in this case the current to be controlled is the input data). An example of the input data windows is provided below:



Input Data Window of a Voltage Mode Controlled Flyback and also for a Peak Current Mode Control Technique



Input Data Window of a Current Mode Controlled Flyback

The parameters shown in the input data windows are defined below:

Steady-state dc operating point

Conduction Mode It can be Continuous or Discontinuous
Duty Cycle t_{on}/T of the active switch
IL avg Inductance average current (A)
IL max Maximum value of the inductance switching ripple (A)
IL min Minimum value of the inductance switching ripple (A)
Io avg Output average current (A)
Vo Output voltage (V)

Other parameters of the converter

V_{in} Input Voltage (V)
R_L Equivalent Series Resistor of the Inductance (Ohms)
L Inductance (H)
R_c Equivalent Series Resistor of the output capacitor (Ohms)
C Output Capacitor (F)
R Load Resistor (Ohms)
P_o Output Power (W)
F_{SW} Switching frequency (Hz)

(*) N2 is the transformer secondary side number of turns
N1 is the transformer primary side number of turns

1.7.5 Forward

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Forward

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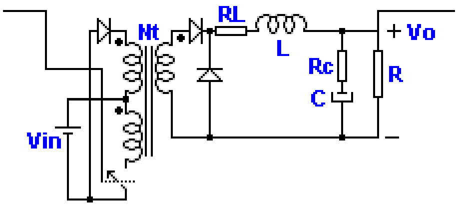
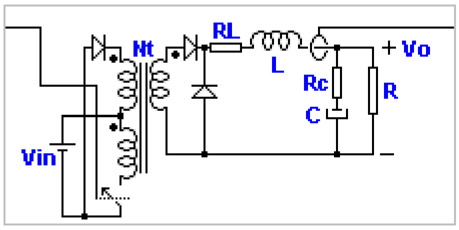
The magnitude to be controlled in a Forward converter can be either the output voltage or the inductance current. Both possibilities have been included in SmartCrl. The schematics are shown below:

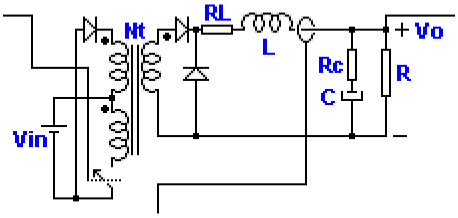


Voltage Mode Controlled Forward



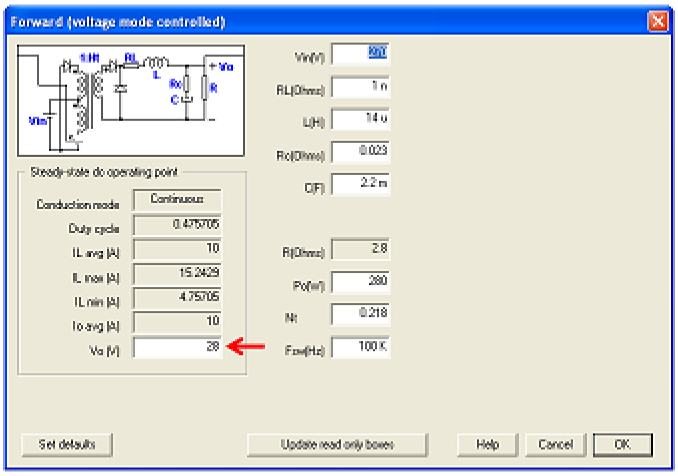
L-Current Sensed Forward

In the case of a **peak current mode control** (PCMC) scheme, the magnitudes sensed are the output voltage and the L current (sensed in the MOSFET).



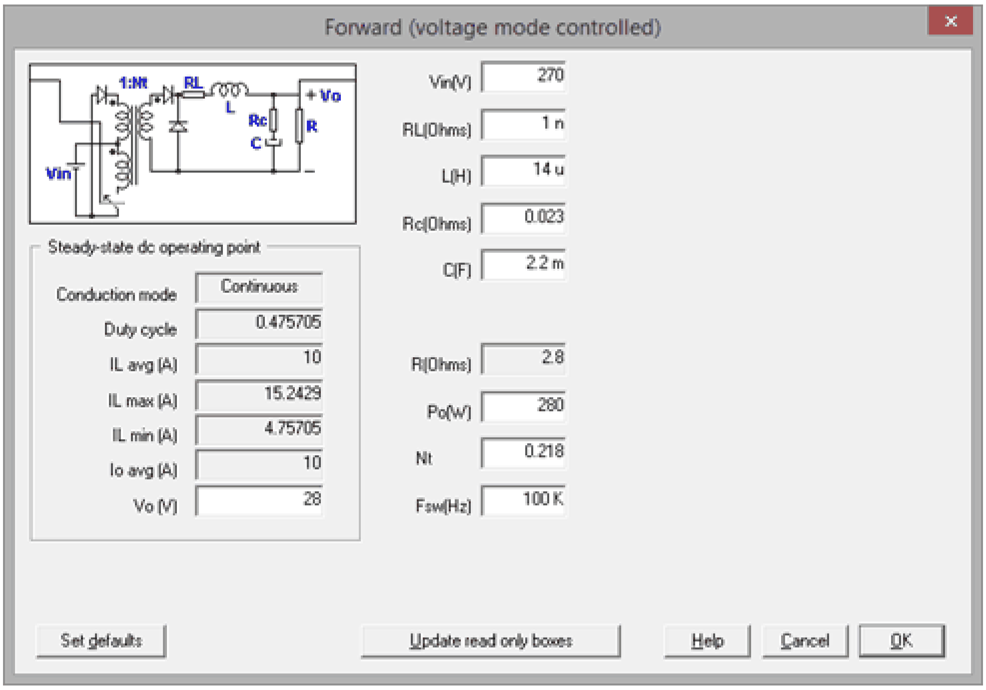
Forward (PCMC)

In the case of a **average current mode** control scheme, the magnitudes sensed are the output voltage and the L current.

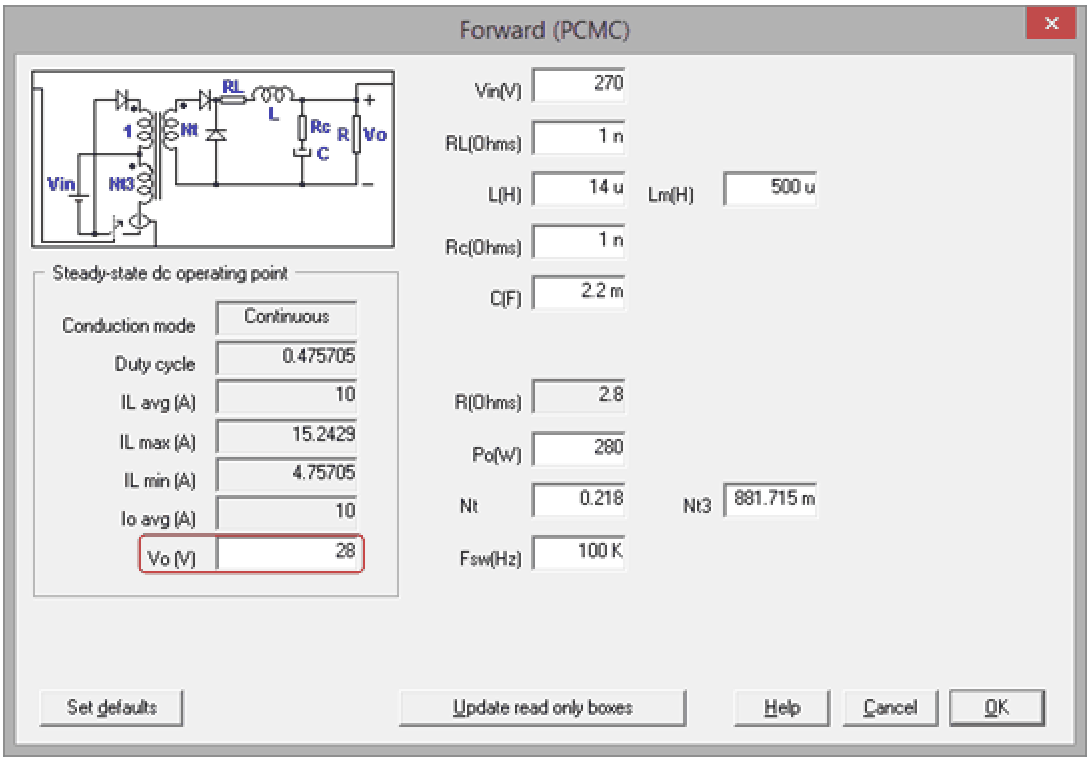


Forward (LCS-VMC)

The **input data window** allows the user to select the desired input parameters and provides useful information such as the **steady state dc operating point**. This information is placed right below the converter image.
Two examples of the input data window are shown below, in each of them, the white shadowed boxes correspond to the input data boxes while the grey shadowed ones correspond to the additional information provided by the program.
Please, note that the input data is different in case of a voltage controlled plant (output voltage is an input) or a current controlled plant (in this case the current to be controlled is the input data). An example of the input data windows is provided below:



Input Data Window of a Voltage Mode Controlled Forward and for Peak Current Mode Control.



Input Data Window of a Current Mode Controlled Forward

The parameters shown in the input data windows are defined below:

Steady-state dc operating point

Conduction Mode	It can be Continuous or Discontinuous
Duty Cycle	t_{on}/T of the active switch
IL avg	Inductance average current (A)
IL max	Maximum value of the inductance switching ripple (A)
IL min	Minimum value of the inductance switching ripple (A)
Io avg	Output average current (A)
Vo	Output voltage (V)

Other parameters of the converter

V_{in}	Input Voltage (V)
R_L	Equivalent Series Resistor of the Inductance (Ohms)
L	Inductance (H)
R_c	Equivalent Series Resistor of the output capacitor (Ohms)
C	Output Capacitor (F)
R	Load Resistor (Ohms)
P_o	Output Power (W)
F_{SW}	Switching frequency (Hz)

(*) N2 is the transformer secondary side number of turns

N1 is the transformer primary side number of turns

1.7.6 Phase Shifted Full Bridge

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Phase Shifted Full Bridge

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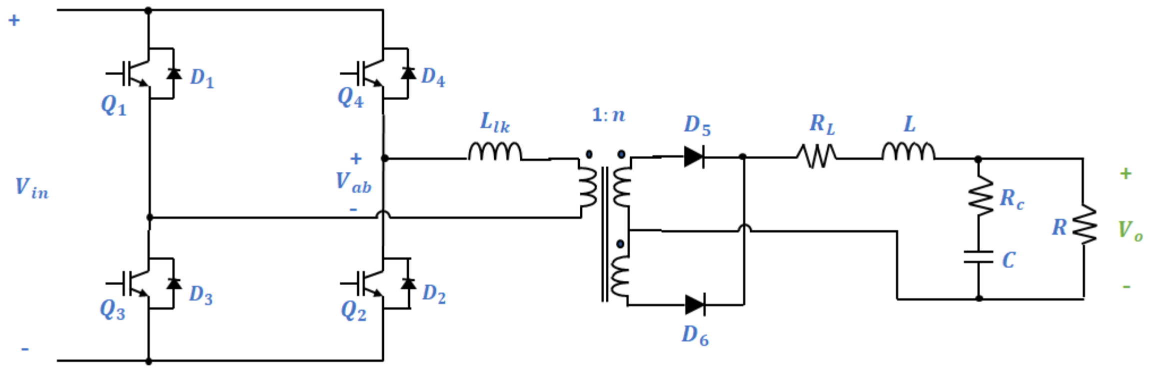
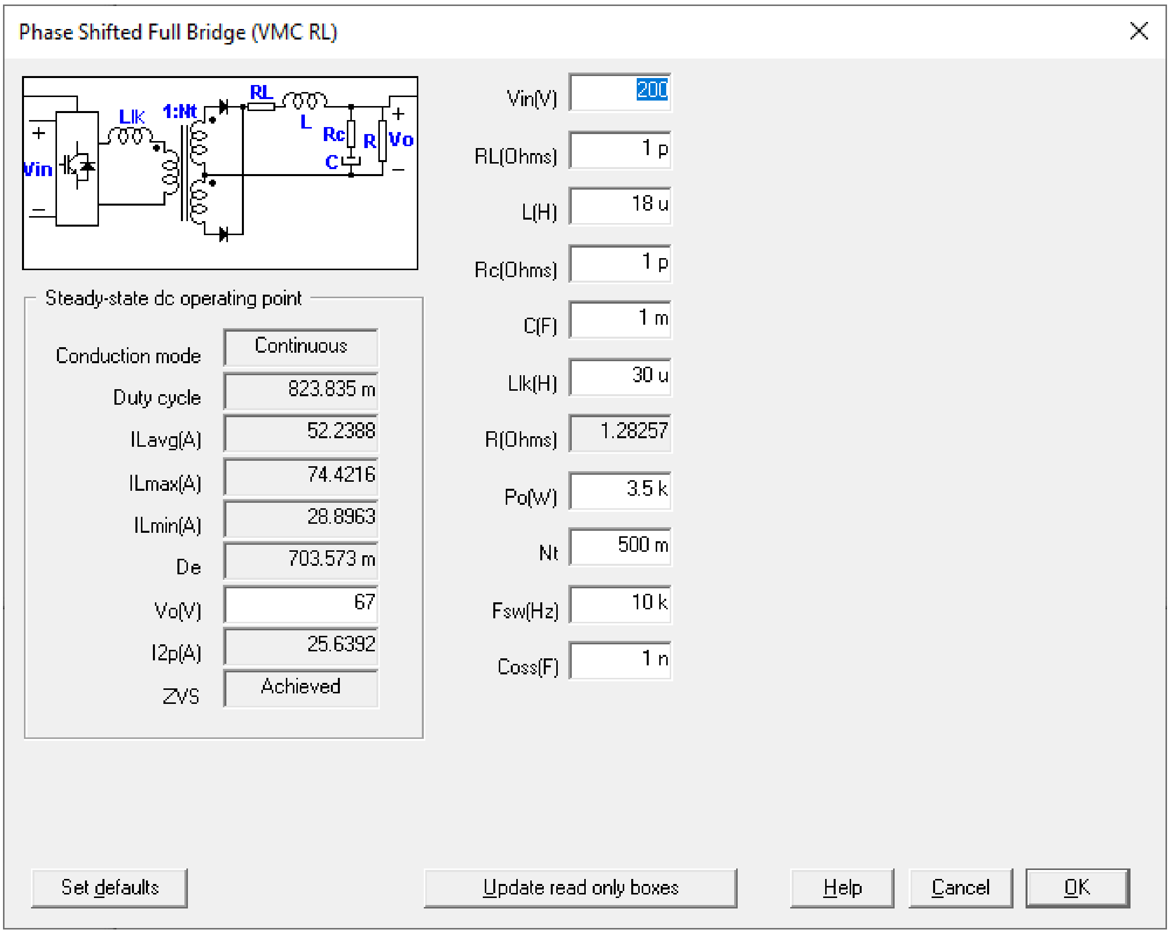
When a **single loop control scheme** is used the magnitude to be controlled in a phase shifted Full Bridge is the output Voltage. The schematics are shown below:



Phase Shifted Full Bridge Voltage Mode Controlled with Resistive Load

The **input data window** allows the user to select the desired input parameters and provides useful information such as the **steady state dc operating point**. This information is placed right below the converter image.

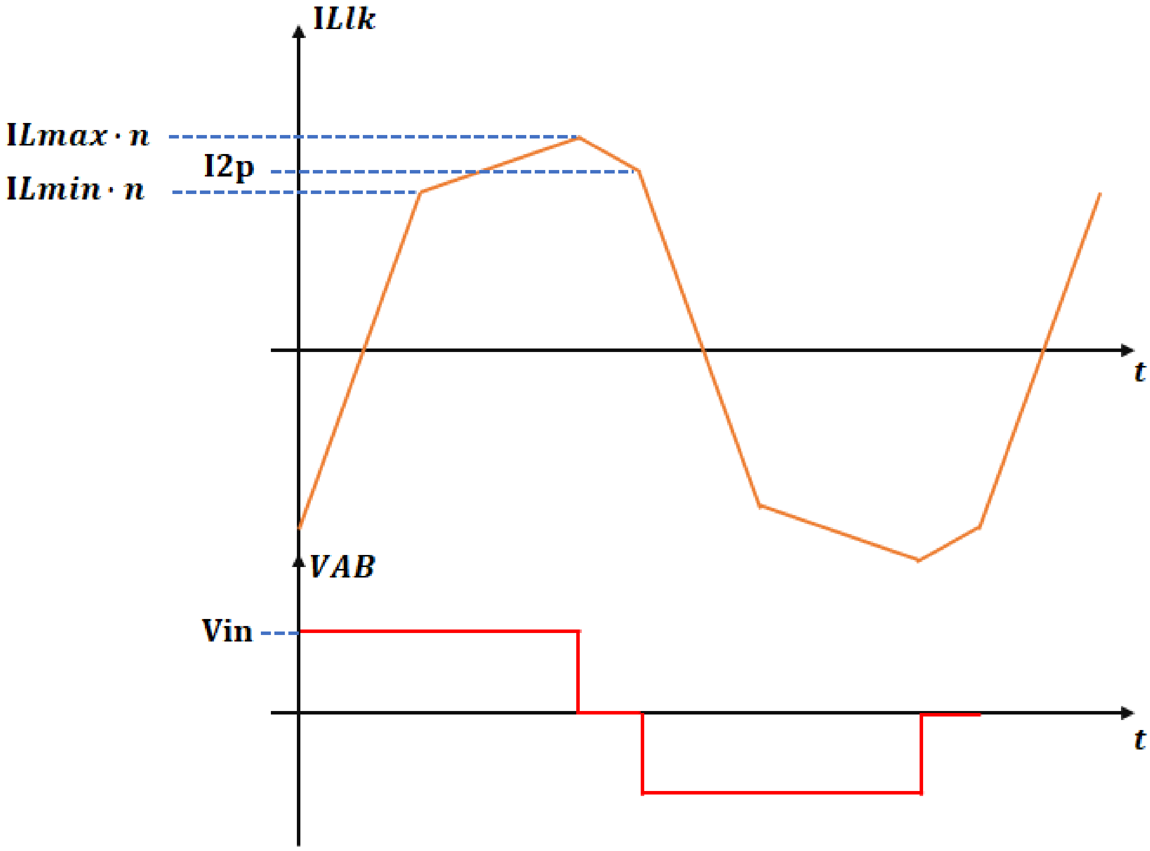


The white shadowed boxes correspond to the input data boxes while the grey shadowed ones correspond to the additional information provided by the program.

The parameters shown in the input data windows are defined below:

Steady-state dc operating point

Conduction Mode It can be Continuous or Discontinuous
Duty Cycle (D) t_{on}/T of the active switch
IL avg Inductance average current (A)
IL max Maximum value of the inductance switching ripple (A)
IL min Minimum value of the inductance switching ripple (A)
Io avg Output average current (A)
De Effective Duty cycle
Vo Output voltage (V)
I2p It is the current through Llk at the moment that the primary voltage (VAB) begins to increase towards Vin (A)



ZVS Zero Voltage Switching

Other parameters of the converter

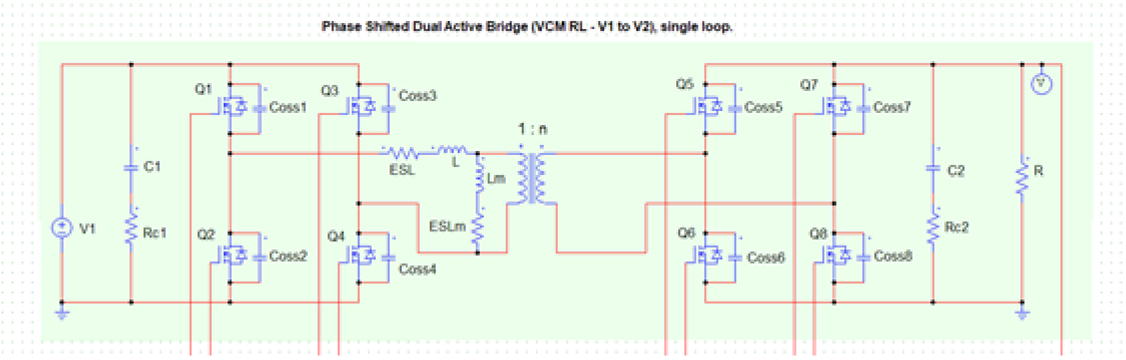
V_{in} Input Voltage (V)
R_L Equivalent Series Resistor of the Inductance (Ohms)
L Inductance (H)
R_c Equivalent Series Resistor of the output capacitor (Ohms)
C Output Capacitor (F)
Llk Leakage Inductance (H)
R Load Resistor (Ohms)
P_o Output Power (W)
Nt Transformer turns ratio (N1/N2)
F_{SW} Switching frequency (Hz)
Coss Mosfet output capacitance (F)

(*) N2 is the transformer secondary side number of turns
N1 is the transformer primary side number of turns

1.7.7 Phase Shifted Dual Active Bridge (VMC RL - V1 to V2)

Phase Shifted Dual Active Bridge (VMC RL - V1 to V2)

Power stage description (NEW in version 5.0):



In this power stage, the **Dual Active Bridge** (DAB) converter is studied with a single voltage control loop on a resistive load ("RL").

The name ("V1 to V2") indicates that the direction of the power transfer is from the bridge whose voltage is denoted V1 (on the left in the picture) to the port with the voltage V2 (on the right).

The voltage V2 (the voltage at Bridge 2) is the one controlled.

Further considerations:

•The power losses are not considered in the theoretical study

•To consider that the switching is done under ZVS (Zero Voltage Switching) conditions, the value of the current at the switching instant must be:

▪≥ $I_{ZVS,Bridge\ 1\ (Q1-Q3)}$ in Q1 and Q3 transistorsof Bridge 1.

▪≥ $I_{ZVS,Bridge\ 1\ (Q2-Q4)}$ at Q2 and Q4 transistors of Bridge 1.

▪≥ $I_{ZVS,Bridge\ 2}$ in the transistors located in Bridge 2.

$$I_{ZVS,Bridge\ 1\ (Q1-Q3)} = V_1\sqrt{\frac{2Coss_1}{L}} - \left[\frac{V_2\left({}^{2\varphi(°)}/_{180} - 1\right)}{4 \cdot L_m \cdot n \cdot F_{sw}}\right] \cdot \sqrt{\frac{L_m}{L}}$$

$$I_{ZVS,Bridge\ 1\ (Q2-Q4)} = V_1\sqrt{\frac{2Coss_1}{L}} + \left[\frac{V_2\left({}^{2\varphi(°)}/_{180} - 1\right)}{4 \cdot L_m \cdot n \cdot F_{sw}}\right] \cdot \sqrt{\frac{L_m}{L}}$$

$$I_{ZVS,Bridge\ 2} = V_2\sqrt{\frac{2Coss_2}{L}}$$

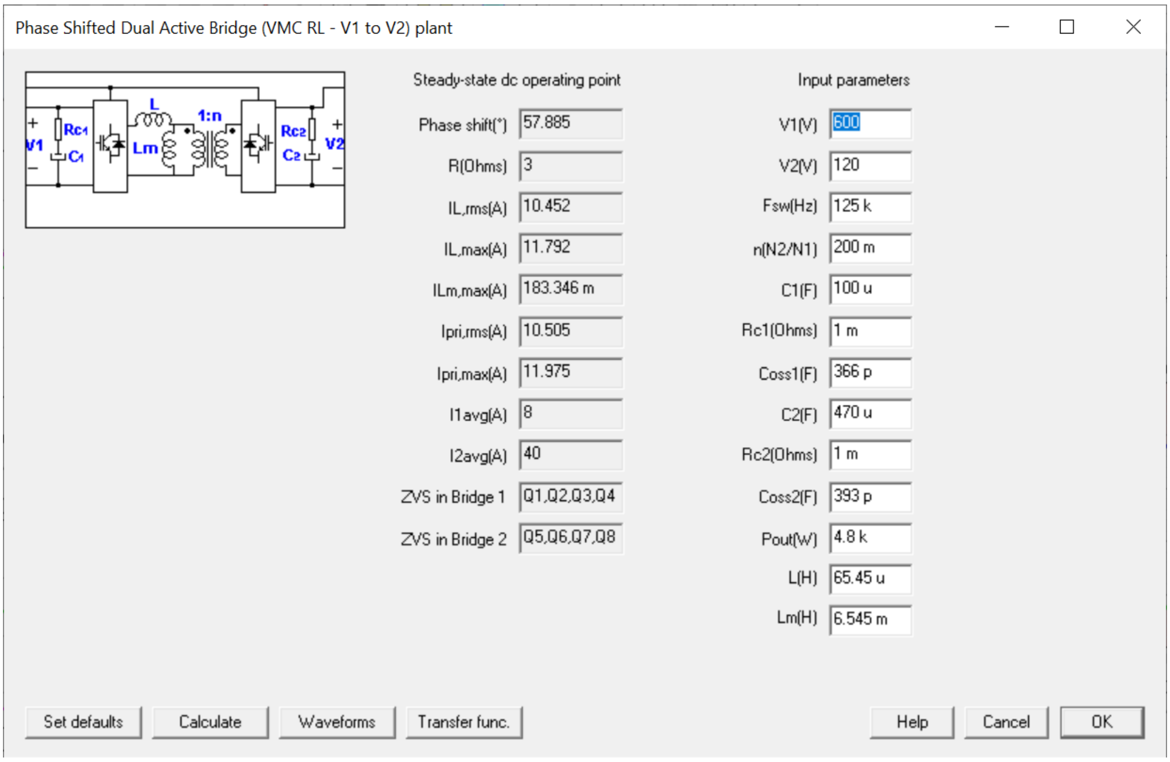
•The input impedance (Zi) calculation considers the input filter (C1 + Rc1).

•The output impedance (Zo) calculation considers the output filter (C2 + Rc2).

•**When exporting the schematic to PSIM**, a series resistance to the inductor L (ESL) of 0.1Ω and a series resistance to the magnetizing inductance Lm (ESLm) of 1Ω are considered to help the steady-state to be reached earlier in the simulation. Those resistances are not considered in the theoretical study.

•**When exporting the schematic to PSIM**, a death time of 50ns is considered. The death time is not considered in the theoretical study.

The **input data window** allows the user to select the desired input parameters and provides useful information such as the **steady state dc operating point**.



Parameter description in the initial dialogue:

Input parameters:

V1(V) Input voltage (Volts)

V2(V) Output voltage. Controlled. (Volts)

Fsw(Hz) Switching frequency (Hertz)

n(N2/N1) Turn ratio (dimensionless). It is considered as the number of turns of the secondary N2, divided by the number of turns in the primary N1.

C1(F) Input filter capacitance (Farads)

Rc1(Ohms) Series resistance to the input filter capacitor (Ohms)

Coss1(F) Output parasitic capacitance of the transistors in Bridge 1 (Farads)

C2(F) Output filter capacitance (Farads)

Rc2(Ohms) Series resistance to the output filter capacitor (Ohms)

Coss2(F) Output parasitic capacitance of the transistors in Bridge 2 (Farads)

Pout(W) Load power (W)

L(H) Inductance (Henries)

Lm(H) Transformer's magnetizing inductance referred to the primary (Henries)

Steady-state dc operating point:

Phase Shift (°) The phase shift between Bridge 1 and Bridge 2 (degrees). It is defined as the time elapsed between the turn-on of transistor Q1 and the turn-on of transistor Q5 related to the period (= 1/Fsw). Control variable. To calculate:

$$\varphi(°) = 180 \cdot \left[\frac{1}{2} - \frac{\sqrt{\left(\frac{1}{F_{sw}}\right) \cdot V_1^2 \cdot V_2^2 - 8 \cdot L \cdot P_{out} \cdot V_1 \cdot V_2}}{2\sqrt{\frac{1}{F_{sw}}} \cdot V_1 \cdot V_2}\right]$$

R(Ohms) Load resistance (Ω).

IL,rms(A) Effective current through L (Amperes)

IL,max(A) Maximum (peak) current through inductance L (Amps). DAB's current through L is AC

ILm,max(A) Maximum (peak) current through Lm (Amperes).

Ipri,rms(A) Effective current at the transformer primary (Amps).

Ipri,max(A) Maximum (peak) current through the transformer's primary winding (Amperes).

I1,avg(A) Average input current (Bridge 1) (Amperes)

I2,avg(A) Average output current (Bridge 2) (Amperes)

ZVS in Bridge 1 This field shows which transistors in Bridge 1 meet the constraint to be considered as switching a ZVS-switching. Whether or not ZVS is obtained depends on the operating point and specifications. If no transistors meet the constraint, the message "None" is displayed.

ZVS in Bridge 2 This field shows which transistors in Bridge 2 meet the constraint to be considered as switching with ZVS. Whether or not ZVS is obtained depends on the operating point and specifications. If no transistors meet the constraint, the message "None" is displayed.

Phase Shifted Full Bridge Dual Active Bridge additional waveforms

•**Bridges differential voltages vs time:** V11 and V22 signals are displayed simultaneously. These signals are important as they show the phase difference between the bridges, which determines the transferred power.

▪The signal V11 refers to the differential voltage between the midpoint of the transistor branches of Bridge 1. In the equation they appear in lower case because they are time-dependent:

$$v_{11} = v_{DS,Q2} - v_{DS,Q4}$$

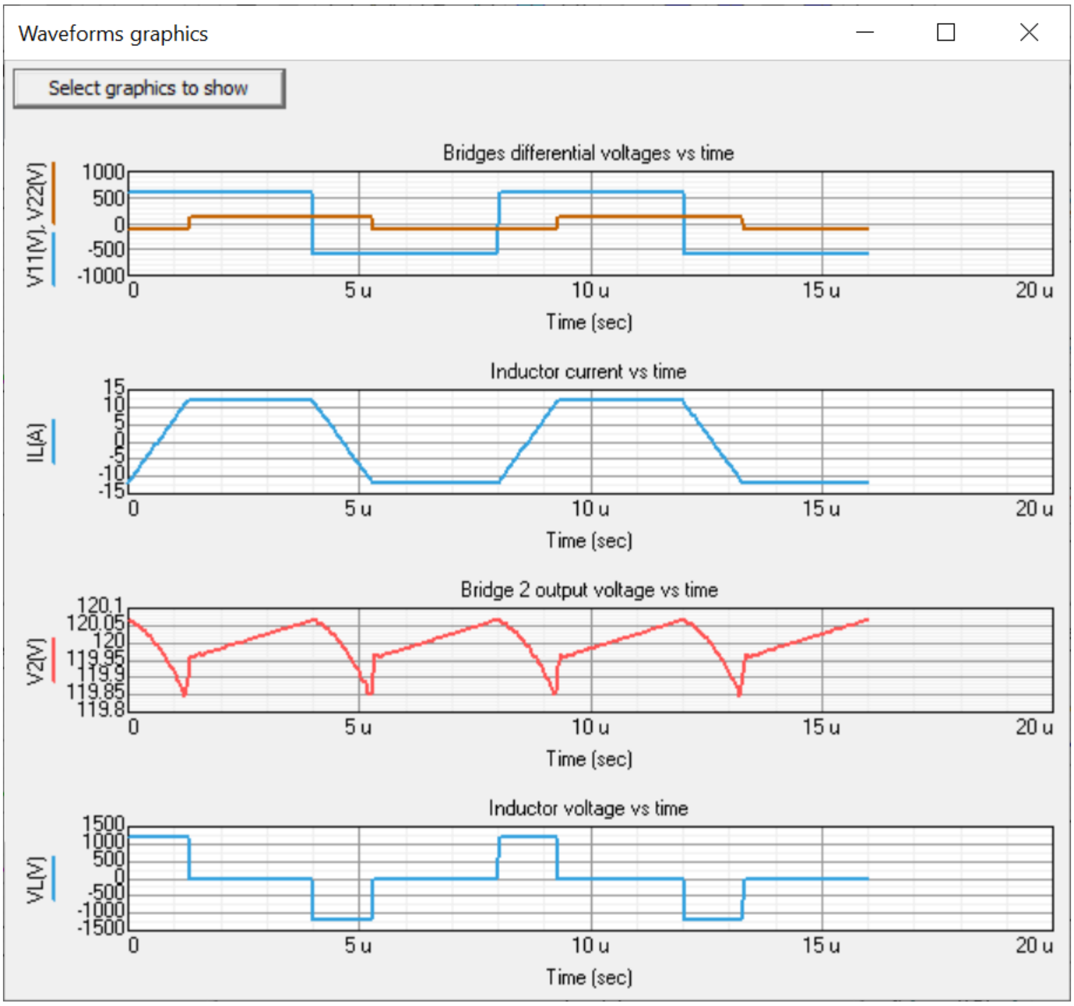
▪The signal V22 refers to the differential voltage between the midpoint of the transistor branches of Bridge 2. In the equation they appear in lower case because they are time-dependent:

$$v_{22} = v_{DS,Q6} - v_{DS,Q8}$$

•Inductor current vs time

•**Bridge 2 output voltage vs time**: This is the DC voltage being controlled, V2.

•Inductor voltage vs time



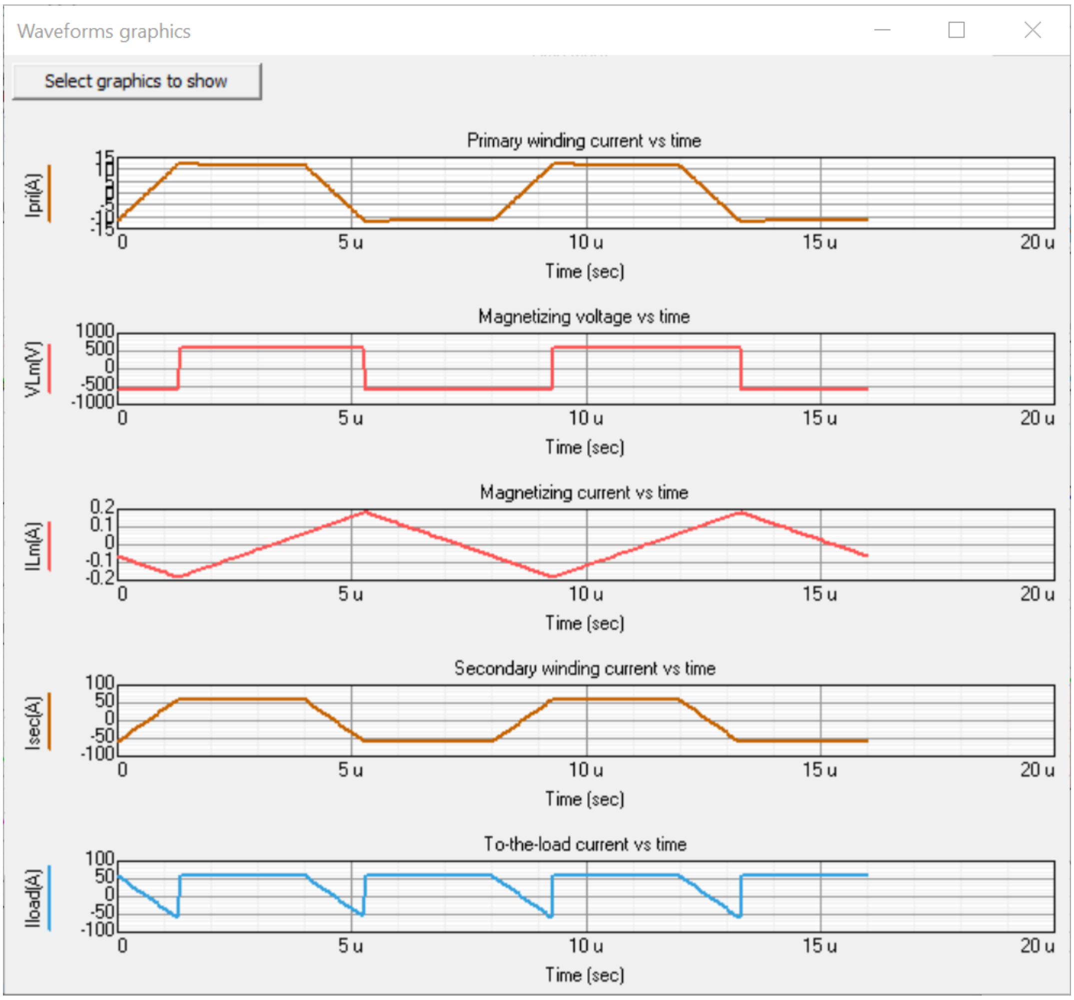
•Primary winding current vs time

•Magnetizing voltage vs time

•Magnetizing current vs time

•Secondary winding current vs time

•**To-the-load current vs time**: It is the filtered current flowing through the load, in this case R.



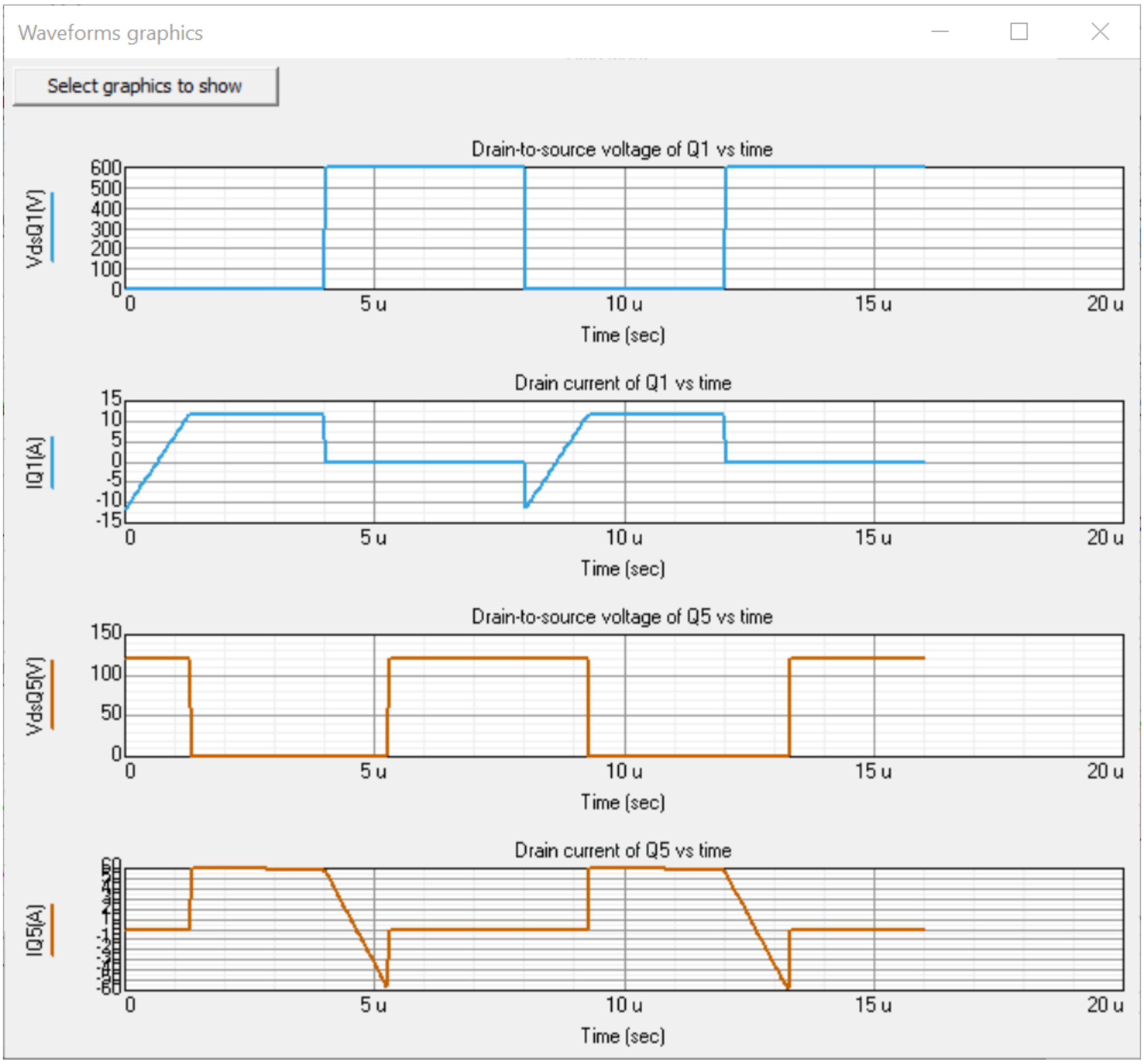
•**Drain-to-source voltage of Q1 vs time**: Drain-to-source voltage on transistor Q1 (Bridge 1, external branch, above). As long as it has the value V1, transistor Q1 is open. The falling edge of this signal is considered the start of the phase shift time and coincides with the rising edge of the *Phase Shift* signal in the SmartCtrl main window.

•**Drain current of Q1 vs time**: Q1 drain current. Being smaller than

$I_{ZVS,Bridge\ 1\ (Q1-Q3)}$ at the turning-on means that the transistor has ZVS.

•**Drain-to-source voltage of Q5 vs time**: Drain-to-source voltage at transistor Q5 (Bridge 2, internal branch, above). If it has the value V2, transistor Q5 is open. The falling edge of this signal is considered the end of the phase-shift time and coincides with the falling edge of the *Phase Shift* signal in the SmartCtrl main window.

•**Drain current of Q5 vs time**: Q5 drain current. Being smaller than $I_{ZVS,Bridge\ 2}$ at the turning-on means that the transistor has ZVS.



Phase Shift waveform interpretation

In the power stages with PWM modulation the waveform that usually appears in this location is the switching signal of the transistor that commands the operation.

In this case (and in the Full-Bridge plant introduced in the SmartCtrl 4.2 version) the phase-shift time is shown, which is the control variable in a *Phase Shif.t* modulation. As can be seen in the picture below, the rising edge refers to the triggering of transistors Q1 and Q3, while the falling edge refers to the triggering of transistors Q5 and Q8.

The classic Phase shift modulation proposed to govern the DAB (Dual Active Bridge) consists of dephasing the turning-on of the Q5-Q6 branch from the Q1-Q2 branch, to transfer power from Bridge 1 to Bridge 2 (POSITIVE phase shift).

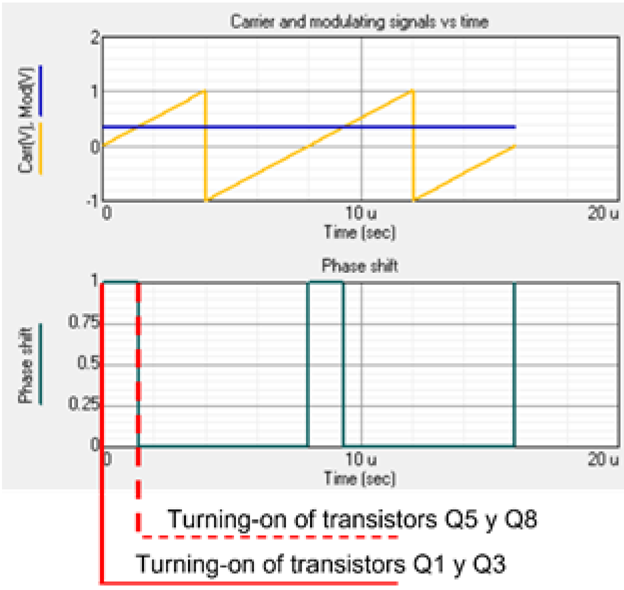
•The transistors in each branch are controlled complementary (ideally with no dead time) and remain on for half the period = $1/(2 \cdot F_{SW})$.

•The transistors in each Bridge are controlled as explained below:

oIn Bridge 1, Q1 and Q4 are turned on simultaneously. Q2 and Q3 operate the remaining half-period once the Q1 and Q4 are turned off.

oIn Bridge 2, Q5 and Q8 are turned on simultaneously. Q6 and Q7 operate the remaining half-period once the Q5 and Q8 are turned off.

Thus, from the representation of the Phase Shift waveform, the operation of all transistors in the DAB (Dual Active Bridge) can be deduced.



SmartCtrl modulator when used for Phase Shift modulation and gain modification

In the SmartCtrl 5.0 version, the image of the modulator is maintained with respect to the PWM basic one, although in this case, it would be representing a modulator that generates the driving signals of all the transistors of Bridges 1 and 2 with the phase shift calculated as discussed in the previous section.

The modulator gain expression is shown below. To adjust it to the gain of a known system, the parameters Vp and Vv can be modified (Vv = -Vp)

$$G_{mod} = \frac{2}{(V_p - V_v)}$$

1.7.8 Phase Shifted Dual Active Bridge (VMC ERL - V1 to V2)

Navigation: SmartCtrl > DC-DC Plants >

Phase Shifted Dual Active Bridge (VMC ERL - V1 to V2)

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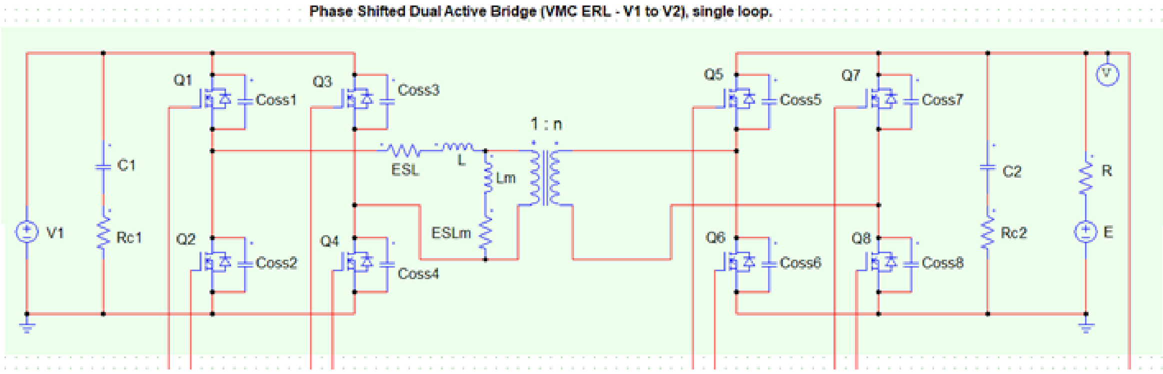
Power stage description (NEW in version 5.0):



In this power stage, the **Dual Active Bridge** (DAB) converter is studied with a single voltage control loop on a bus type load, modeled as a voltage source with a series resistor ("ERL"). The voltage source represents the voltage at the operating point analyzed, whereas the series resistor models the bus resistance.

The name ("*V1 to V2*") indicates that the direction of the power transfer is from the bridge whose voltage is denoted V1 (on the left in the picture) to the port with the voltage V2 (on the right).

The voltage V2 (the voltage at Bridge 2) is the one controlled.

Further considerations:

•This study helps the control design of a battery charger during the fixed-voltage stages

•The power losses are not considered in the theoretical study

•To consider that the switching is done under ZVS (*Zero Voltage Switching*) conditions, the value of the current at the switching instant must be:

$0 \geq I_{ZVS,Bridge\ 1\ (Q1-Q3)}$ in Q1 and Q3 transistors of Bridge 1 o≥ $I_{ZVS,Bridge\ 1\ (Q2-\ Q4)}$ in Q2 y Q4 transistors of Bridge 1

o≥ $I_{ZVS,Bridge\ 2}$ in the transistors located in Bridge 2

$$I_{ZVS,Bridge\ 1\ (Q1-Q3)} = V_1\sqrt{\frac{2Coss_1}{L}} - \left[\frac{V_2({}^{2\varphi(°)}/_{180} - 1)}{4 \cdot L_m \cdot n \cdot F_{sw}}\right] \cdot \sqrt{\frac{L_m}{L}}$$

$$I_{ZVS,Bridge\ 1\ (Q2-Q4)} = V_1\sqrt{\frac{2Coss_1}{L}} + \left[\frac{V_2({}^{2\varphi(°)}/_{180} - 1)}{4 \cdot L_m \cdot n \cdot F_{sw}}\right] \cdot \sqrt{\frac{L_m}{L}}$$

$$I_{ZVS,Bridge\ 2} = V_2\sqrt{\frac{2Coss_2}{L}}$$

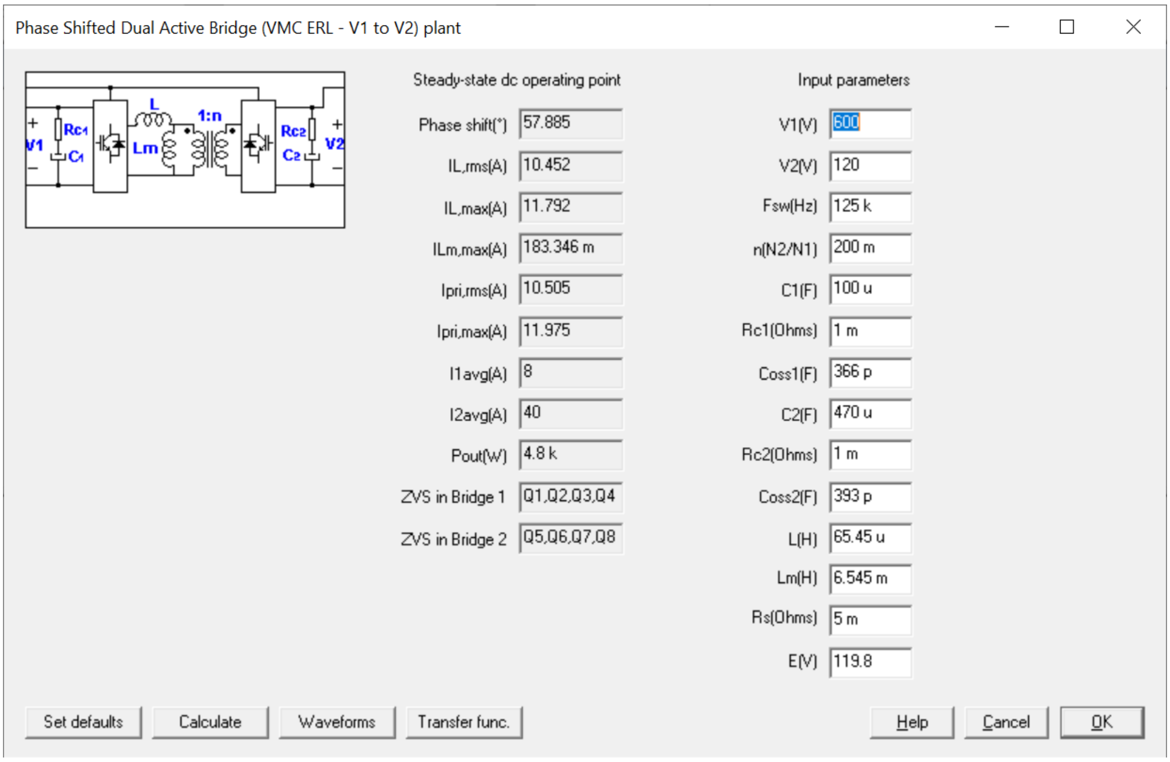
•The input impedance (Zi) calculation considers the input filter (C1 + Rc1)

•The output impedance (Zo) calculation considers the output filter (C2 + Rc2)

•**When exporting the schematic to PSIM,** a series resistance to the inductor L (ESL) of 0.1Ω and series resistance to the magnetizing inductance Lm (ESLm) of 1Ω are considered to help the steady-state to be reached earlier in the simulation. Those are not considered in the theoretical study

•**When exporting the schematic to PSIM,** a death-time of 50ns is considered. The death time is not considered in the theoretical study

The **input data window** allows the user to select the desired input parameters and provides useful information such as the **steady state dc operating point**.



Parameter description in the initial dialogue:

Input parameters:

V1(V) Input voltage (Volts)

V2(V) Output voltage. Controlled. (Volts)

Fsw(Hz) Switching frequency (Hertz)

n(N2/N1) Turn ratio (dimensionless). It is considered as the number of turns of the secondary N2, divided by the number of turns in the primary N1.

C1(F) Input filter capacitance (Farads)

Rc1(Ohms) Series resistance to the input filter capacitor (Ohms)

Coss1(F) Output parasitic capacitance of the transistors in Bridge 1 (Farads)

C2(F) Output filter capacitance (Farads)

Rc2(Ohms) Series resistance to the output filter capacitor (Ohms)

Coss2(F) Output parasitic capacitance of the transistors in Bridge 2 (Farads)

L(H) Inductance (Henries)

Lm(H) Transformer's magnetizing inductance referred to the primary (Henries)

Rs(Ohms) Series resistance in the bus load

E(V) Voltage at the operating point

Steady-state dc operating point:

Phase Shift (°) The phase shift between Bridge 1 and Bridge 2 (degrees). It is defined as the time elapsed between the turn-on of transistor Q1 and the turn-on of transistor Q5 related to the period (= 1/Fsw). Control variable. To calculate:

$$\varphi(^\circ) = 180 \cdot \left[\frac{1}{2} - \frac{\sqrt{\left(\frac{1}{F_{sw}}\right) \cdot V_1^2 \cdot V_2^2 - 8 \cdot L \cdot P_{out} \cdot V_1 \cdot V_2}}{2\sqrt{\frac{1}{F_{sw}}} \cdot V_1 \cdot V_2} \right]$$

IL,rms(A) Effective current through L (Amperes)

IL,max(A) Maximum (peak) current through L (Amps). DAB's current through L is AC

ILm,max(A) Maximum (peak) current through Lm (Amperes).

Ipri,rms(A) Effective current at the transformer's primary winding (Amps).

Ipri,max(A) Maximum (peak) current through the transformer's primary winding (Amperes).

I1,avg(A) Average input current (Bridge 1) (Amperes)

I2,avg(A) Average output current (Bridge 2) (Amperes)

Pout(W) Load power (W)

ZVS in Bridge 1 This field shows which transistors in Bridge 1 meet the constraint to be considered as switching a ZVS-switching. Whether or not ZVS is obtained depends on the operating point and specifications. If no transistors meet the constraint, the message "None" is displayed.

ZVS in Bridge 2 This field shows which transistors in Bridge 2 meet the constraint to be considered as switching with ZVS. Whether or not ZVS is obtained depends on the operating point and specifications. If no transistors meet the constraint, the message "None" is displayed.

Waveforms displayed

•**Bridges differential voltages vs time**: signals V11 and V22 are displayed simultaneously. These signals are important as they show the phase difference between the bridges, which determines the transferred power.

oThe signal V11 refers to the differential voltage between the midpoint of the transistor branches of Bridge 1. In the equation they appear in lower case because they are time-dependent:

$$v_{11} = v_{DS,Q2} - v_{DS,Q4}$$

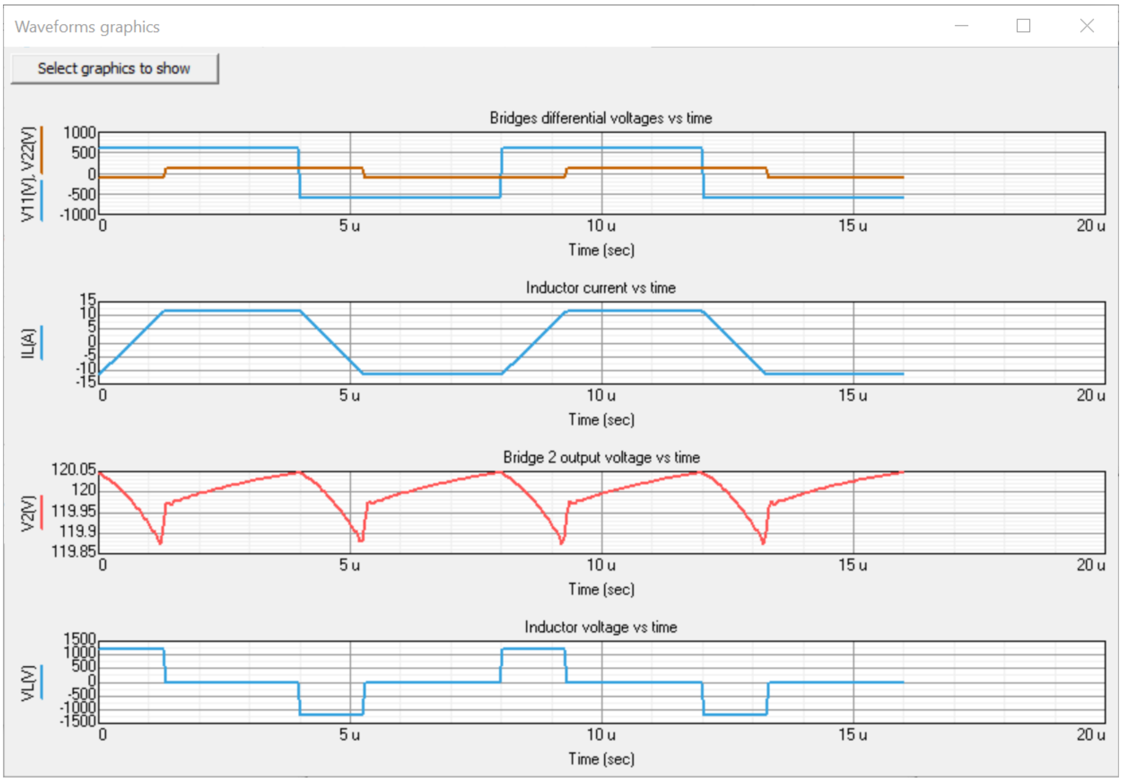
oThe signal V22refers to the differential voltage between the midpoint of the transistor branches of Bridge 2. In the equation they appear in lower case because they are time-dependent:

$$v_{22} = v_{DS,Q6} - v_{DS,Q8}$$

•Inductor current vs time

•**Bridge 2 output voltage vs time**: This is the DC voltage being controlled, V2.

•Inductor voltage vs time



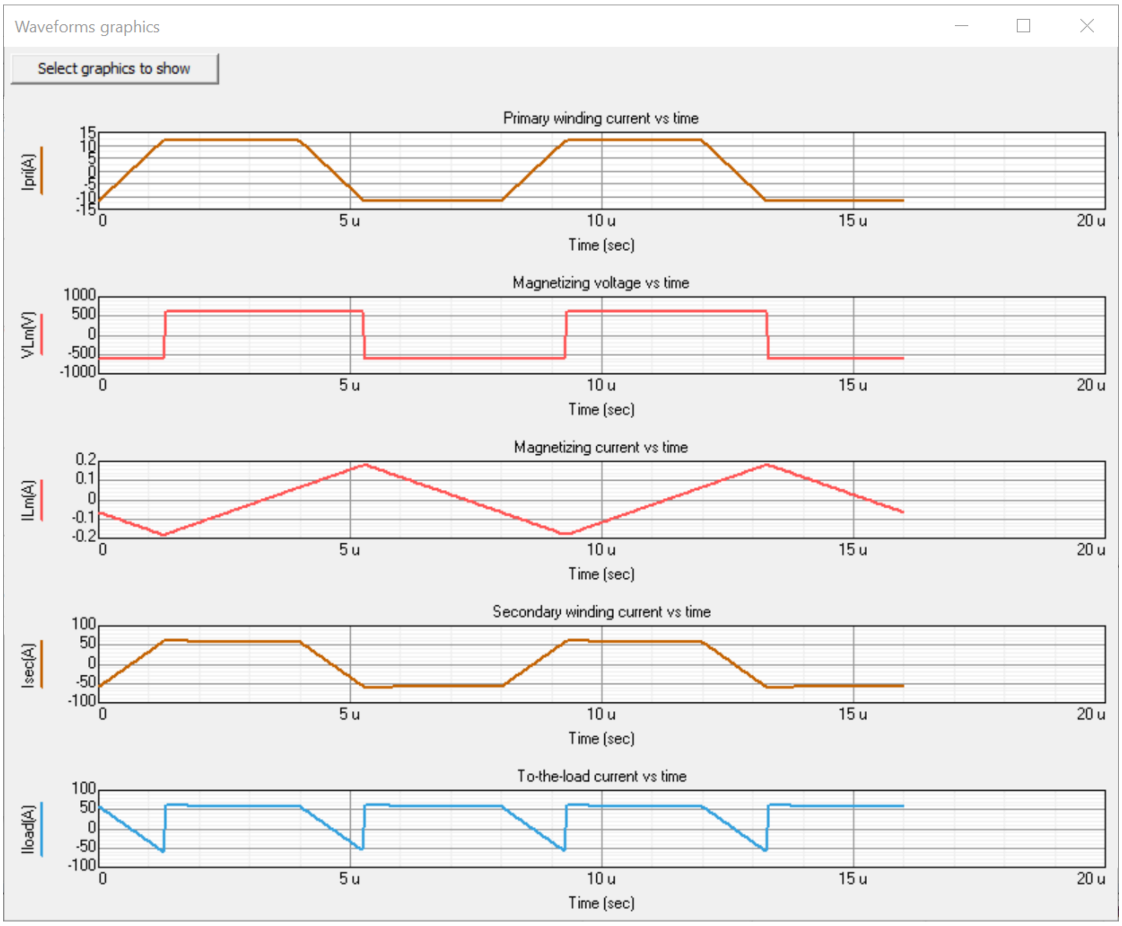
•Primary winding current vs time

•Magnetizing voltage vs time

•Magnetizing current vs time

•Secondary winding current vs time

•**To-the-load current vs time:** It is the filtered current flowing through the load, in this case, R.

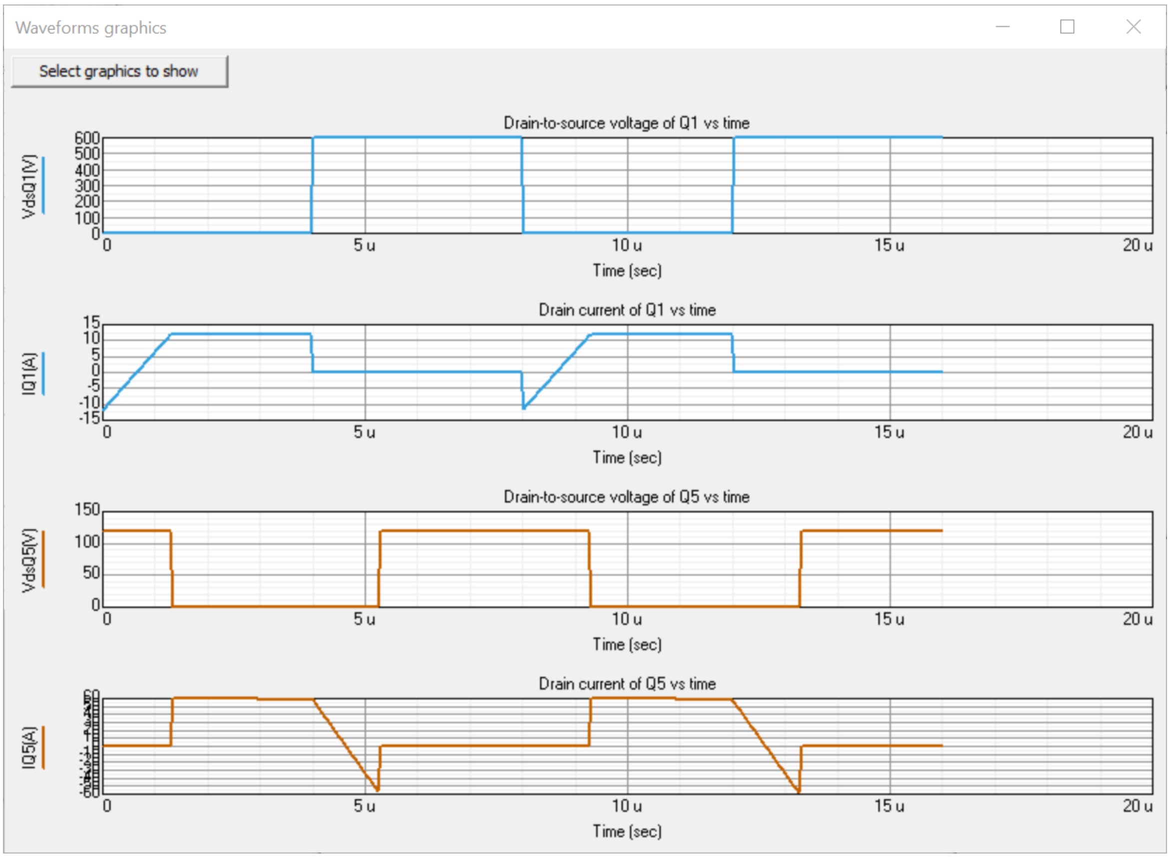


•**Drain-to-source voltage of Q1 vs time:** Drain-to-source voltage on transistor Q1 (Bridge 1, external branch, above). If it has the value V1, transistor Q1 is open. The falling edge of this signal is considered the start of the phase shift time and coincides with the rising edge of the *Phase Shift* signal in the SmartCtrl main window.

•**Drain current of Q1 vs time:** Q1s drain current. Being smaller than $I_{ZVS,Bridge\ 1\ (Q1-Q3)}$ at the turning-on means that the transistor has ZVS.

•**Drain-to-source voltage of Q5 vs time:** Drain-to-source voltage on transistor Q5 (Bridge 2, inner branch, above). If it has the value V2, transistor Q5 is open. The falling edge of this signal is considered the end of the phase-shift time and coincides with the falling edge of the *Phase Shift* signal in the SmartCtrl main window.

•**Drain current of Q5 vs time:** Q5s drain current. Being smaller than $I_{ZVS,Bridge\ 2}$ at the turning-on means that the transistor has ZVS.



Phase Shift waveform interpretation

In the power stages with PWM modulation the waveform that usually appears in this location is the switching signal of the transistor that commands the operation.

In this case (and in the Full-Bridge plant introduced in the SmartCtrl 4.2 version) the phase-shift time is shown, which is the control variable in a *Phase Shift* modulation. As can be seen in the picture below, the rising edge refers to the triggering of transistors Q1 and Q3, while the falling edge refers to the triggering of transistors Q5 and Q8.

The classic Phase shift modulation proposed to govern the DAB consists of dephasing the turning-on of the Q5-Q6 branch from the Q1-Q2 branch, to transfer power from Bridge 1 to Bridge 2 (POSITIVE phase shift).

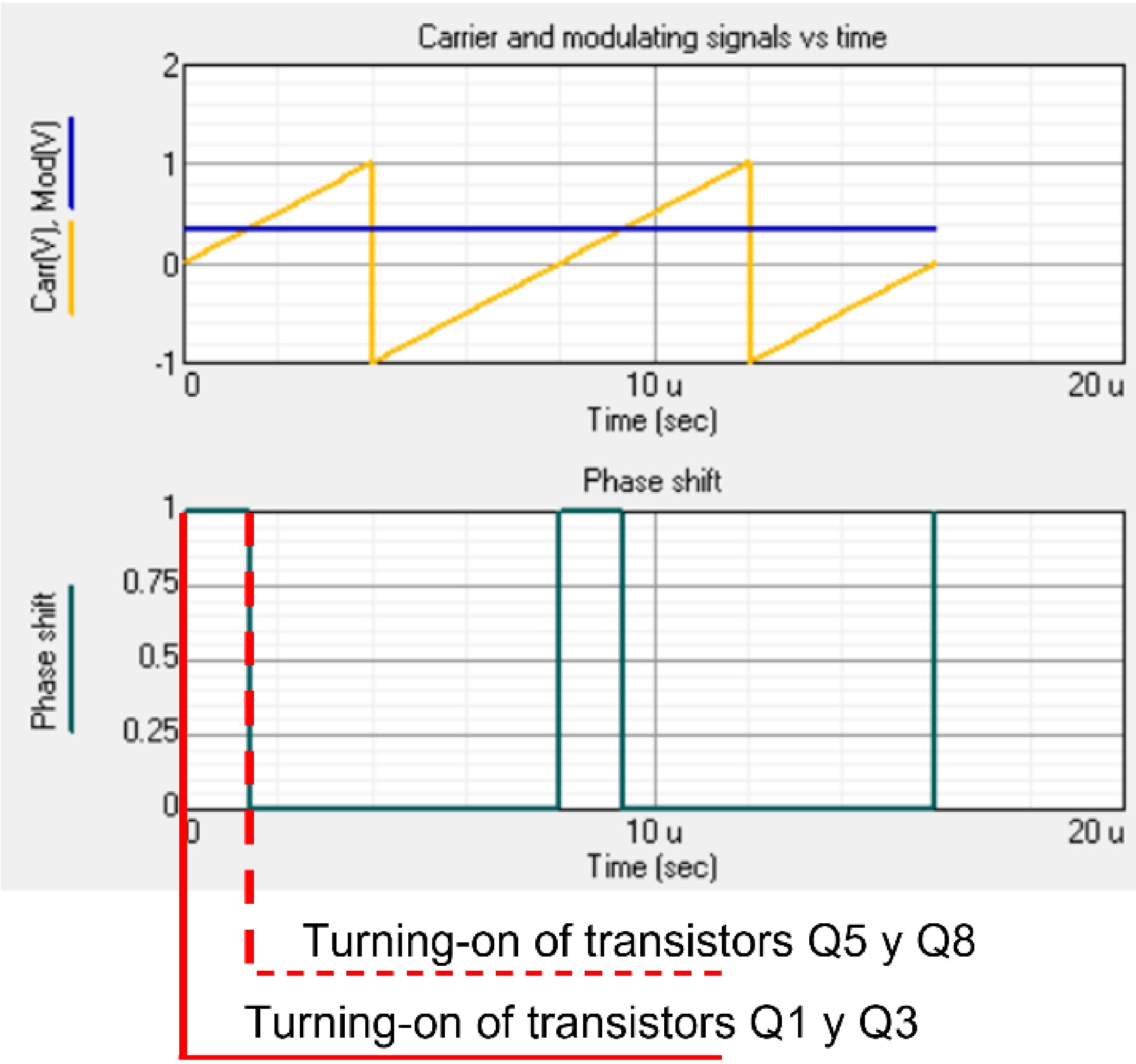
- The transistors in each branch are controlled complementary (ideally with no dead time) and remain on for half the period = $1/(2 \cdot F_{SW})$.

- The transistors in each Bridge are controlled as explained below:

    - In Bridge 1, Q1 and Q4 are turned on simultaneously. Q2 and Q3 operate the remaining half-period once the Q1 and Q4 are turned off.

    - In Bridge 2, Q5 and Q8 are turned on simultaneously. Q6 and Q7 operate the remaining half-period once the Q5 and Q8 are turned off.

Thus, from the representation of the Phase Shift waveform, the operation of all transistors in the DAB can be deduced.



SmartCtrl modulator when used for Phase Shift modulation and gain modification

In the SmartCtrl 5.0 version, the image of the modulator is maintained with respect to the PWM basic one, although in this case, it would be representing a modulator that generates the driving signals of all the transistors of Bridges 1 and 2 with the phase shift calculated as discussed in the previous section.

The modulator gain expression is shown below. To adjust it to the gain of a known system, the parameters Vp and Vv can be modified (Vv = -Vp)

$$G_{mod} = \frac{2}{(V_p - V_v)}$$

1.7.9 Phase Shifted Dual Active Bridge (CS ERL - V1 to V2)

Navigation: SmartCtrl > DC-DC Plants >

Phase Shifted Dual Active Bridge (CS ERL - V1 to V2)

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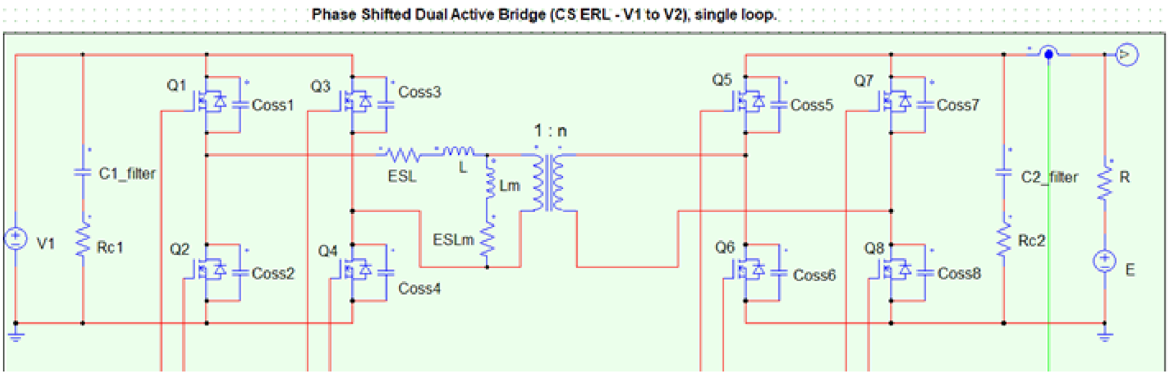
Power stage description (NEW in version 5.0):



In this power stage, the **Dual Active Bridge** (DAB) converter is studied with a single current control loop on a bus type load, modeled as a voltage source with a series resistor ("ERL"). The voltage source represents the voltage at the operating point analyzed, whereas the series resistor models the bus resistance.

The name ("*V1 to V2*") indicates that the direction of the power transfer is from the bridge whose voltage is denoted V1 (on the left in the picture) to the port with the voltage V2 (on the right).

The current I2 (output average current at Bridge 2) is the one controlled.

Further considerations

•This study helps the control design of a battery charger during the fixed-current stages

•The power losses are not considered in the theoretical study

•To consider that the switching is done under ZVS (*Zero Voltage Switching*) conditions, the value of the current at the switching instant must be:

o≥ $I_{ZVS,Bridge\ 1\ (Q1-Q3)}$ in Q1 and Q3 transistors of Bridge 1

o≥ $I_{ZVS,Bridge\ 1\ (Q2-\ Q4)}$ in Q2 y Q4 transistors of Bridge 1

o≥ $I_{ZVS,Bridge\ 2}$ in the transistors located in Bridge 2

$$I_{ZVS,Bridge\ 1\ (Q1-Q3)} = V_1\sqrt{\frac{2Coss_1}{L}} - \left[\frac{V_2\left({}^{2\varphi(°)}/_{180} - 1\right)}{4 \cdot L_m \cdot n \cdot F_{sw}}\right] \cdot \sqrt{\frac{L_m}{L}}$$

$$I_{ZVS,Bridge\ 1\ (Q2-Q4)} = V_1 \sqrt{\frac{2Coss_1}{L} + \left[\frac{V_2\left({}^{2\varphi(°)}/_{180} - 1\right)}{4 \cdot L_m \cdot n \cdot F_{sw}}\right] \cdot \sqrt{\frac{L_m}{L}}}$$

$$I_{ZVS,Bridge\ 2} = V_2 \sqrt{\frac{2Coss_2}{L}}$$

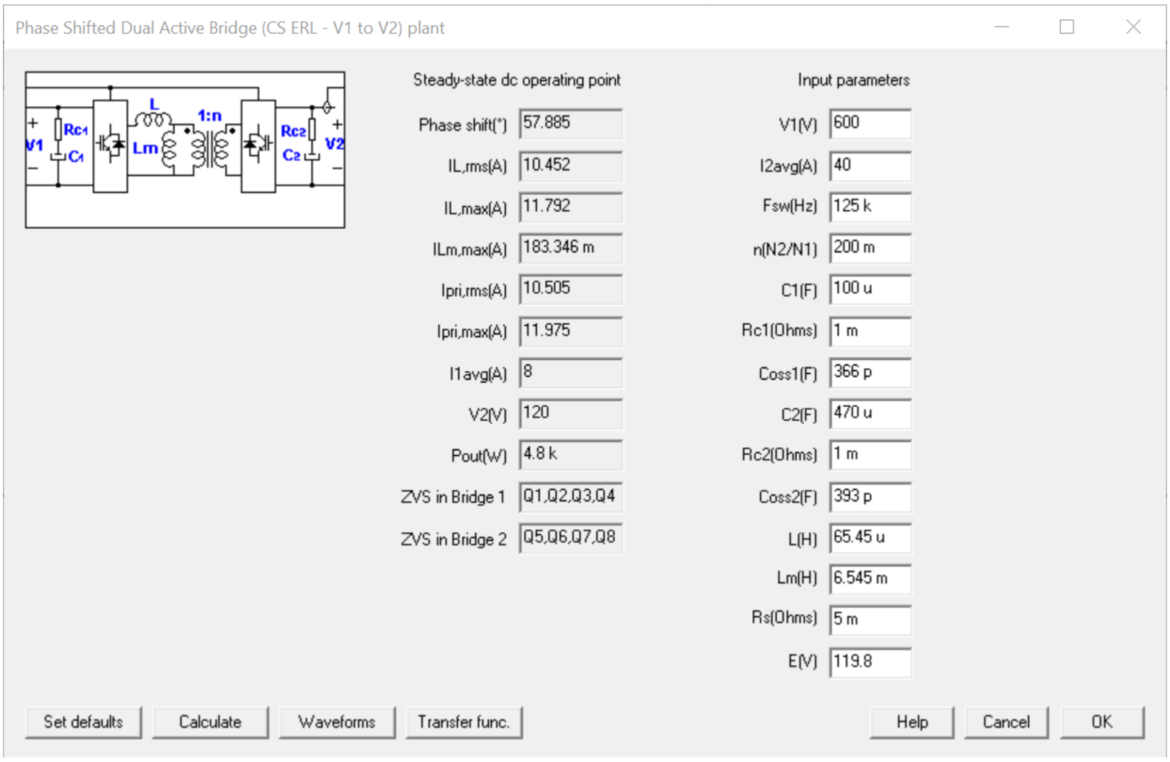
•The input impedance (Zi) calculation considers the input filter (C1 + Rc1)

•The output impedance (Zo) calculation considers the output filter (C2 + Rc2)

•**When exporting the schematic to PSIM,** a series resistance to the inductor L (ESL) of 0.1Ω and series resistance to the magnetizing inductance Lm (ESLm) of 1Ω are considered to help the steady-state to be reached earlier in the simulation. Those are not considered in the theoretical study

•**When exporting the schematic to PSIM,** a death-time of 50ns is considered. The death time is not considered in the theoretical study

The **input data window** allows the user to select the desired input parameters and provides useful information such as the **steady state dc operating point**.



Parameter description in the initial dialogue:

Input parameters:

V1(V) Input voltage (Volts)

I2,avg(A) Average output current (Bridge 2). Controlled. (Amperes)

Fsw(Hz) Switching frequency (Hertz)

n(N2/N1) Turn ratio (dimensionless). It is considered as the number of turns of the secondary N2, divided by the number of turns in the primary N1.

C1(F) Input filter capacitance (Farads)

Rc1(Ohms) Series resistance to the input filter capacitor (Ohms)

Coss1(F) Output parasitic capacitance of the transistors in Bridge 1 (Farads)

C2(F) Output filter capacitance (Farads)

Rc2(Ohms) Series resistance to the output filter capacitor (Ohms)

Coss2(F) Output parasitic capacitance of the transistors in Bridge 2 (Farads)

L(H) Inductance (Henries)

Lm(H) Transformer's magnetizing inductance referred to the primary (Henries)

Rs(Ohms) Series resistance in the bus load

E(V) Voltage at the operating point

Steady-state dc operating point:

Phase Shift (°) The phase shift between Bridge 1 and Bridge 2 (degrees). It is defined as the time elapsed between the turn-on of transistor Q1 and the turn-on of transistor Q5 related to the period (= 1/Fsw). Control variable. To calculate:

$$\varphi(°) = 180 \cdot \left[\frac{1}{2} - \frac{\sqrt{\left(\frac{1}{F_{sw}}\right) \cdot V_1^2 \cdot V_2^2 - 8 \cdot L \cdot P_{out} \cdot V_1 \cdot V_2}}{2\sqrt{\frac{1}{F_{sw}}} \cdot V_1 \cdot V_2} \right]$$

IL,rms(A) Effective current through L (Amperes)

IL,max(A) Maximum (peak) current through L (Amps). DAB's current through L is AC

ILm,max(A) Maximum (peak) current through Lm (Amperes).

Ipri,rms(A) Effective current at the transformer's primary winding (Amps).

Ipri,max(A) Maximum (peak) current through the transformer's primary winding (Amperes).

I1,avg(A) Average input current (Bridge 1) (Amperes)

V2(V) Output voltage (Volts)

Pout(W) Load power (W)

ZVS in Bridge 1 This field shows which transistors in Bridge 1 meet the constraint to be considered as switching a ZVS-switching. Whether or not ZVS is obtained depends on the operating point and specifications. If no transistors meet the constraint, the message "None" is displayed.

ZVS in Bridge 2 This field shows which transistors in Bridge 2 meet the constraint to be considered as switching with ZVS. Whether or not ZVS is obtained depends on the operating point and specifications. If no transistors meet the constraint, the message "None" is displayed.

Waveforms displayed

•**Bridges differential voltages vs time**: signals V11 and V22 are displayed simultaneously. These signals are important as they show the phase difference between the bridges, which determines the transferred power.

oThe signal V11 refers to the differential voltage between the midpoint of the transistor branches of Bridge 1. In the equation they appear in lower case because they are time-dependent:

$$v_{11} = v_{DS,Q2} - v_{DS,Q4}$$

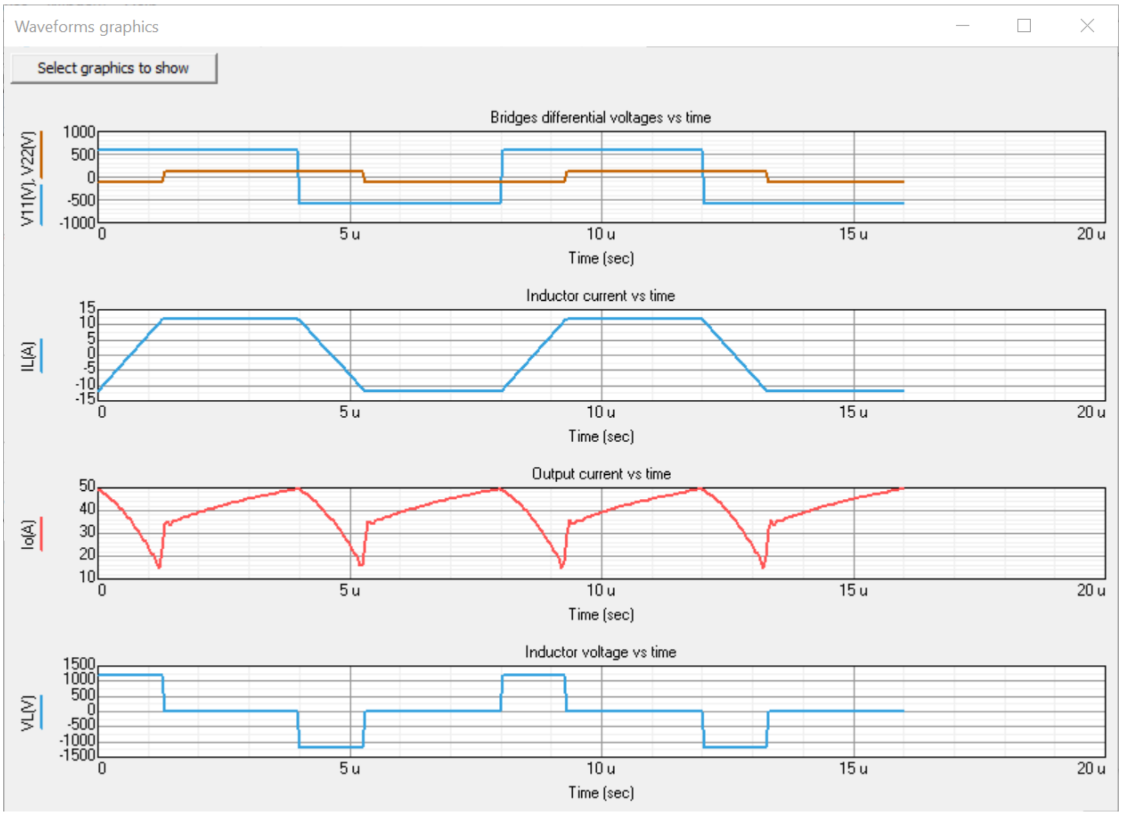
oThe signal V22refers to the differential voltage between the midpoint of the transistor branches of Bridge 2. In the equation they appear in lower case because they are time-dependent:

$$v_{22} = v_{DS,Q6} - v_{DS,Q8}$$

•Inductor current vs time

•**Output current vs time**: This is the average current controlled, I2.

•Inductor voltage vs time



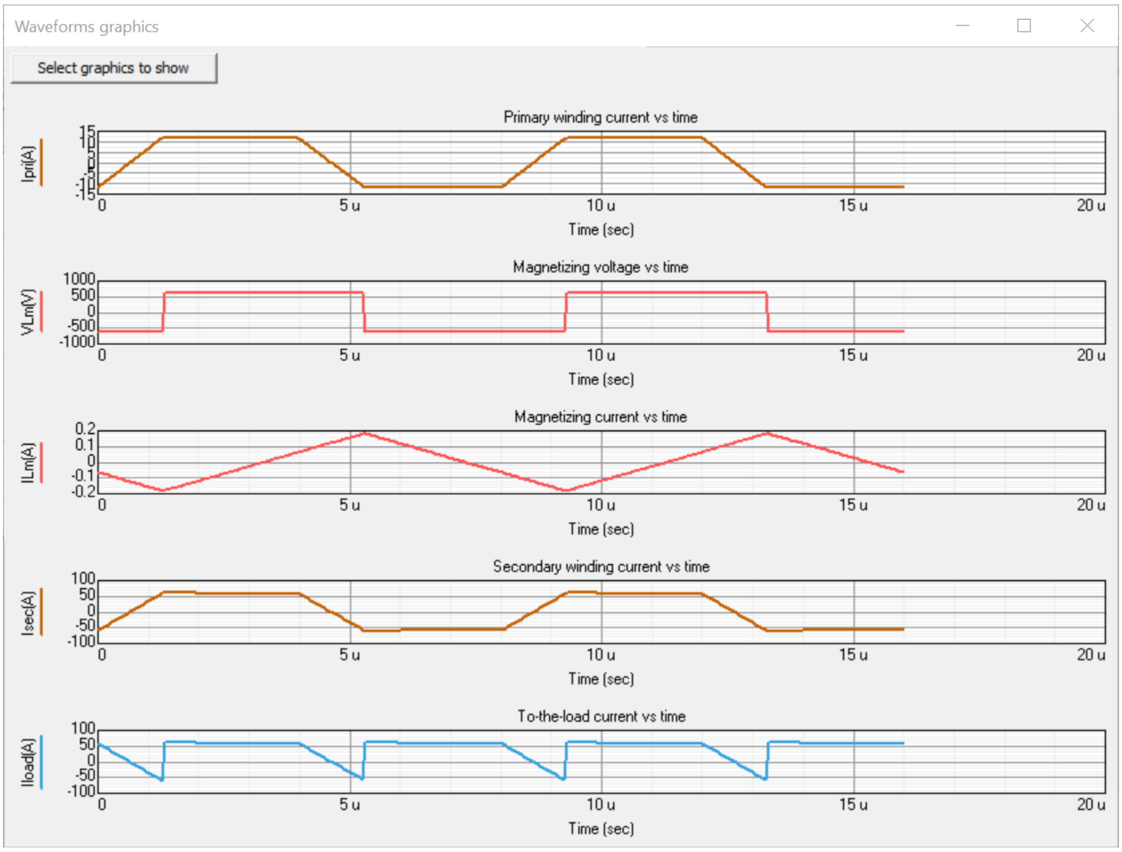
•Primary winding current vs time

•Magnetizing voltage vs time

•Magnetizing current vs time

•Secondary winding current vs time

•**To-the-load current vs time:** It is the filtered current flowing through the load, in this case, R.



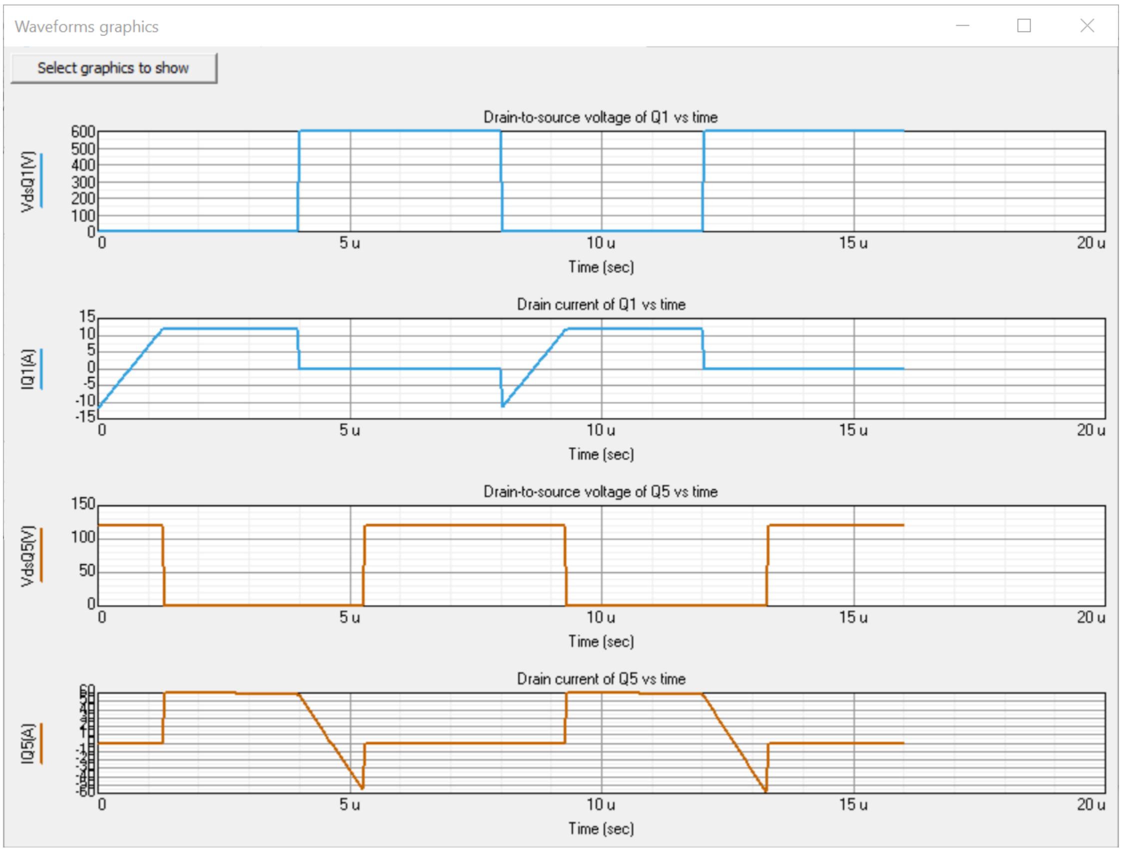
•Drain-to-source voltage of Q1 vs time: Drain-to-source voltage on transistor Q1 (Bridge 1, external branch, above). If it has the value V1, transistor Q1 is open. The falling edge of this signal is considered the start of the phase shift time and coincides with the rising edge of the *Phase Shift* signal in the SMC main window.

•Drain current of Q1 vs time: Q1s drain current. Being smaller than

$I_{ZVS,Bridge\ 1\ (Q1-Q3)}$ at the turning-on means that the transistor has ZVS.

•Drain-to-source voltage of Q5 vs time: Drain-to-source voltage on transistor Q5 (Bridge 2, inner branch, above). If it has the value V2, transistor Q5 is open. The falling edge of this signal is considered the end of the phase-shift time and coincides with the falling edge of the *Phase Shift* signal in the SMC main window.

•**Drain current of Q5 vs time:** Q5s drain current. Being smaller than $I_{ZVS,Bridge\ 2}$ at the turning-on means that the transistor has ZVS.



Phase Shift waveform interpretation

In the power stages with PWM modulation the waveform that usually appears in this location is the switching signal of the transistor that commands the operation.

In this case (and in the Full-Bridge plant introduced in the previous SMC update) the phase-shift time is shown, which is the control variable in a *Phase Shift* modulation. As can be seen in the picture below, the rising edge refers to the triggering of transistors Q1 and Q3, while the falling edge refers to the triggering of transistors Q5 and Q8.

The classic Phase shift modulation proposed to govern the DAB consists of dephasing the turning-on of the Q5-Q6 branch from the Q1-Q2 branch, to transfer power from Bridge 1 to Bridge 2 (POSITIVE phase shift).

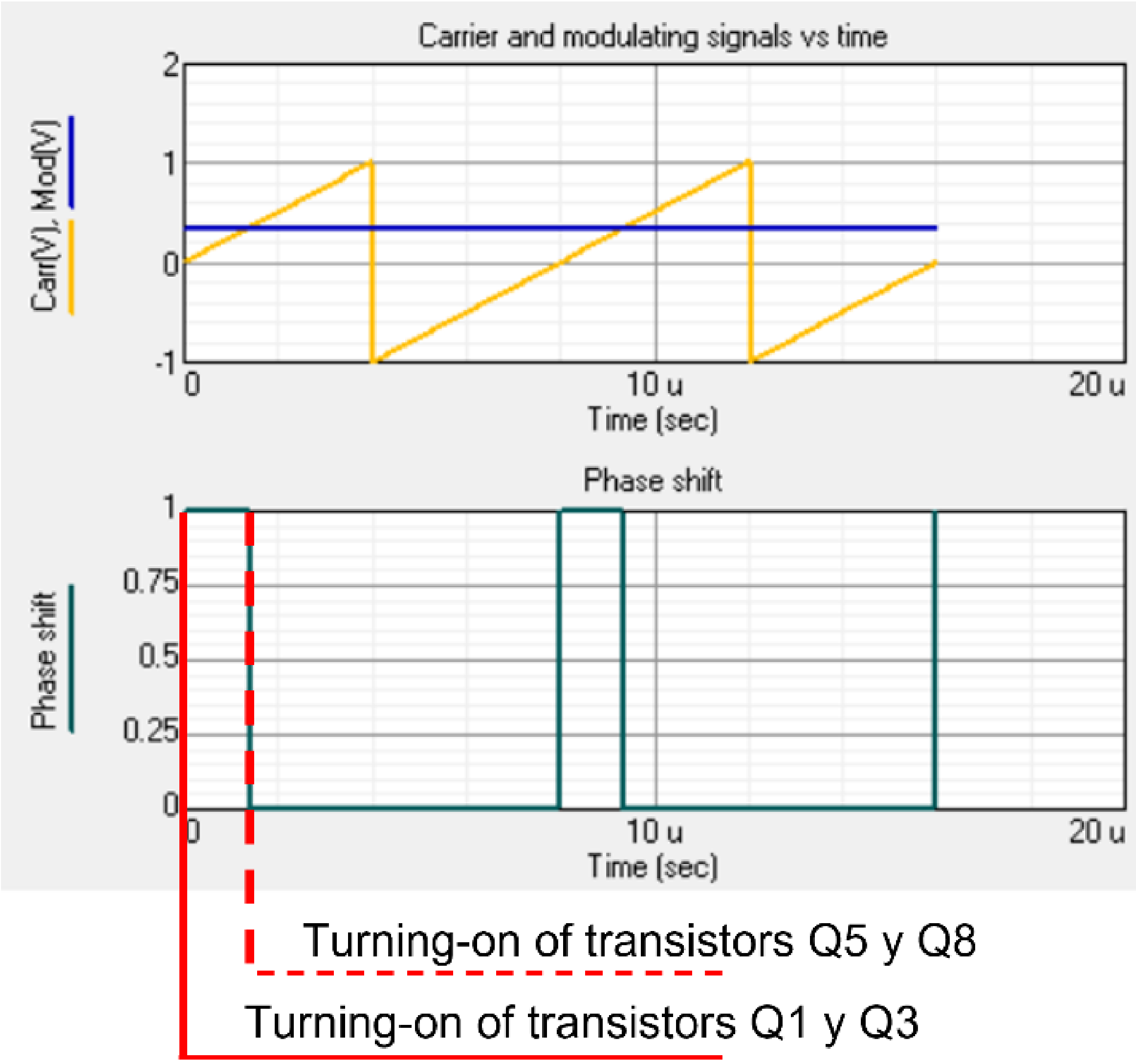
- The transistors in each branch are controlled complementary (ideally with no dead time) and remain on for half the period = $1/(2 \cdot F_{SW})$.

- The transistors in each Bridge are controlled as explained below:

  - In Bridge 1, Q1 and Q4 are turned on simultaneously. Q2 and Q3 operate the remaining half-period once the Q1 and Q4 are turned off.

  - In Bridge 2, Q5 and Q8 are turned on simultaneously. Q6 and Q7 operate the remaining half-period once the Q5 and Q8 are turned off.

Thus, from the representation of the Phase Shift waveform, the operation of all transistors in the DAB can be deduced.



SmartCtrl modulator when used for Phase Shift modulation and gain modification

In the SmarCtrl 5.0 version, the image of the modulator is maintained with respect to the PWM basic one, although in this case, it would be representing a modulator that generates the driving signals of all the transistors of Bridges 1 and 2 with the phase shift calculated as discussed in the previous section.

The modulator gain expression is shown below. To adjust it to the gain of a known system, the parameters Vp and Vv can be modified (Vv = -Vp)

$$G_{mod} = \frac{2}{(V_p - V_v)}$$

1.8 Three-Phase PFC Boost Converter

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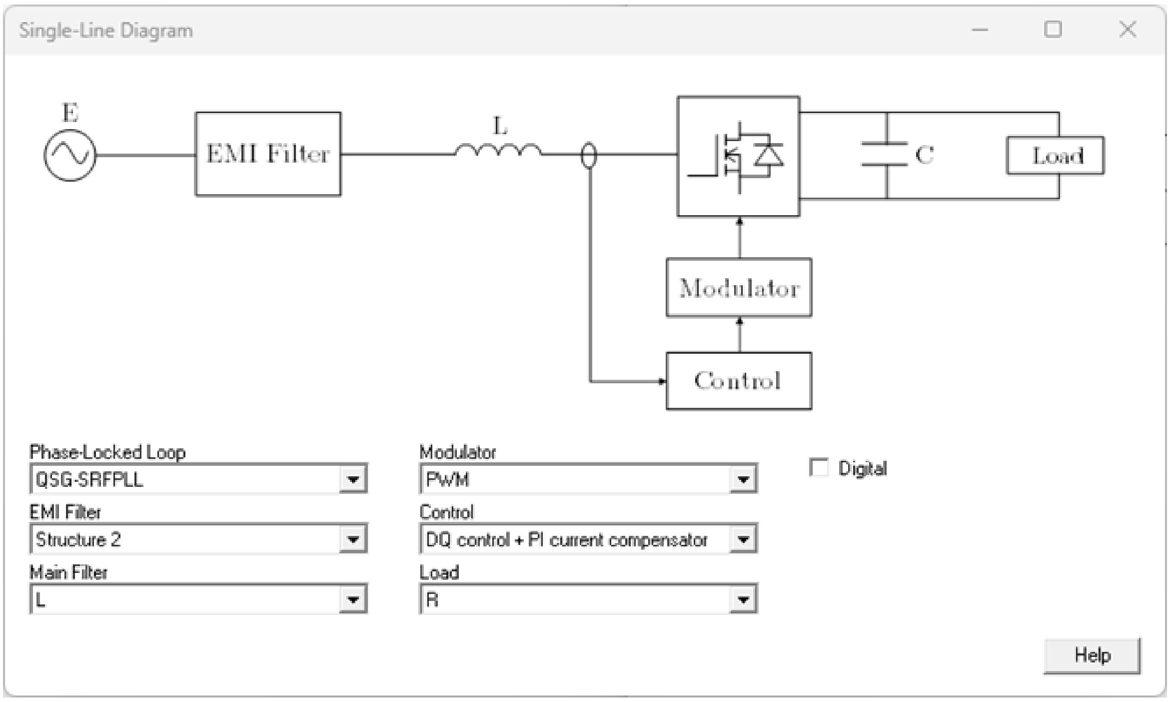
Three-Phase PFC Boost Converter Previous Top Next

1.8.1 Single-Line Diagram

Navigation: SmartCtrl > Three-Phase PFC Boost Converter >

Single-Line Diagram Previous Top Next

This window shows a simplified representation of the whole system. The single line diagram allows the user to configure different types of control, modulators, loads and filters.



The drop-down list called “Control” allows the user to choose different types of controls.

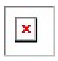
- Alpha-Beta control + PI current compensator (Proportional-Integral compensator)
- Alpha-Beta control + PR current compensator (Proportional-Resonant compensator)
- DQ control + PI current compensator (Proportional-Integral compensator)

If the dq control option is chosen then the drop-down list called "Phase-Locked Loop" is enabled, which allows the user to choose different types of PLLs.

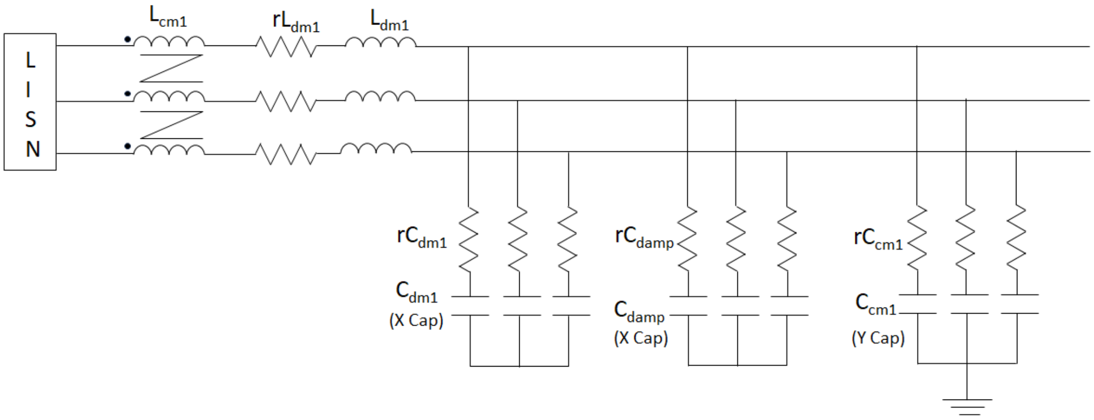
- SRFPLL: Synchronous Reference Frame PLL
- QSG-SRFPLL: Quadrature Signal Generator - Synchronous Reference Frame PLL

The drop-down list called “EMI Filter” allows the user to choose different types of EMI Filter.

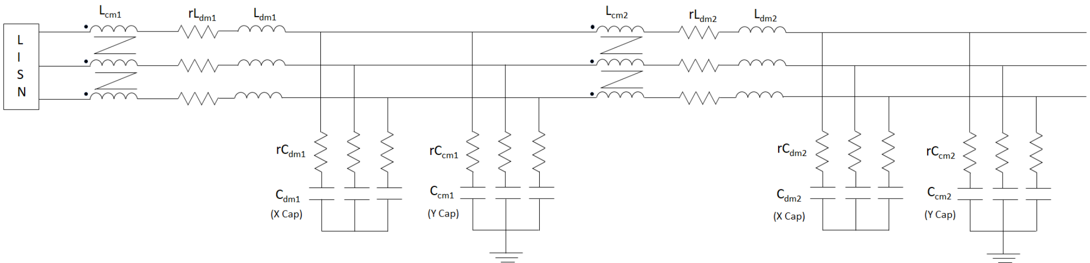
- Structure 1: One stage of differential mode and one stage of common mode.



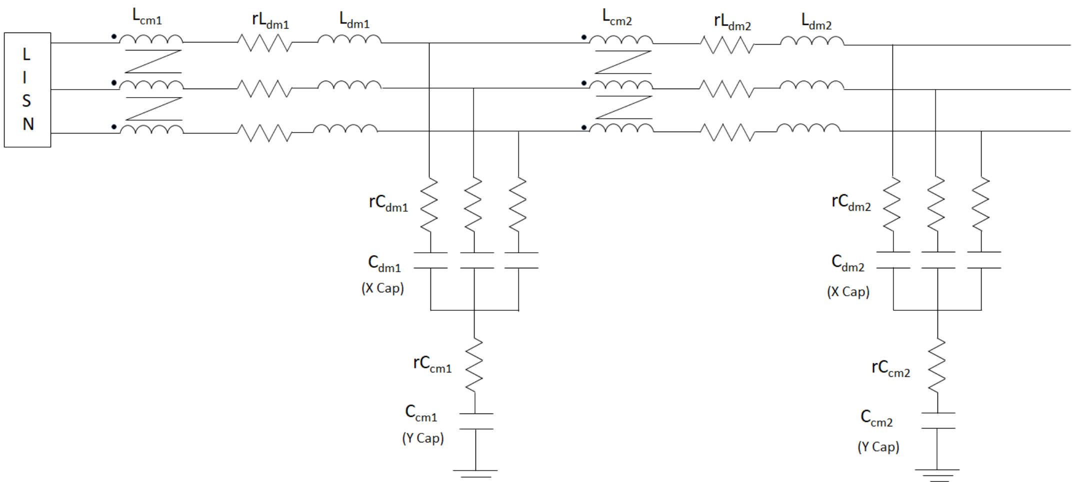
- Structure 2: One stage of differential mode with damping network and one stage of common mode.



- Structure 3: Two stages of differential mode and two stages of common mode.



- Structure 4: Two stages of differential mode and two stages of common mode with capacitor connected to the neutral point.



- N/A: Not applicable.

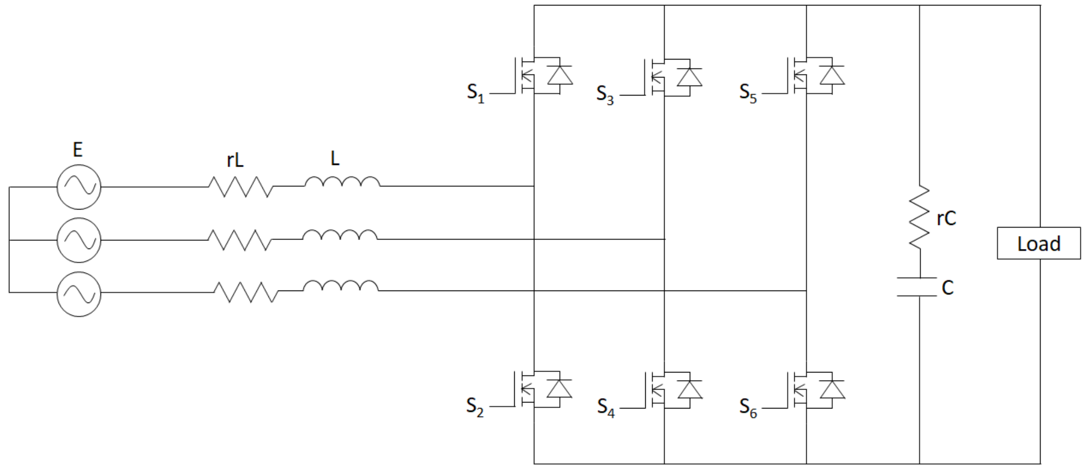
The drop-down list called “Load” allows the user to choose different types of loads.

- R: Simple resistor

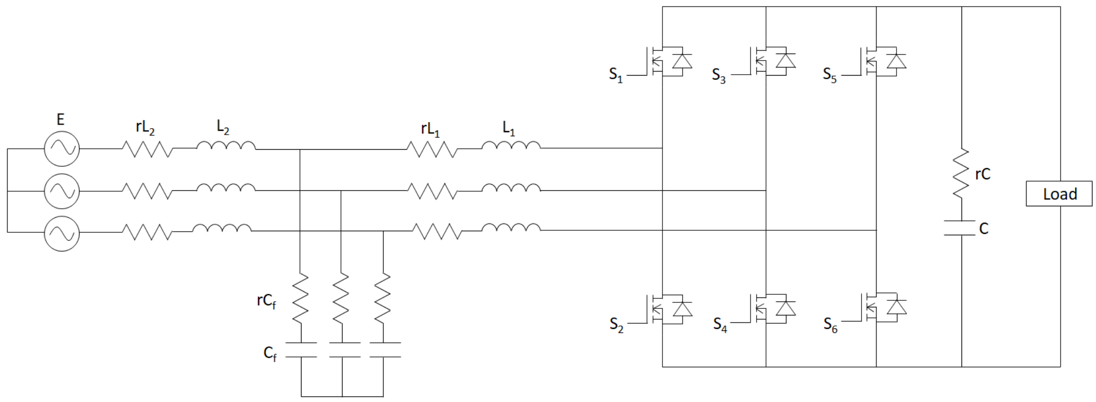
- CPL: Constant Power Load
- I constant: Represents loads with constant current

The drop-down list called “Main Filter” allows the user to choose different types of filters.

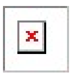
- L: Simple inductor per phase



- LCL: Two inductors and one capacitor per phase
- LCL active damping: Two inductors and one capacitor per phase. In this case it is necessary to sense the capacitor current.

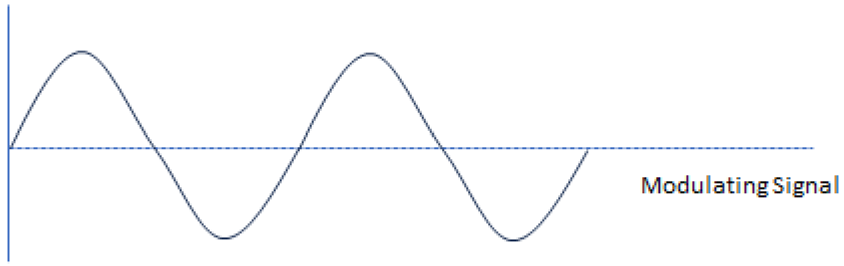


- LCL passive damping: Two inductors and one capacitor per phase. The damping network considers a capacitor and resistor in parallel to the main filter capacitor.

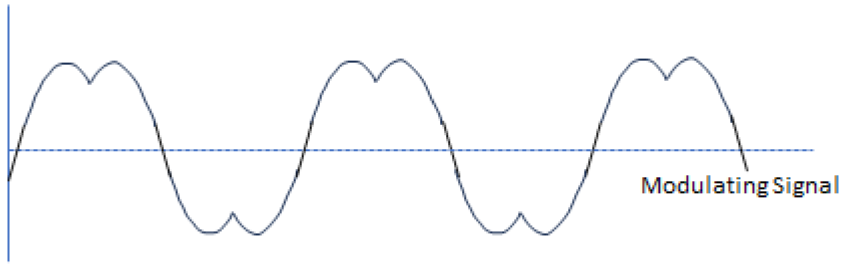


The drop-down list called “Modulator” allows the user to choose different types of modulators.

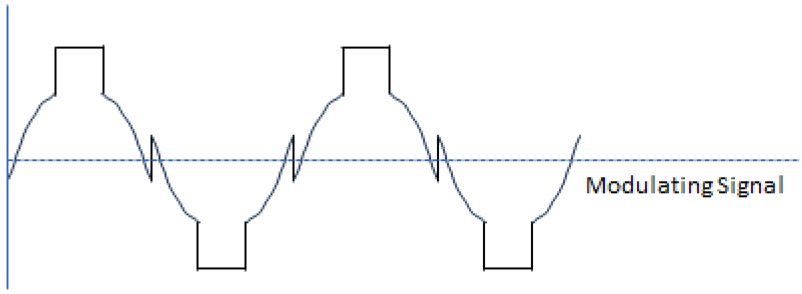
- PWM: Sinusoidal Pulse Width Modulation



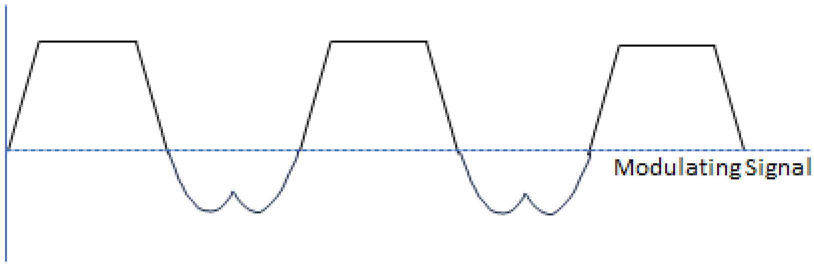
- SVPWM: Space Vector Pulse Width Modulation



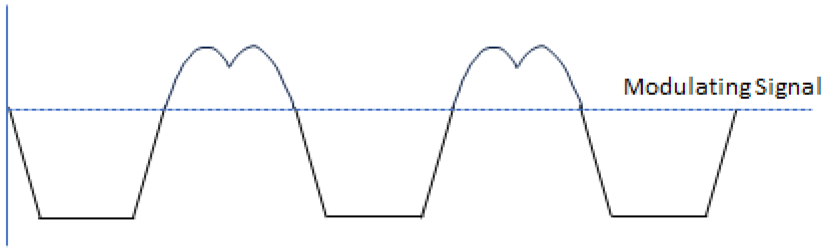
- Discontinuous 1: 60-degree Discontinuous Pulse Width Modulation with positive and negative DC clamping



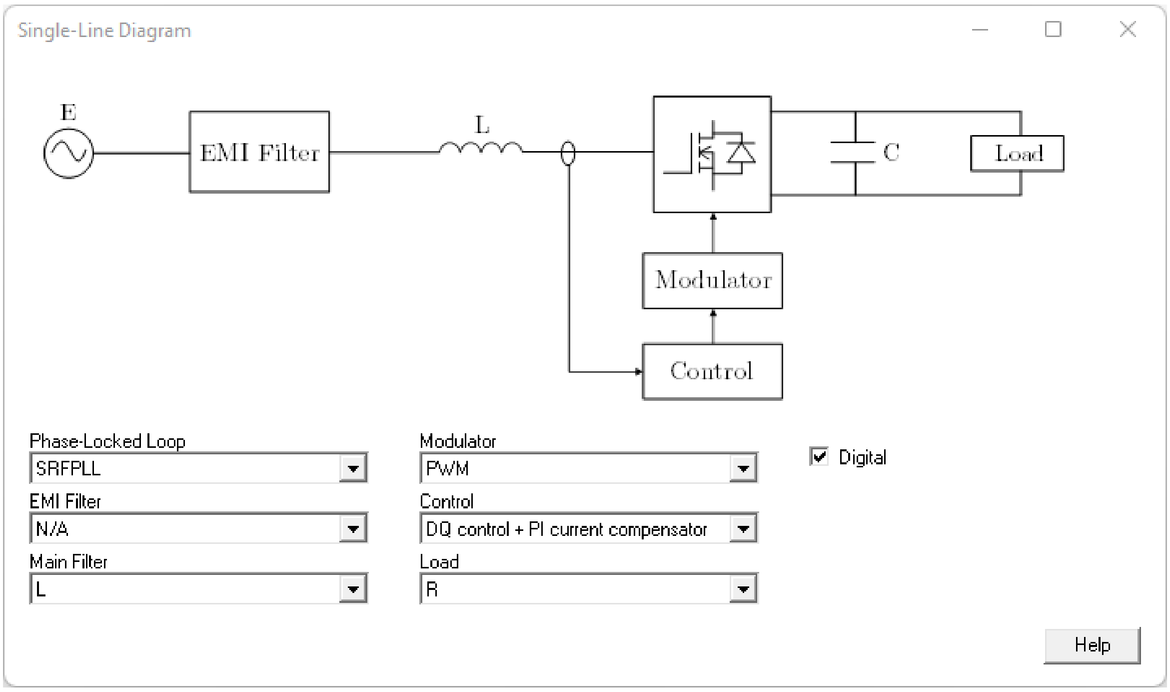
- Discontinuous Max: 120-degree Discontinuous Pulse Width Modulation with positive DC clamping



- Discontinuous Min: 120-degree Discontinuous Pulse Width Modulation with negative DC clamping



The checkbox called "Digital" allows the user to select whether the control to be designed is digital or analog. This checkbox determines the different options that can be selected later.



In the menu bar, the user can select the different input data windows.

SLD Single-Line Diagram window

CTRL Control Structure window

PS Power Stage window

EF EMI Filter window

PLL Phase-Locked Loop window

Current Sensor window

Grid Voltage Sensor window

Output Voltage Sensor_window

Current Compensator window

Modulator window

Output Voltage Compensator window

EMI Filter Attenuation graph

Solutions Map of Phase-Locked Loop

Nyquist Diagram of the Phase-locked Loop

Transient response of the Phase-Locked Loop in small signal

Graph of the transient response of the Phase-Locked Loop considering a phase step

Solutions Map of current loop

Solutions Map of output voltage loop

Bode diagrams of different transfer functions

Schematic of the entire system

The input parameters can be changed at any time as the results obtained are updated automatically.

SmartCtrl calculates the stable solution space in which all the possible combinations of crossover frequency (Fc) and phase margin (PhM) that lead to stable solutions are shown graphically. It is called Solutions Map. The designer is asked to select the crossover frequency and the phase margin just by clicking within the white zone. This option is available only for pre-defined compensators. On the hand, the constants of the compensators can also be defined manually.

It should be remarked that, due to stability constraints, the crossover frequency of the outer loop (Output Voltage Loop) cannot be greater than the crossover frequency of the inner loop (Inductance Current Loop).

The stability of the system can be checked by analyzing the bode diagrams.

SmartCtrl also allows the user to plot the frequency response of the output impedance of the EMI Filter and the input impedance of the three-phase rectifier in order to analyze system-level stability.

Once the control loops have been designed, SmartCtrl allows the user to export the design to third-party simulators .
The third-party simulators that SmartCtrl can export are: PSIM or SIMBA .

1.8.2 System Level Stability Analysis

Navigation: SmartCtrl > Three-Phase PFC Boost Converter >

System Level Stability Analysis

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EMI filter can lead to stability problems due to the interaction between two subsystems. The system level stability can be analyzed using the criterion proposed in the following reference:

R. D. Middlebrook, "Input filter considerations in design and application of switching regulators," in Conf. Rec. IEEE IAS Annu. Meeting, 1976, pp. 366–382.

The Middlebrook criterion establishes that if the magnitude of the output impedance of the EMI filter, Z_o^{EMI} , is much smaller than the magnitude of the input impedance of the three-phase rectifier, Z_{in} , then system stability can be guaranteed. This criterion may result in conservative design.

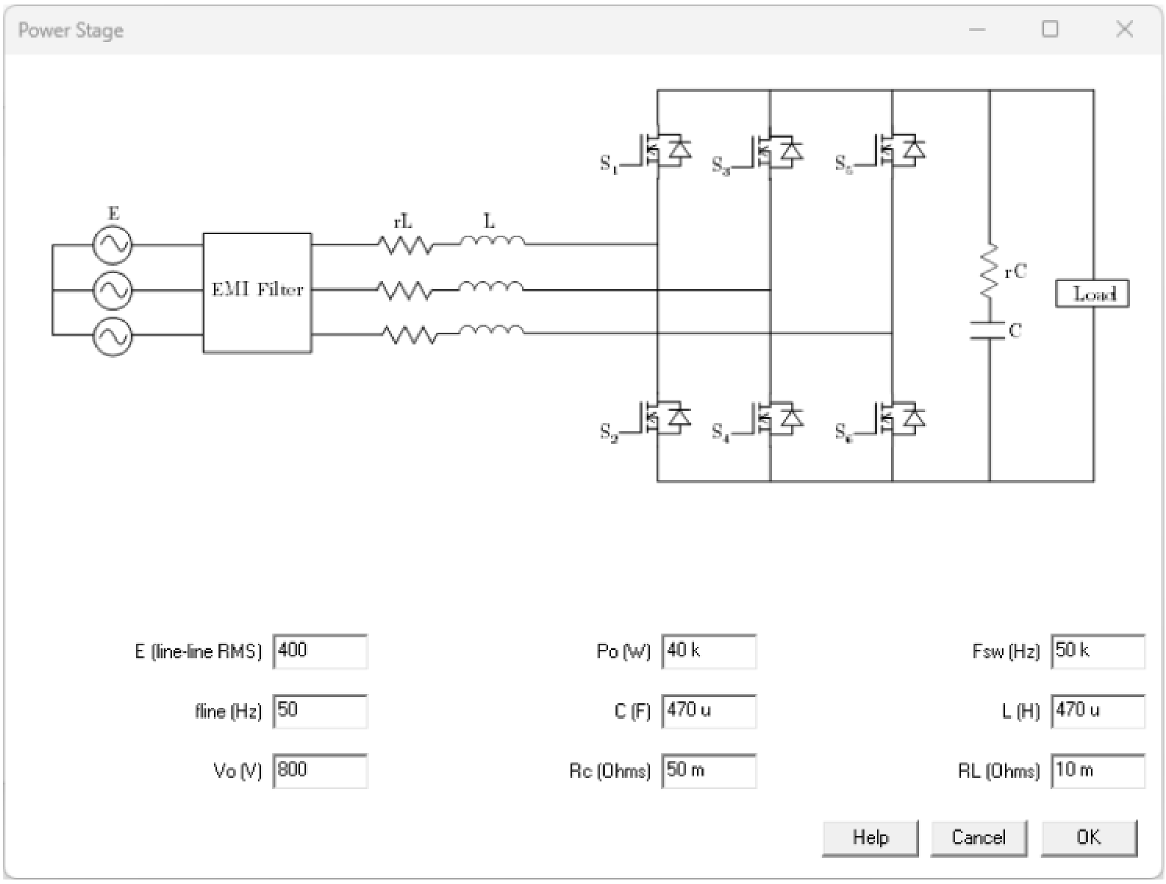
$$\left\|\frac{Z_o^{EMI}}{Z_{in}}\right\| \ll 1$$

Another stability criterion is called Gain Margin and Phase Margin (GMPM) proposed in the following reference: *C. M. Wildrick, F. C. Lee, B. H. Cho, and B. Choi, "A method of defining the load impedance specification for a stable distributed power system," IEEE Trans. Power Electron., vol. 10, no. 3, pp. 280–285, May 1995.*

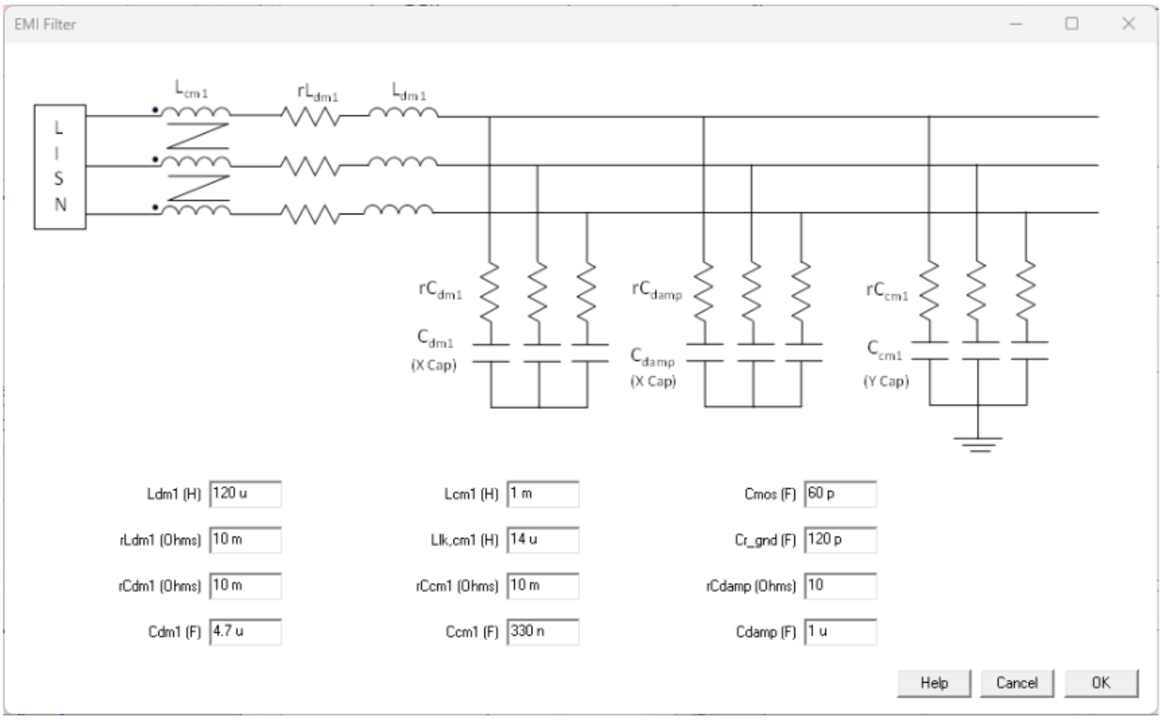
The GMPM criterion is based on analyzing the phase difference at the points where the magnitude of Z_o^{EMI} is equal to the magnitude of Z_{in} then the system could be stable if the absolute value of the phase difference of Z_o^{EMI} and Z_{in} is not greater than 180 degrees in order to satisfy the Nyquist criterion.

$$\left\|\frac{Z_o^{EMI}}{Z_{in}}\right\| \leq 1 \quad and \quad \left|arg(Z_o^{EMI}) - arg(Z_{in})\right| \leq 180^\circ$$

Three examples are given below. The input parameters that the examples have in common are:

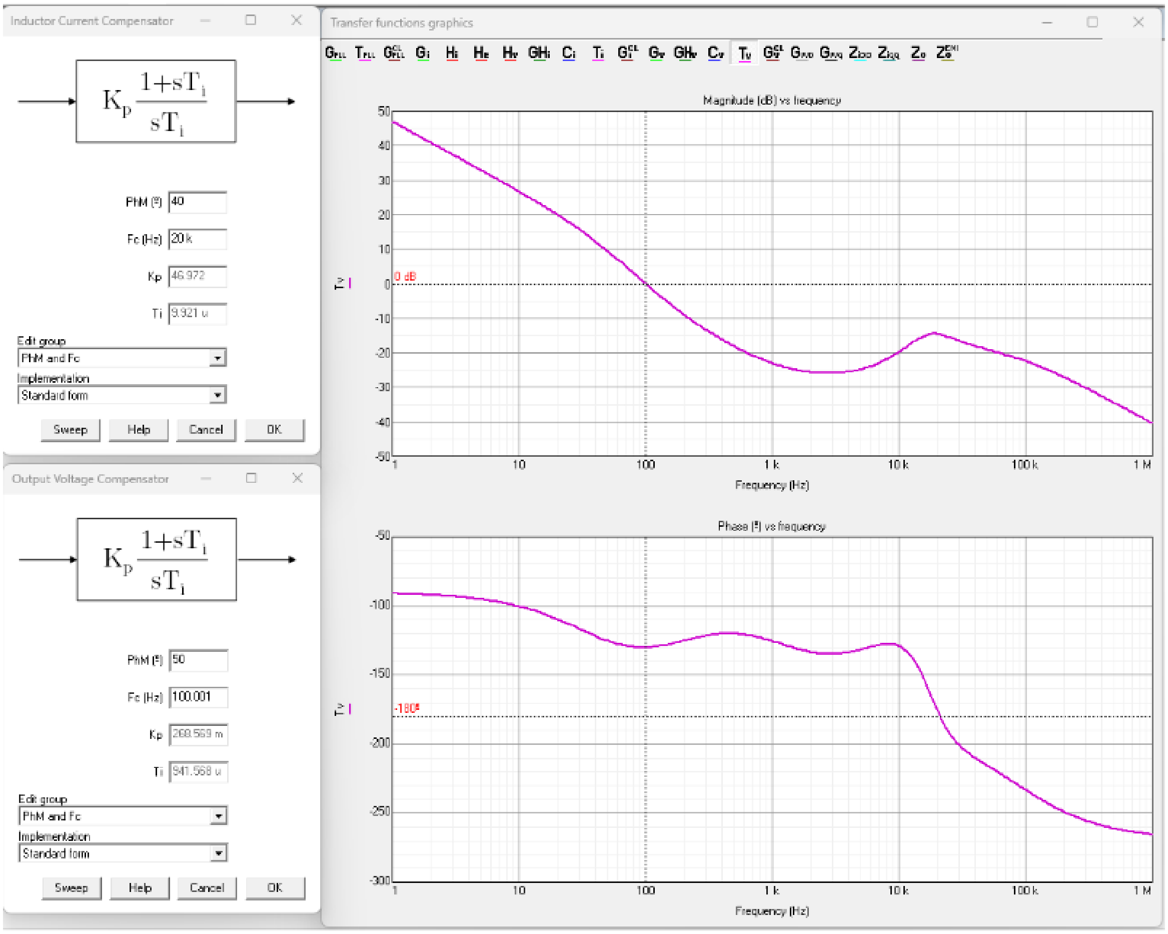


The second EMI filter structure has been chosen. The modulator under consideration is the space vector modulation (SVPWM). DQ Control has been selected as the control structure.



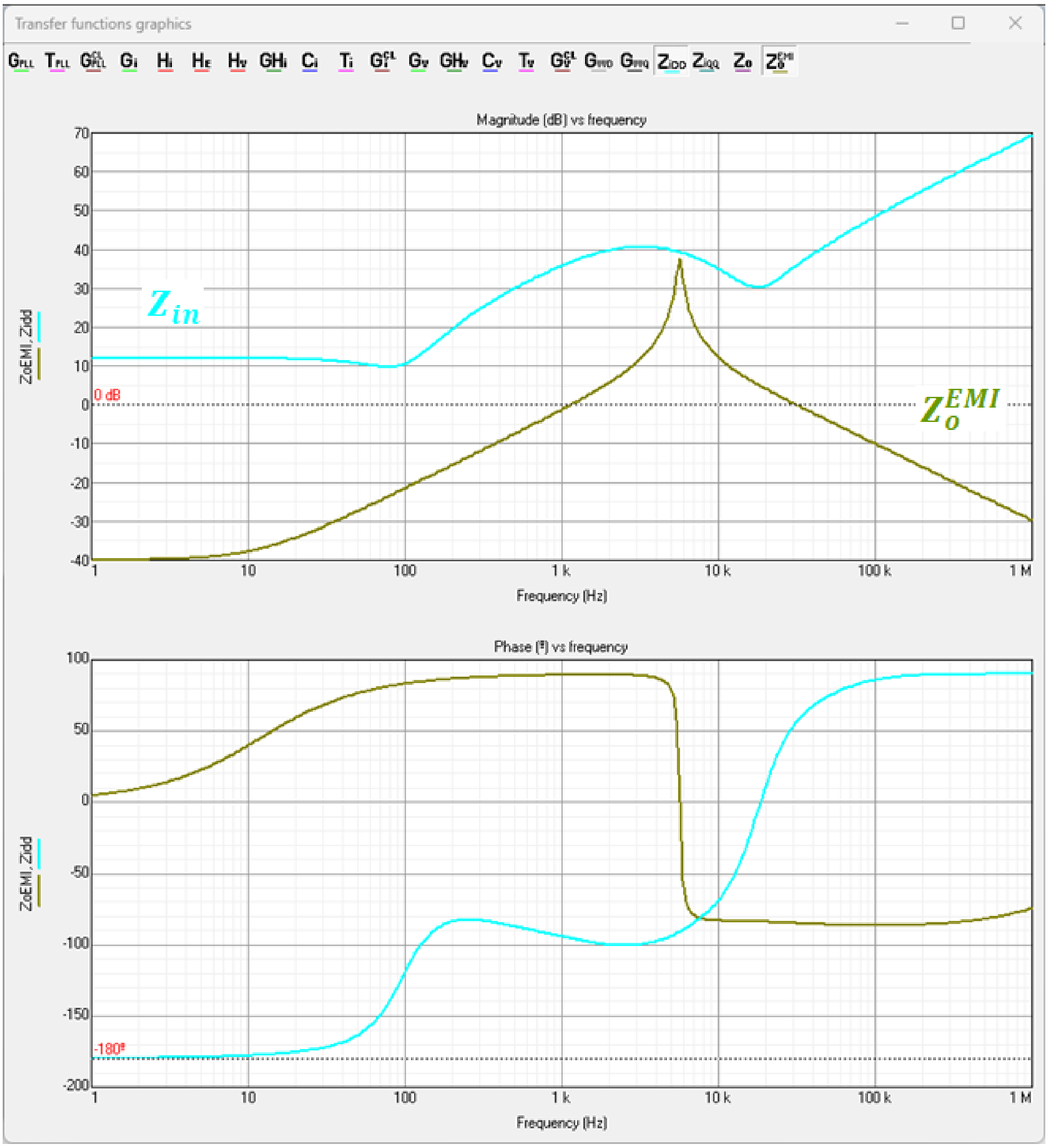
Stable System (Middlebrook criterion)

In the first example, an outer control loop has been designed with a crossover frequency equal to 100 Hz and a phase margin of 50° as shown in the following figure.

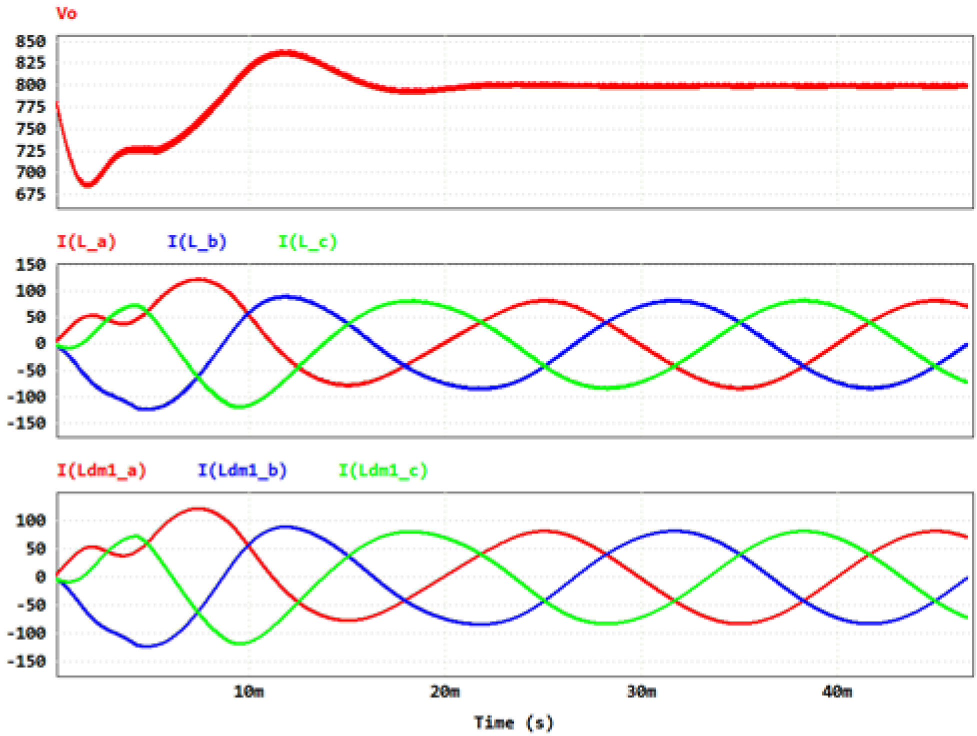


Once the control loops have been designed, the output impedance of the EMI filter and the input impedance of the three-phase rectifier are analyzed.

According to Middlebrook criterion, this system is stable because there is no intersection between the magnitude of the two impedances, as can be seen in the following figure.

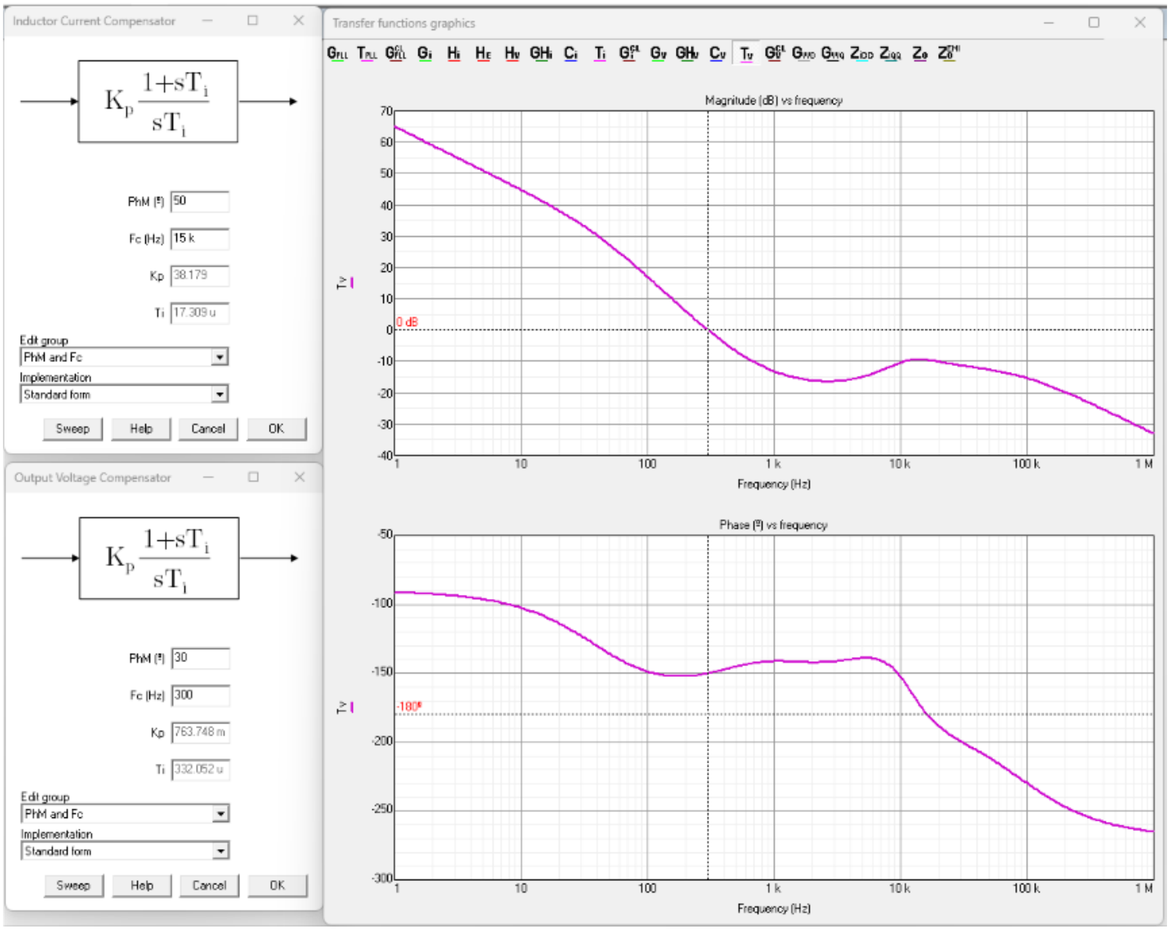


The designed control loops can be validated using any simulator. In this example, it is verified that the system is stable, as can be seen in the following figure.



Stable System (GMPM criterion)

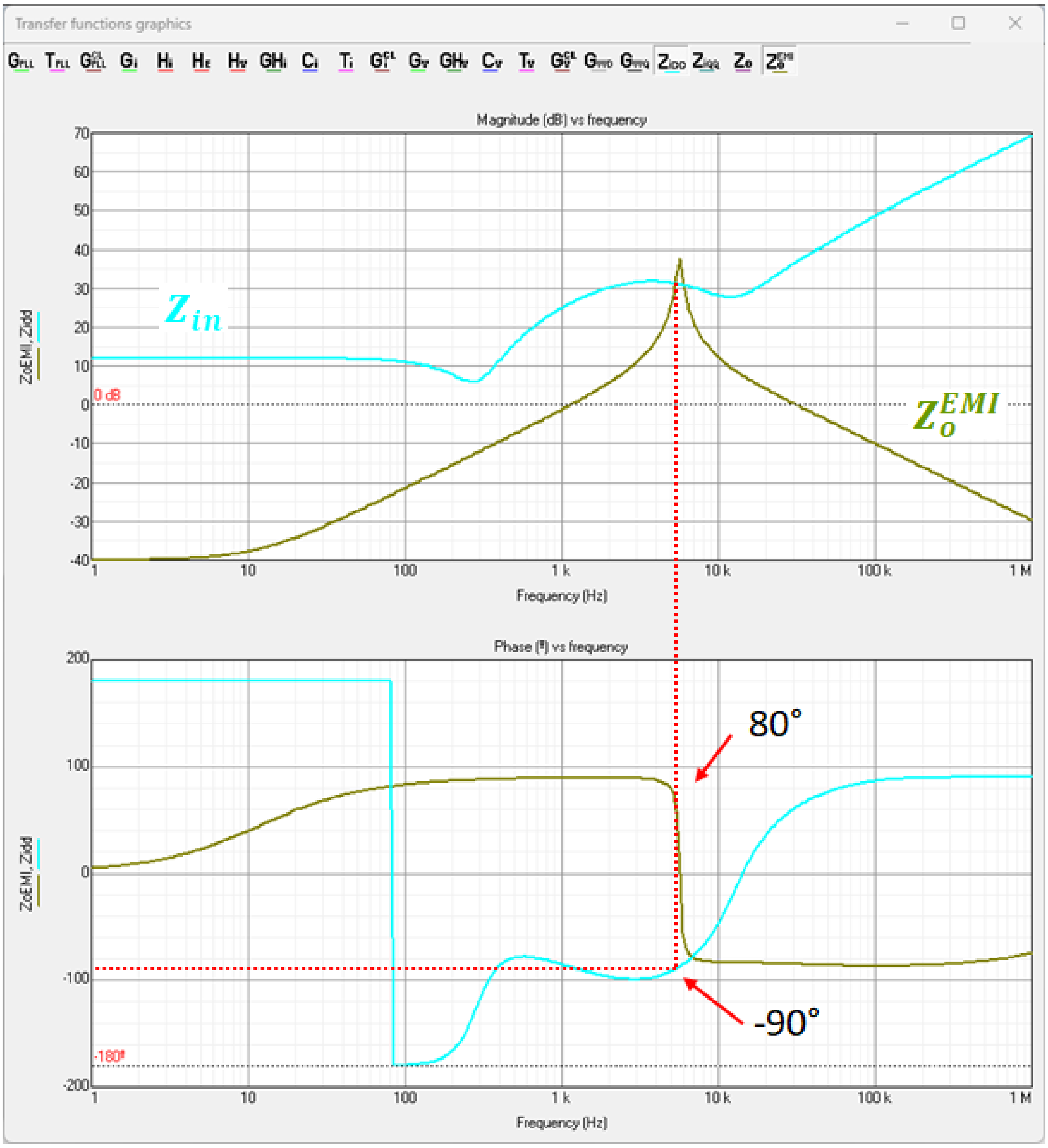
In the second example, an outer control loop has been designed with a crossover frequency equal to 300 Hz and a phase margin of 30° as shown in the following figure.



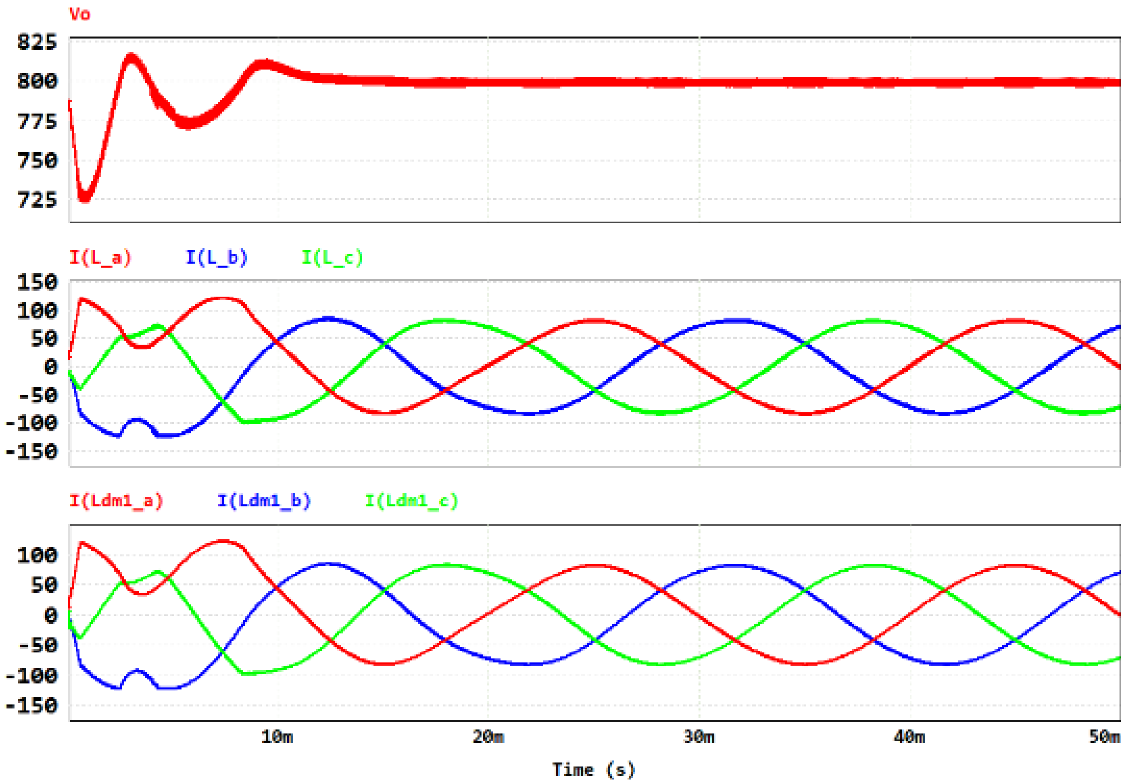
Once the control loops have been designed, the output impedance of the EMI filter and the input impedance of the three-phase rectifier are analyzed.

According to GMPM criterion, the system is stable because the phase difference is less than 180° at the points where the magnitude of Z_o^{EMI} and Z_{in} are equal, as can be seen in the following figure.

$$|arg(Z_o^{EMI}) - arg(Z_{in})| = 80 - (-90) = 170^{\circ}$$

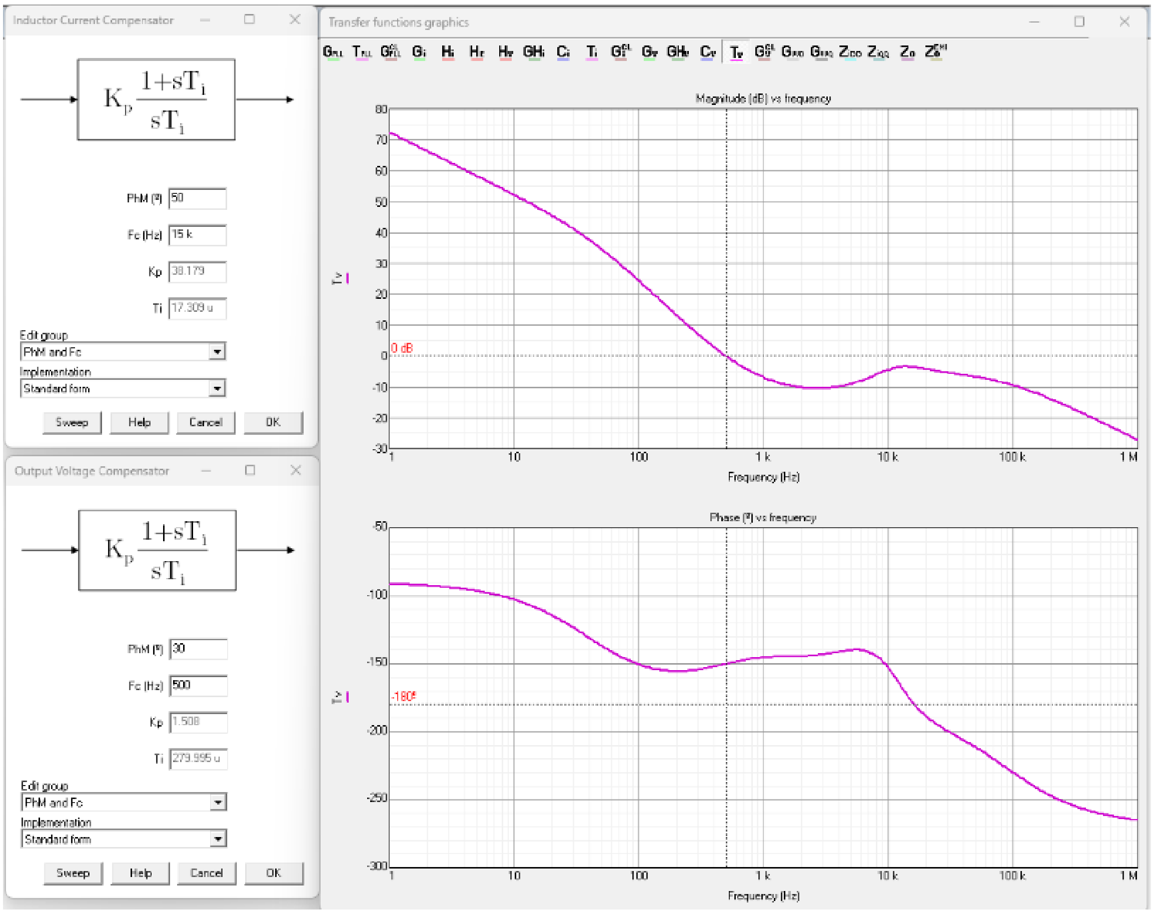


In this example, it is verified that the system is stable, as can be seen in the following figure.



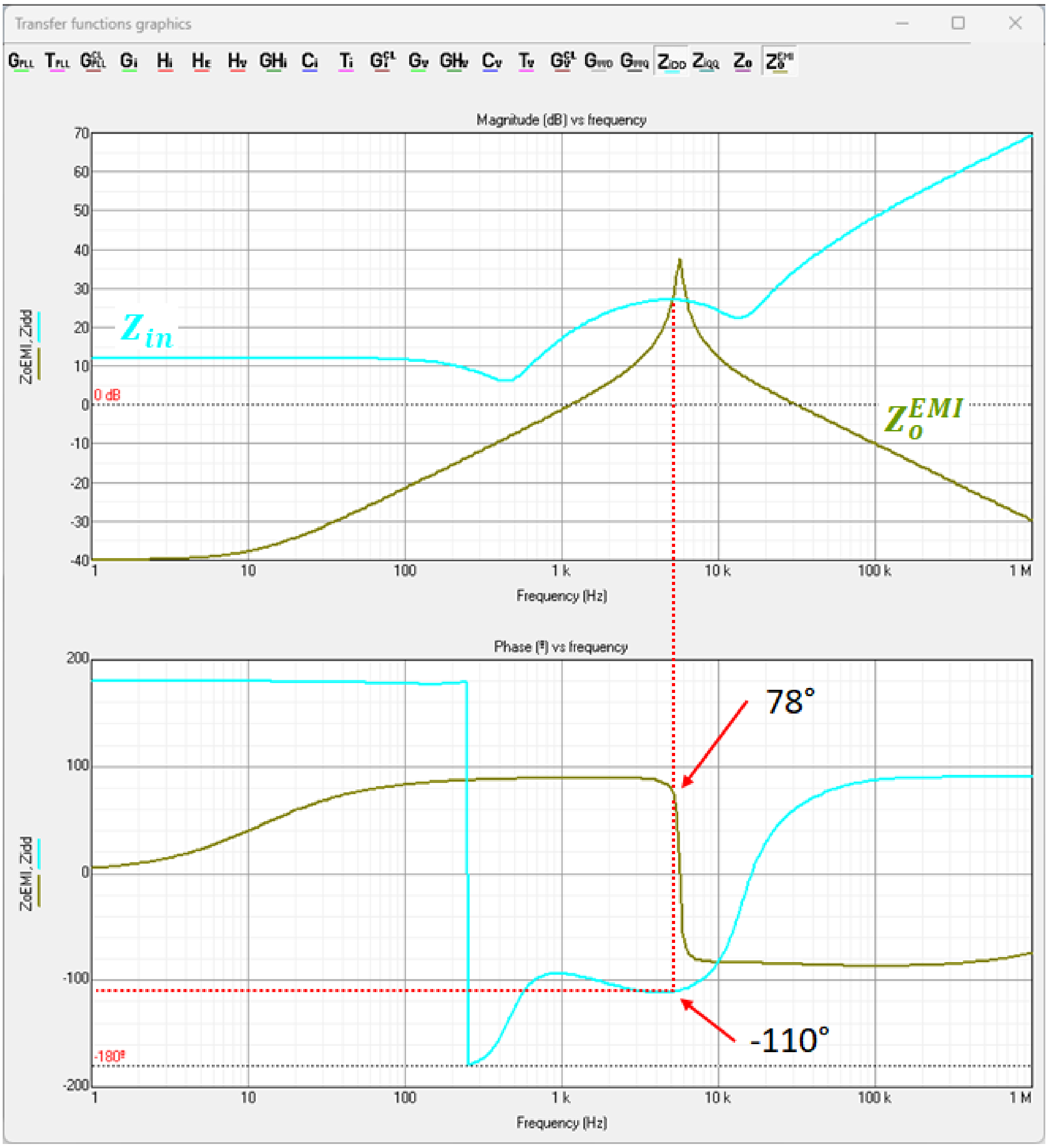
Unstable System

In the third example, an outer control loop has been designed with a crossover frequency equal to 500 Hz and a phase margin of 30° as shown in the following figure.

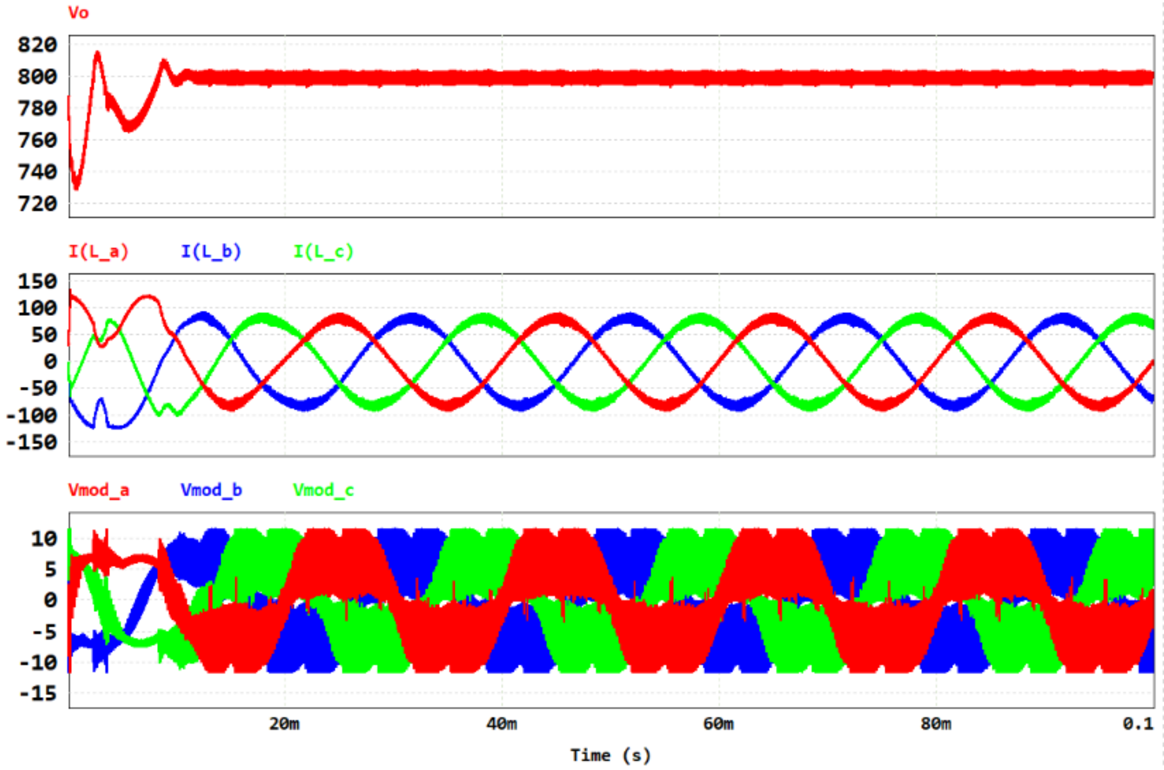


According to GMPM criterion, the system is unstable because the phase difference is greater than 180° at the points where the magnitude of Z_o^{EMI} and Z_{in} are equal, as can be seen in the following figure.

$$\left|arg\left(Z_o^{EMI}\right)-arg\left(Z_{in}\right)\right|= 78 -(-110)= 188^\circ$$



In this example, it is verified that the system is unstable, as can be seen in the following figure.



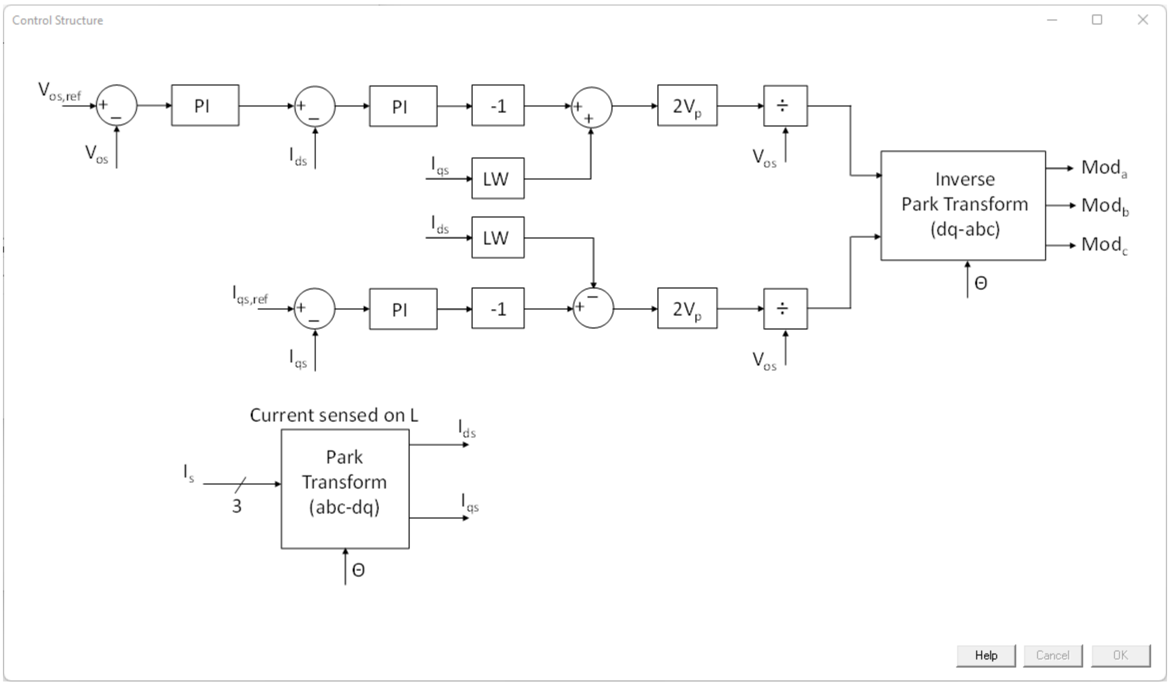
Note: If a d-axis alignment has been chosen in the Phase Locked Loop (PLL) window, then the input impedance to be used in the stability analysis is Z_{idd} , otherwise Z_{iqq} is used.

1.8.3 Control Structure

Navigation: SmartCtrl > Three-Phase PFC Boost Converter >

Control Structure Previous Top Next

This window shows only the control structure. No parameters are defined in this window.



1.8.4 Power Stage

Navigation: SmartCtrl > Three-Phase PFC Boost Converter >

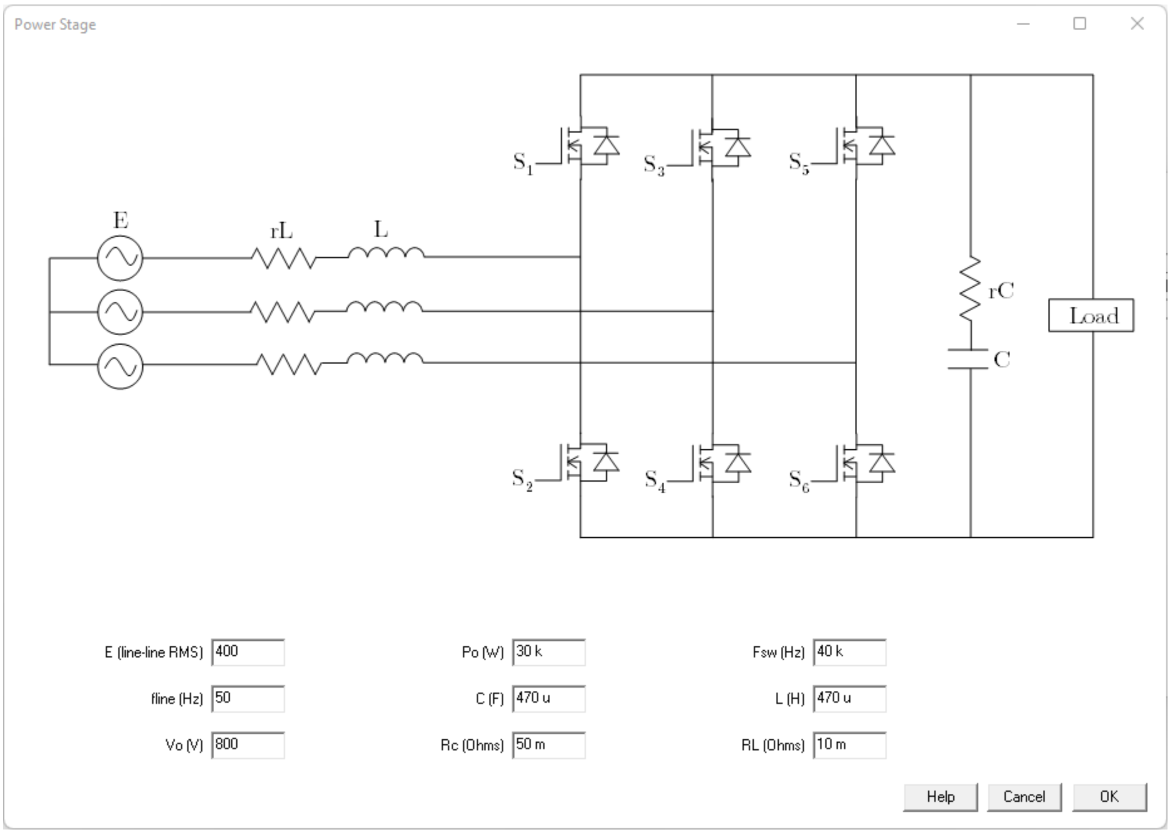
Power Stage Previous Top Next

1.8.4.1 L

Navigation: SmartCtrl > Three-Phase PFC Boost Converter > Power Stage >

L Previous Top Next

The power stage window allows the user to select the desired input parameters.



The parameters of the converter:

E	Line-to-line Grid Voltage (VRMS)
Fline	Grid Frequency (Hz)
Vo	Output Voltage (V)
Po	Output Power (W)
C	Output Capacitor (F)
Rc	Equivalent Series Resistor of the output capacitor (ohms)
Fsw	Switching Frequency (Hz)
L	Converter-side Inductance (H)
RL	Equivalent Series Resistor of the converter-side Inductance (ohms)

1.8.4.2 LCL

Navigation: SmartCtrl > Three-Phase PFC Boost Converter > Power Stage >

LCL

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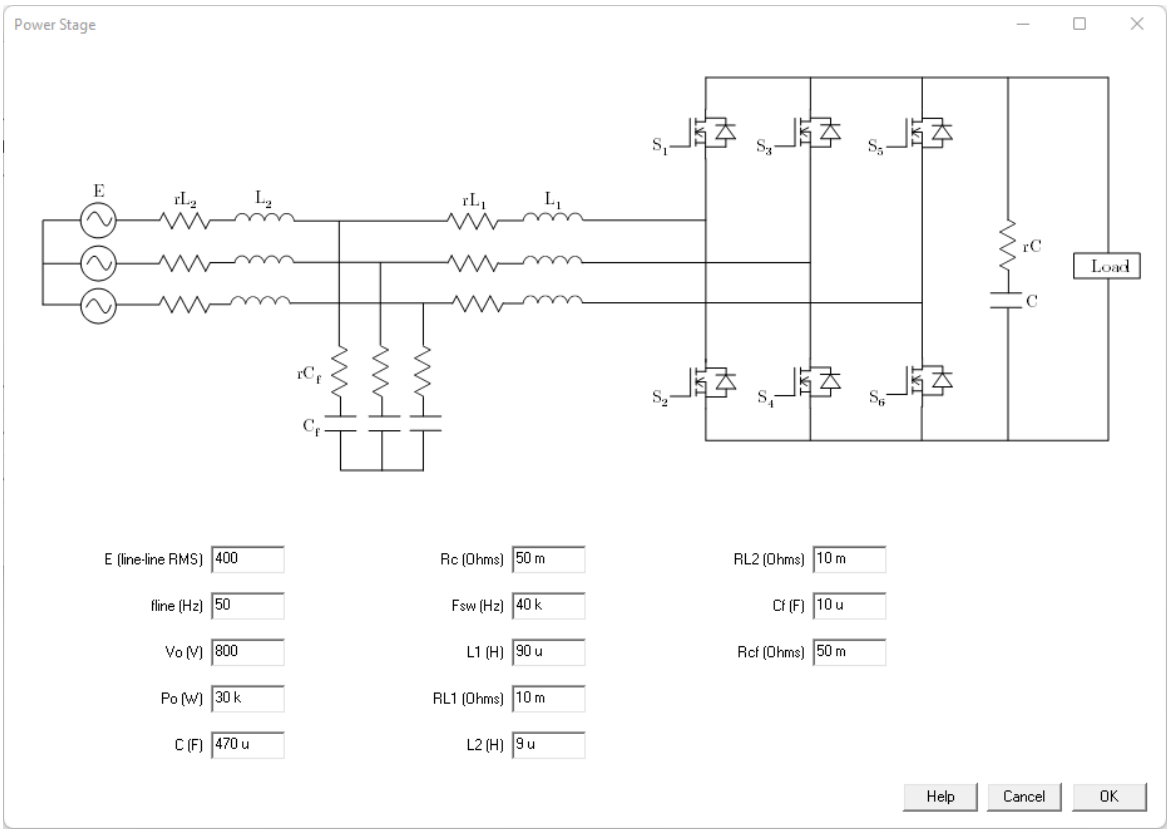
The power stage window allows the user to select the desired input parameters.



The parameters of the converter:

E	Line-to-line Grid Voltage (VRMS)
Fline	Grid Frequency (Hz)
Vo	Output Voltage (V)
Po	Output Power (W)
C	Output Capacitor (F)
Rc	Equivalent Series Resistor of the output capacitor (ohms)
Fsw	Switching Frequency (Hz)
L1	Converter-side Inductance (H)
RL1	Equivalent Series Resistor of the converter-side Inductance (ohms)
L2	Grid-side Inductance (H)
RL2	Equivalent Series Resistor of the grid-side Inductance (ohms)
Cf	AC Capacitor of the LCL filter (F)

Rcf Equivalent Series Resistor of the AC Capacitor of the LCL

1.8.4.3 LCL Active Damping

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LCL Active Damping

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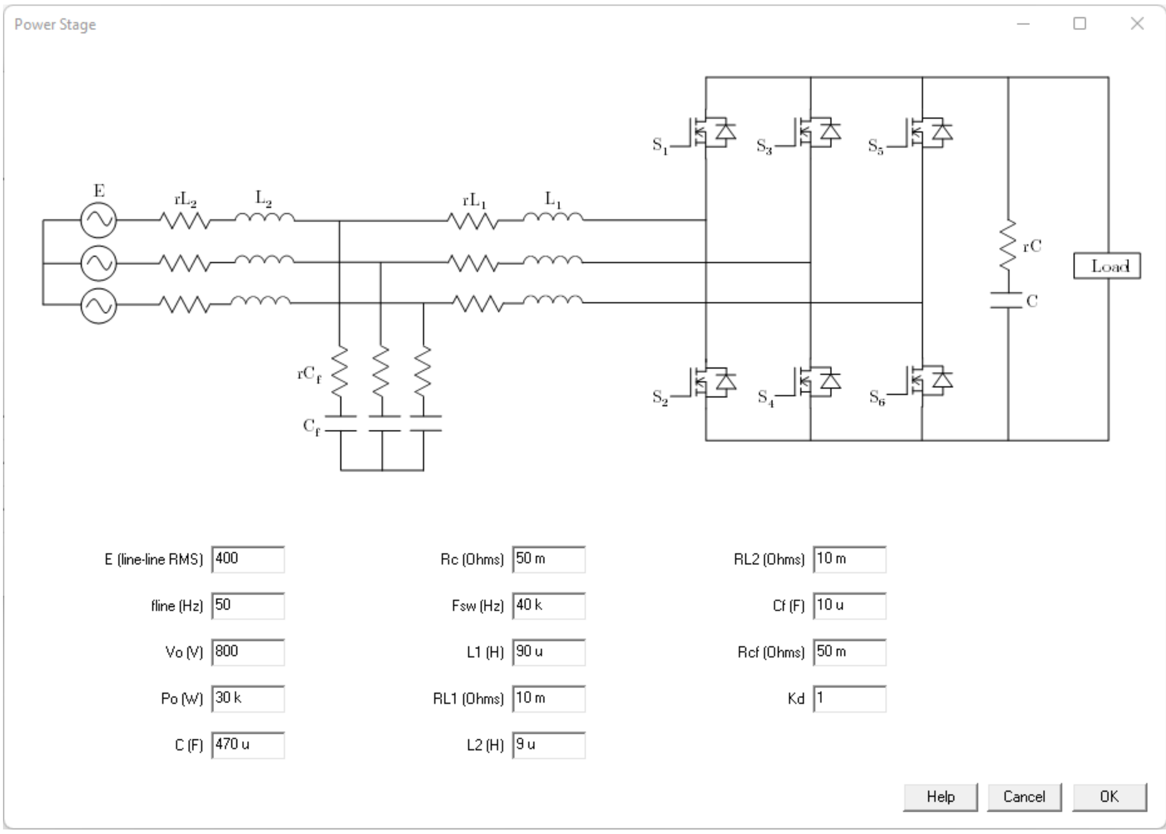
The power stage window allows the user to select the desired input parameters.



The parameters of the converter:

E Line-to-line Grid Voltage (VRMS)

Fline Grid Frequency (Hz)

Vo Output Voltage (V)

Po Output Power (W)

C Output Capacitor (F)

Rc Equivalent Series Resistor of the output capacitor (ohms)

Fsw Switching Frequency (Hz)

L1 Converter-side Inductance (H)

RL1 Equivalent Series Resistor of the converter-side Inductance (ohms)

L2 Grid-side Inductance (H)

RL2 Equivalent Series Resistor of the grid-side Inductance (ohms)

Cf AC Capacitor of the LCL filter (F)

Rcf Equivalent Series Resistor of the AC Capacitor of the LCL filter (ohms)

Kd Active damping loop gain

1.8.4.4 LCL Passive Damping

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LCL Passive Damping

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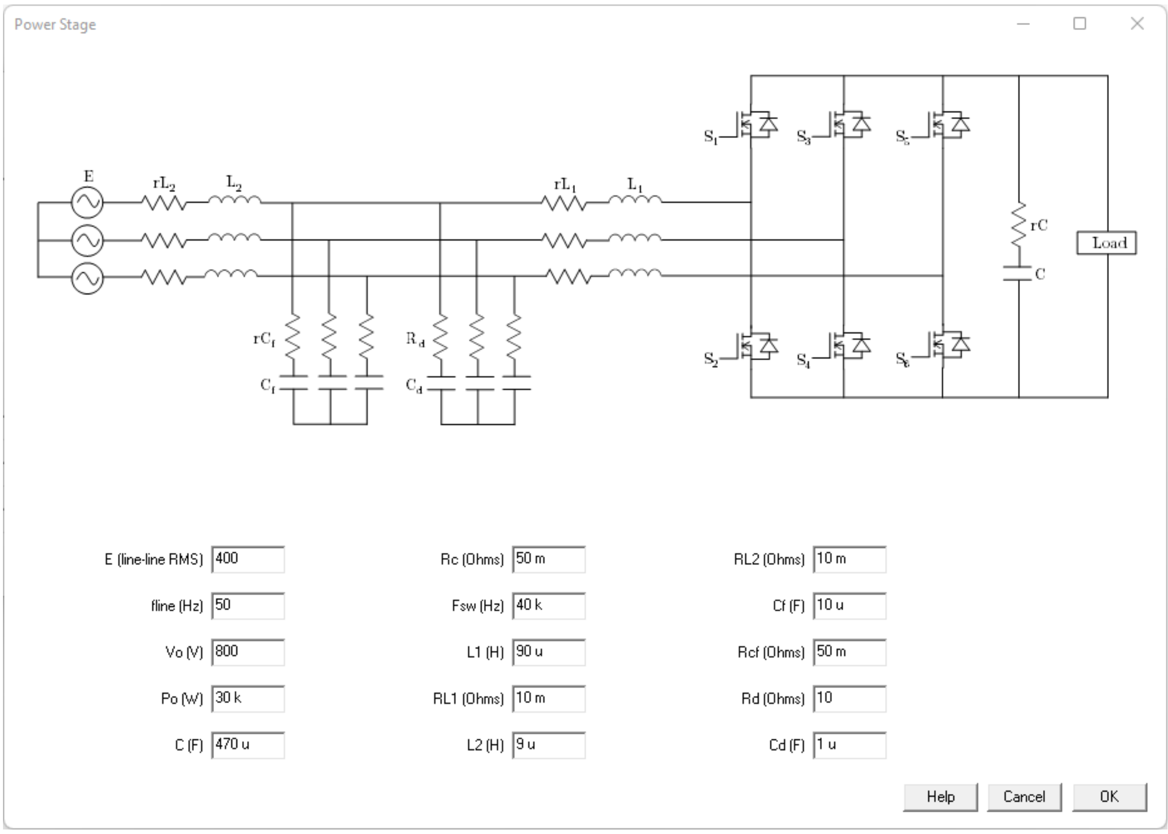
The power stage window allows the user to select the desired input parameters.



The parameters of the converter:

E Line-to-line Grid Voltage (VRMS)

Fline Grid Frequency (Hz)

Vo	Output Voltage (V)
Po	Output Power (W)
C	Output Capacitor (F)
Rc	Equivalent Series Resistor of the output capacitor (ohms)
Fsw	Switching Frequency (Hz)
L1	Converter-side Inductance (H)
RL1	Equivalent Series Resistor of the converter-side Inductance (ohms)
L2	Grid-side Inductance (H)
RL2	Equivalent Series Resistor of the grid-side Inductance (ohms)
Cf	AC Capacitor of the LCL filter (F)
Rcf	Equivalent Series Resistor of the AC Capacitor of the LCL filter (ohms)
Rd	Damping Resistor (ohms)
Cd	Damping Capacitor (F)

1.8.5 EMI Filter

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EMI Filter

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1.8.5.1 Structure 1

Navigation: SmartCtrl > Three-Phase PFC Boost Converter > EMI Filter >

Structure 1

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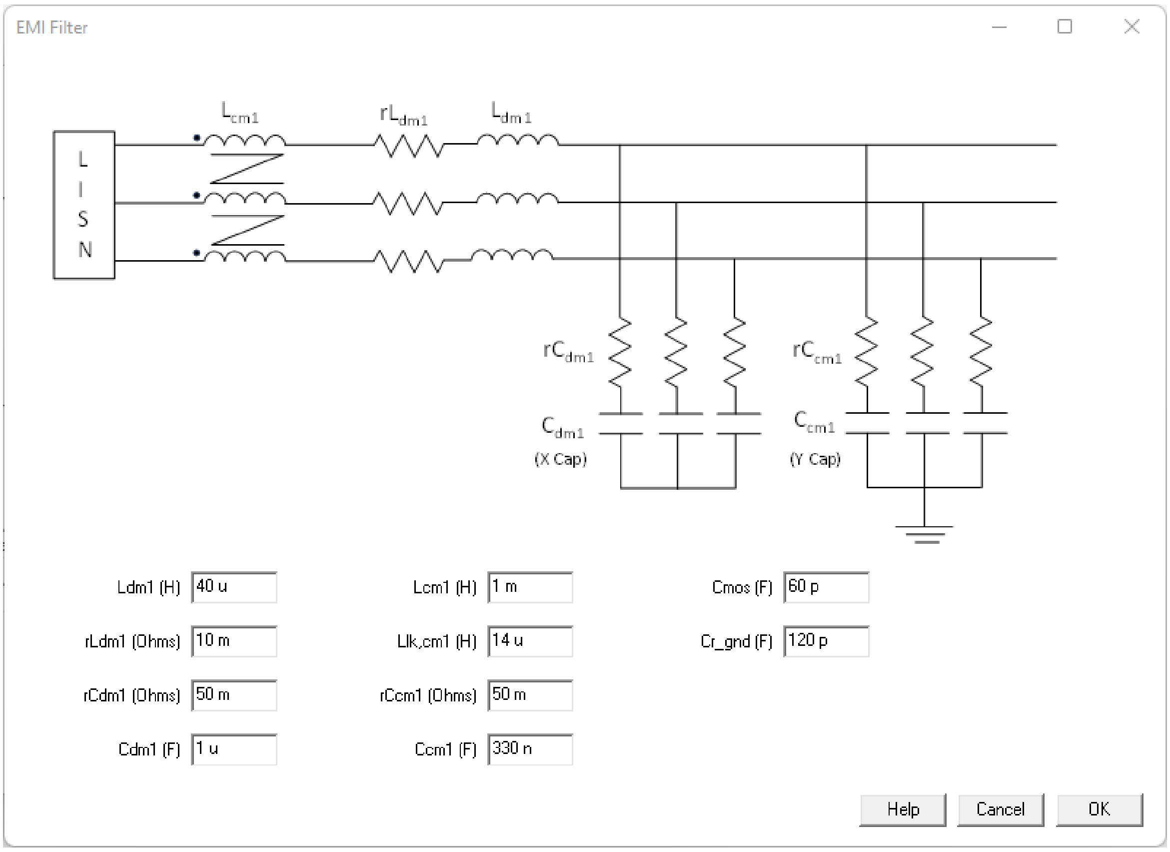
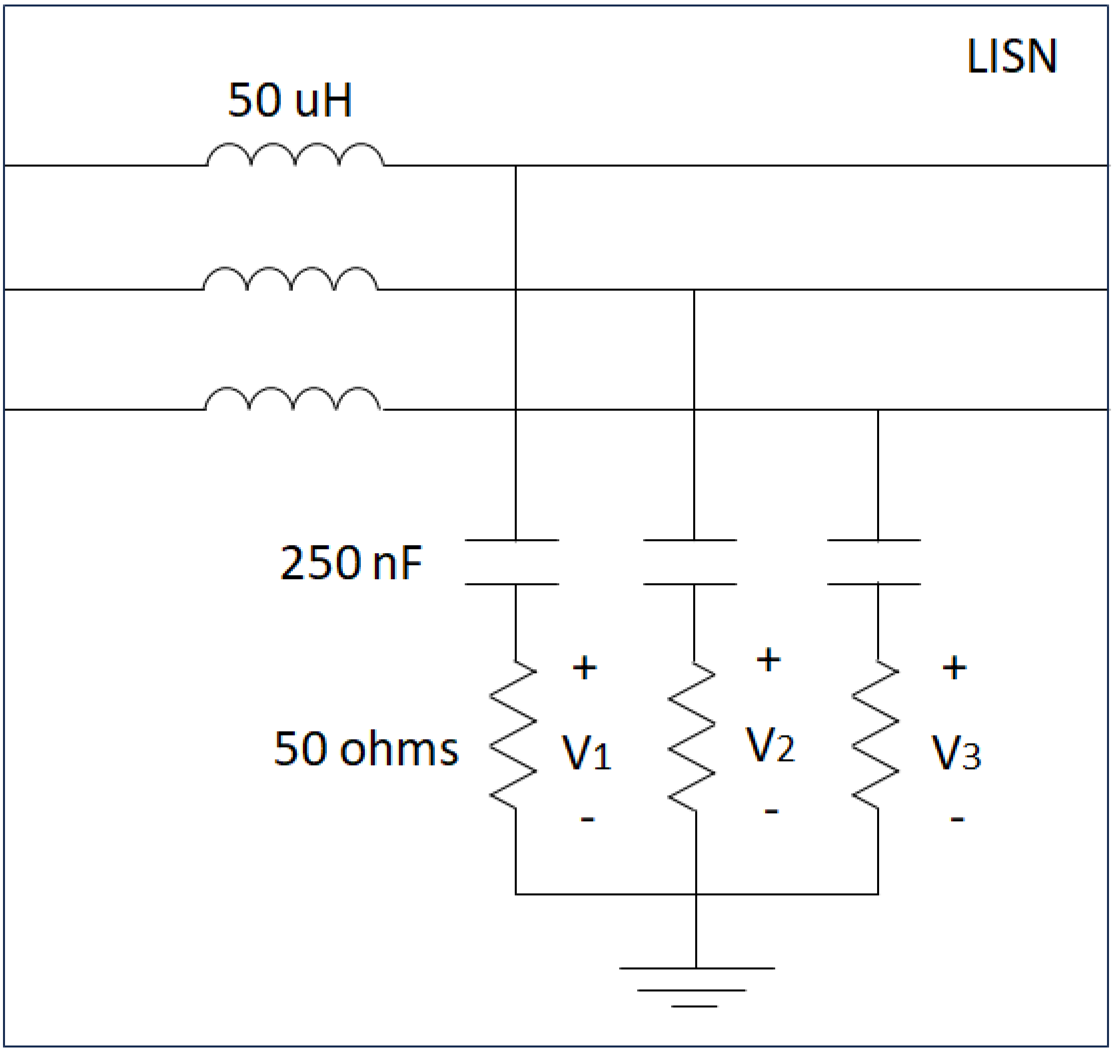
The EMI Filter window allows the user to select the desired input parameters.



The parameters of the EMI Filter are:

Ldm1	Differential Mode Inductance (H)
rLdm1	Equivalent Series Resistor of the differential mode inductance (ohms)
rCdm1	Equivalent Series Resistor of the differential mode capacitor (ohms)
Cdm1	Differential Mode Capacitor (F)
Lcm1	Three-Phase Choke or Common Mode Inductance (H)
Llk,cm1	Leakage inductance of Three-Phase Choke (H)
rCcm1	Equivalent Series Resistor of the common mode capacitor (ohms)
Ccm1	Common Mode Capacitor (F)
Cmos	Stray Capacitance between MOSFET's drain and ground (F)
Cr_gnd	Parasitic Capacitance between Positive-Negative Rail and ground (F)

The Line Impedance Stabilization Network (LISN) used for the attenuation calculation consists of a 50 uH inductance, a 250 nF capacitor and a 50 ohms resistor.



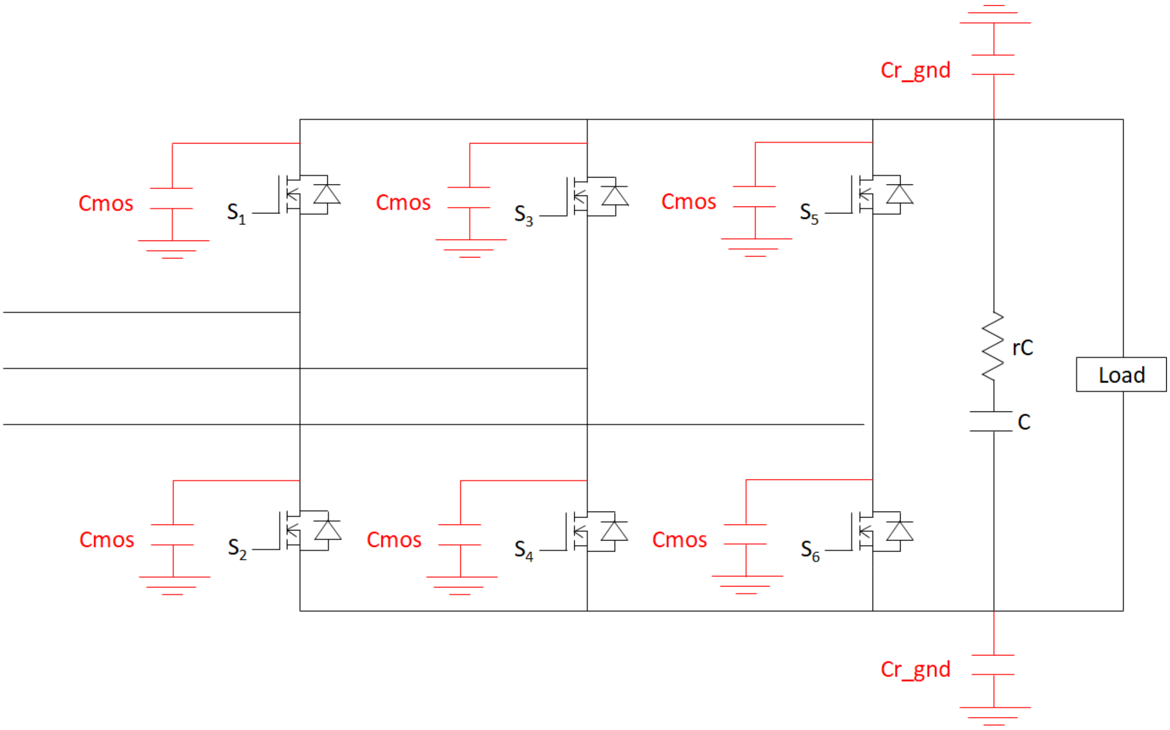
The attenuation of the common mode is considered as:

$$v_{cm} = \frac{1}{3} \cdot (V_1 + V_2 + V_3)$$

The attenuation of the differential mode is considered as:

$$v_{dm} = V_1 - v_{cm}$$

On the other hand, the following grounded parasitic capacitors are considered for the estimation of the common mode attenuation.



1.8.5.2 Structure 2

Navigation: SmartCtrl > Three-Phase PFC Boost Converter > EMI Filter >

Structure 2

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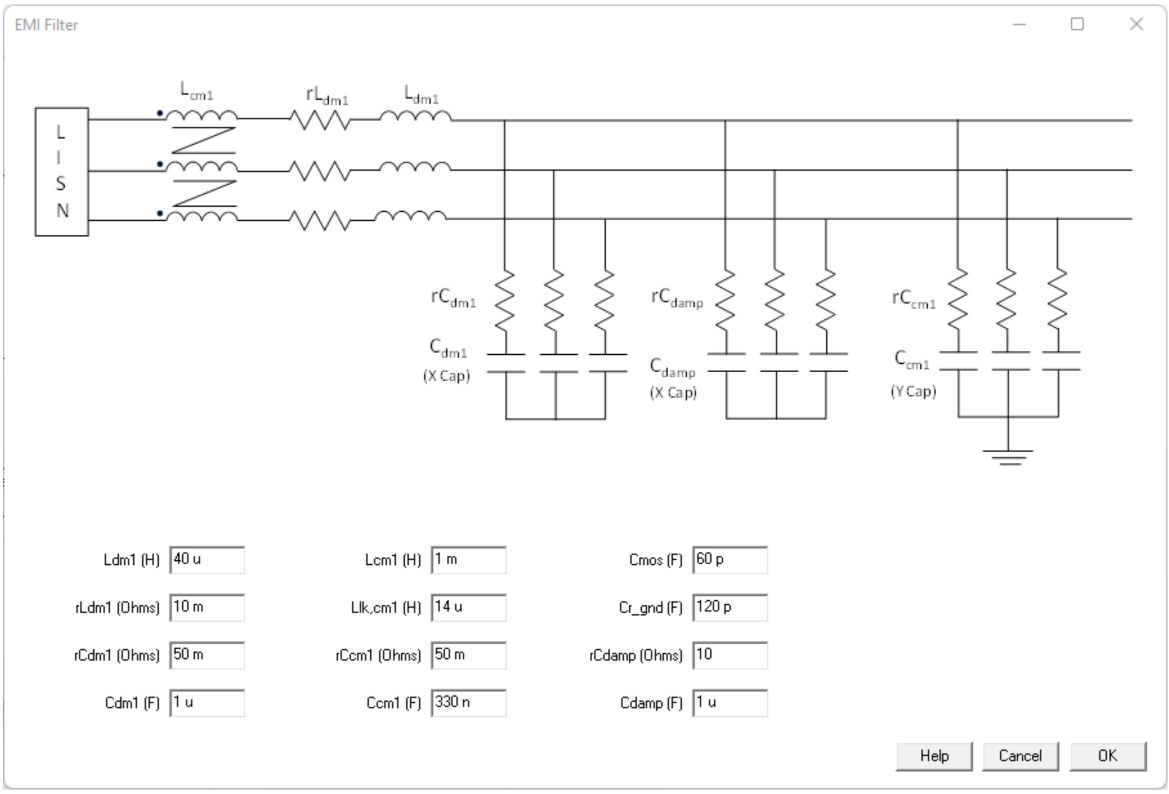
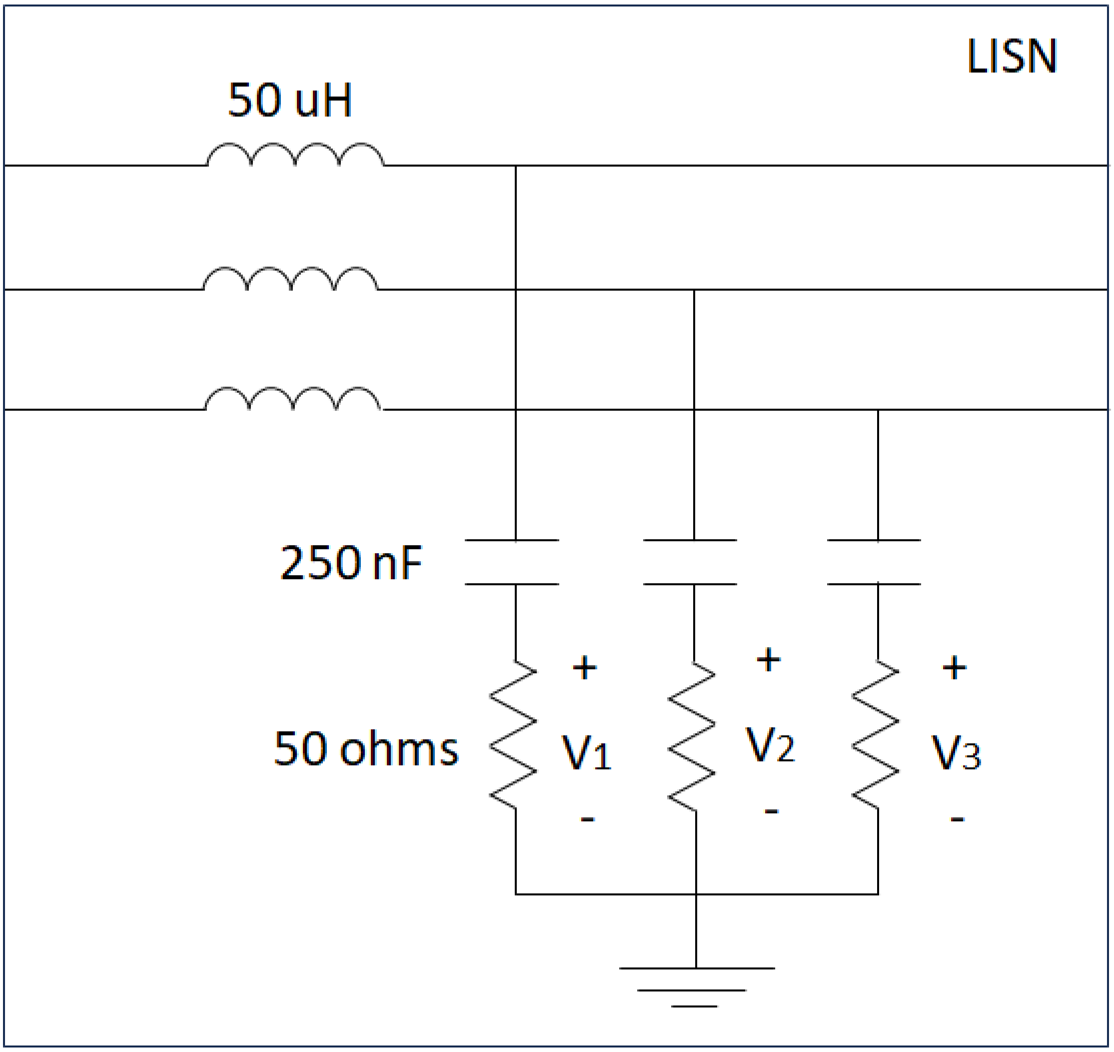
The EMI Filter window allows the user to select the desired input parameters.



The parameters of the EMI Filter are:

Ldm1	Differential Mode Inductance (H)
rLdm1	Equivalent Series Resistor of the differential mode inductance (ohms)
rCdm1	Equivalent Series Resistor of the differential mode capacitor (ohms)
Cdm1	Differential Mode Capacitor (F)
Lcm1	Three-Phase Choke or Common Mode Inductance (H)
Llk,cm1	Leakage inductance of Three-Phase Choke (H)
rCcm1	Equivalent Series Resistor of the common mode capacitor (ohms)
Ccm1	Common Mode Capacitor (F)
Cmos	Stray Capacitance between MOSFET’s drain and ground (F)
Cr_gnd	Parasitic Capacitance between Positive-Negative Rail and ground (F)
rCdamp	Damping Resistor (ohms)
Cdamp	Damping Capacitor (F)

The Line Impedance Stabilization Network (LISN) used for the attenuation calculation consists of a 50 uH inductance, a 250 nF capacitor and a 50 ohms resistor.



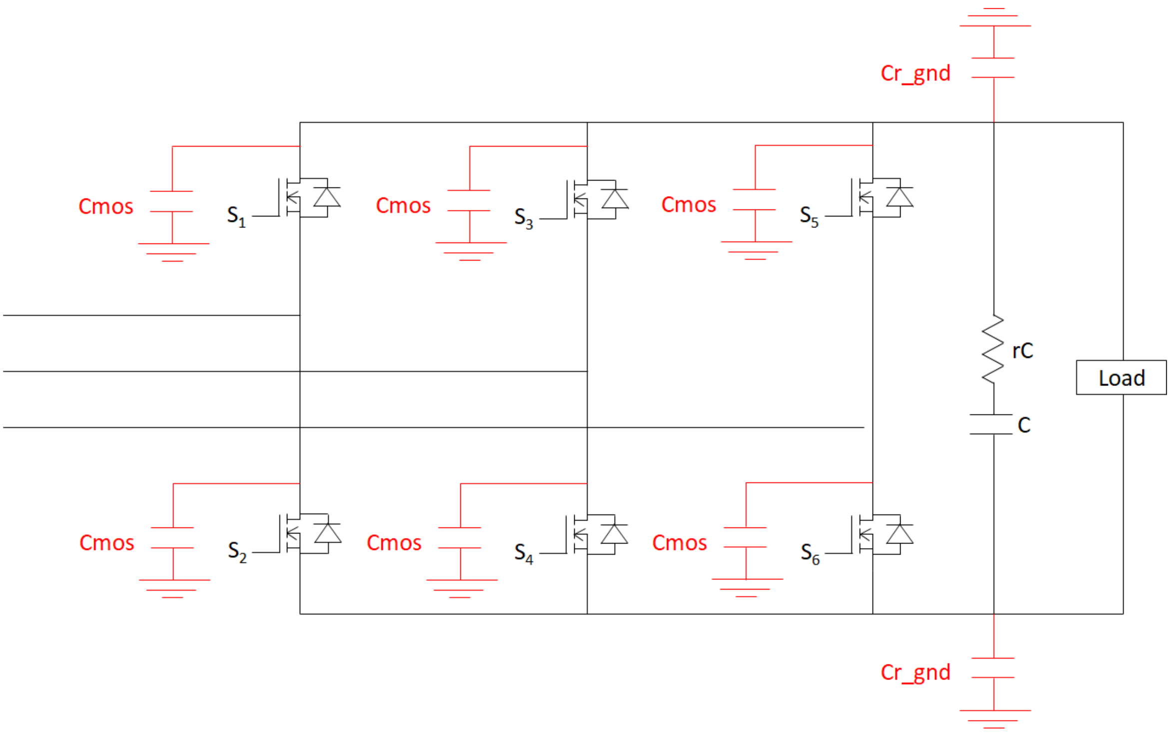
The attenuation of the common mode is considered as:

$$v_{cm} = \frac{1}{3} \cdot (V_1 + V_2 + V_3)$$

The attenuation of the differential mode is considered as:

$$v_{dm} = V_1 - v_{cm}$$

On the other hand, the following grounded parasitic capacitors are considered for the estimation of the common mode attenuation.



1.8.5.3 Structure 3

Navigation: SmartCtrl > Three-Phase PFC Boost Converter > EMI Filter >

Structure 3

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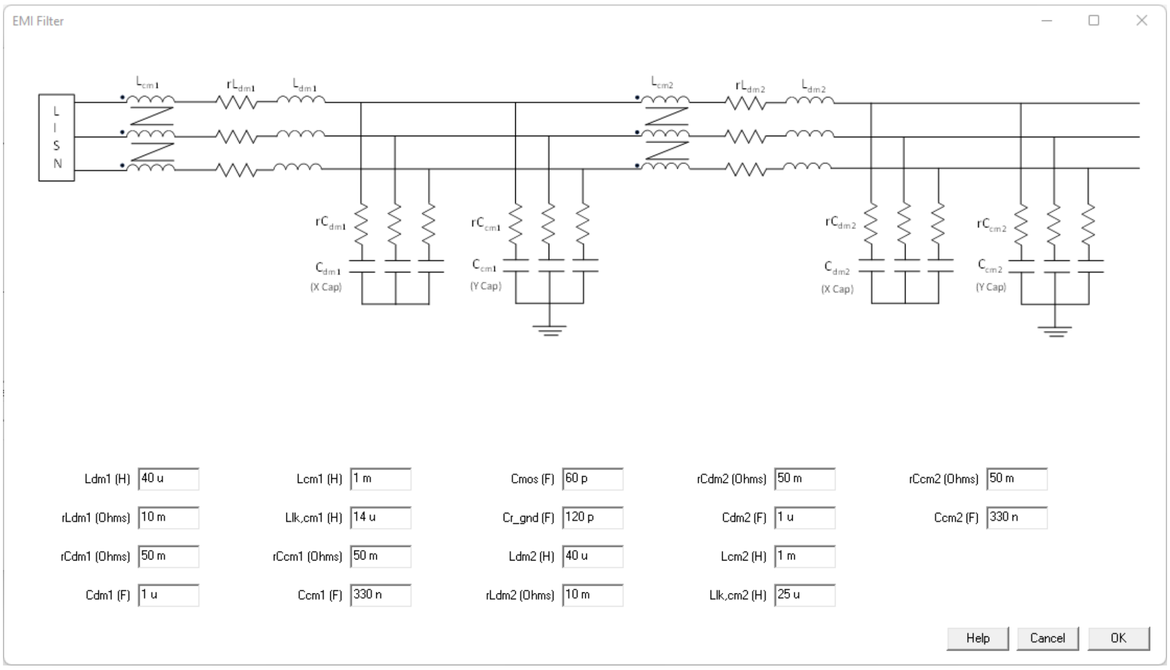
The EMI Filter window allows the user to select the desired input parameters.



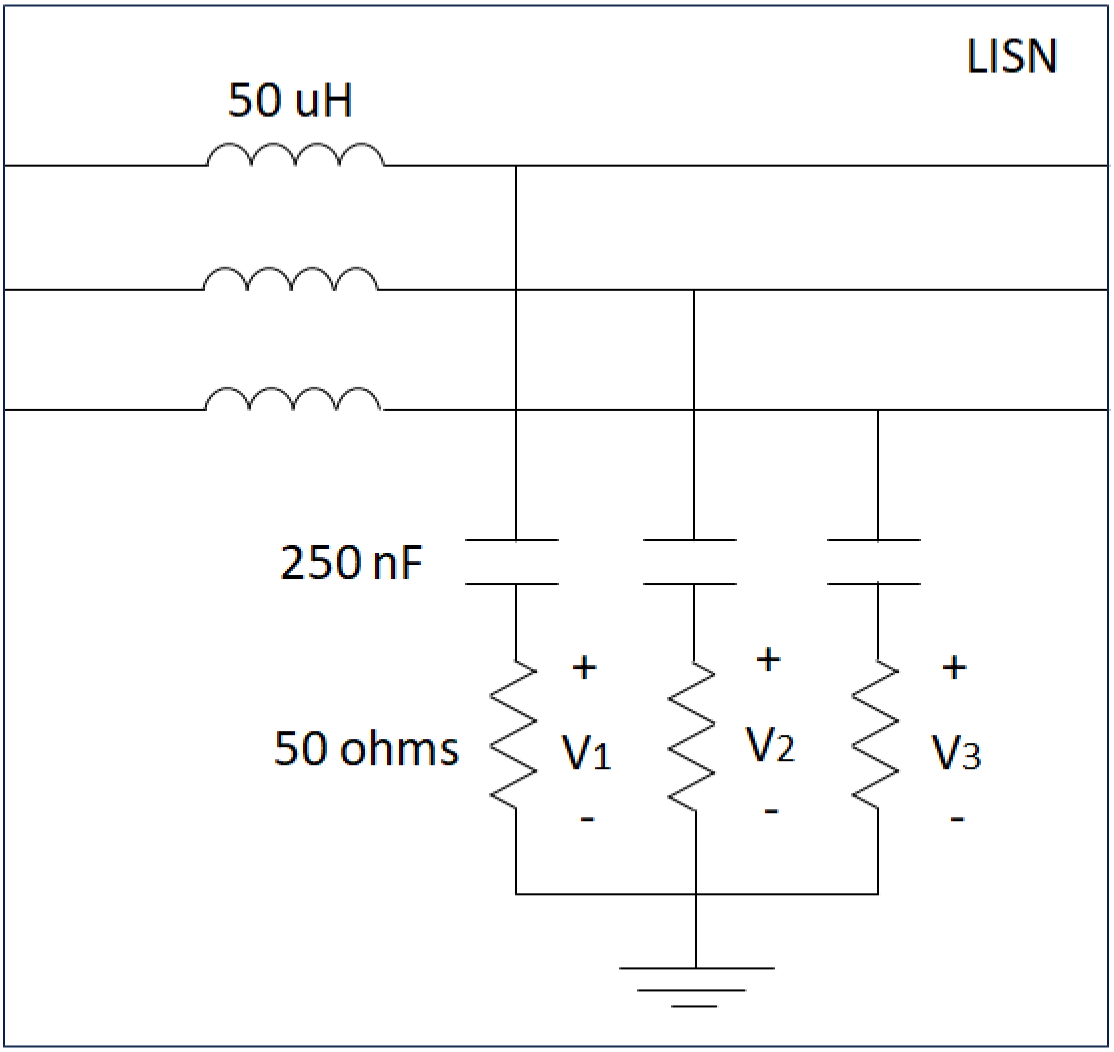
The parameters of the EMI Filter are:

Ldm1	Differential Mode Inductance of the 2nd stage (H)
rLdm1	Equivalent Series Resistor of the differential mode inductance of the 2nd stage (ohms)
rCdm1	Equivalent Series Resistor of the differential mode capacitor of the 2nd stage (ohms)
Cdm1	Differential Mode Capacitor of the 2nd stage (F)
Lcm1	Three-Phase Choke or Common Mode Inductance of the 2nd stage (H)
Llk,cm1	Leakage inductance of Three-Phase Choke of the 2nd stage (H)
rCcm1	Equivalent Series Resistor of the common mode capacitor of the 2nd stage (ohms)
Ccm1	Common Mode Capacitor of the 2nd stage (F)
Ldm2	Differential Mode Inductance of the 1st stage (H)
rLdm2	Equivalent Series Resistor of the differential mode inductance of the 1st stage (ohms)
rCdm2	Equivalent Series Resistor of the differential mode capacitor of the 1st stage (ohms)
Cdm2	Differential Mode Capacitor of the 1st stage (F)
Lcm2	Three-Phase Choke or Common Mode Inductance of the 1st stage (H)
Llk,cm2	Leakage inductance of Three-Phase Choke of the 1st stage (H)
rCcm2	Equivalent Series Resistor of the common mode capacitor of the 1st stage (ohms)
Ccm2	Common Mode Capacitor of the 1st stage (F)

Cmos Stray Capacitance between MOSFET's drain and ground (F)

Cr_gnd Parasitic Capacitance between Positive-Negative Rail and ground (F)

The Line Impedance Stabilization Network (LISN) used for the attenuation calculation consists of a 50 uH inductance, a 250 nF capacitor and a 50 ohms resistor.



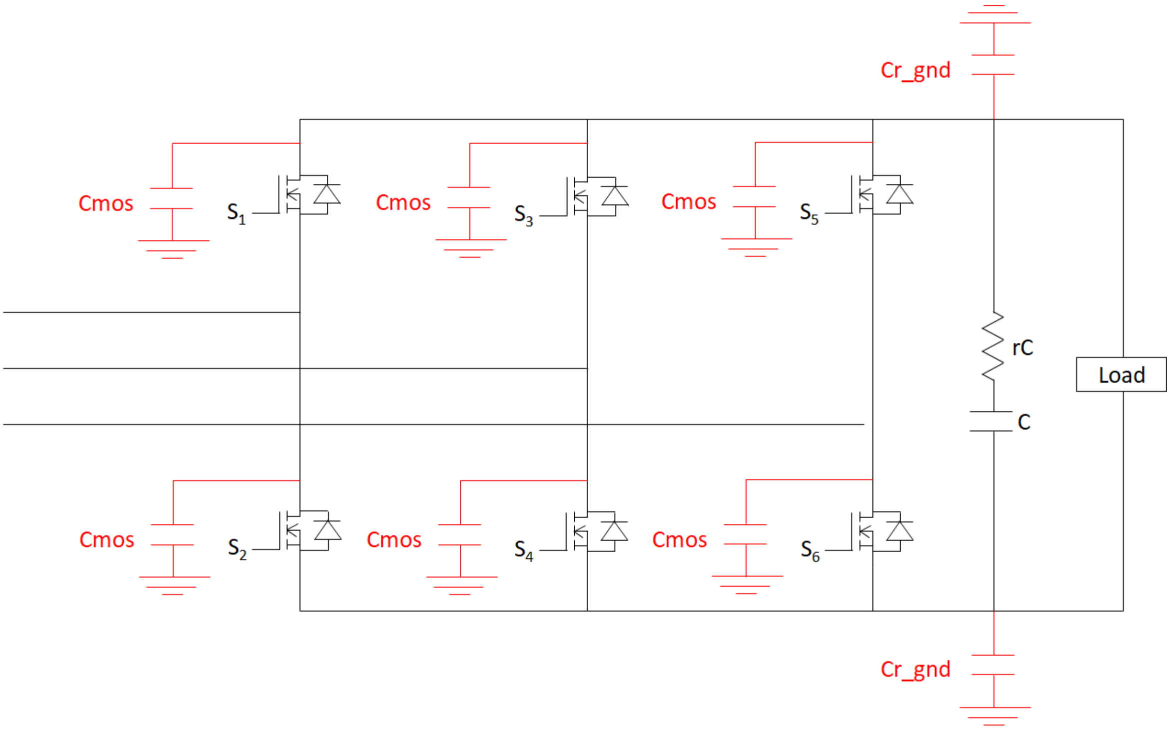
The attenuation of the common mode is considered as:

$$v_{cm} = \frac{1}{3} \cdot (V_1 + V_2 + V_3)$$

The attenuation of the differential mode is considered as:

$$v_{dm} = V_1 - v_{cm}$$

On the other hand, the following grounded parasitic capacitors are considered for the estimation of the common mode attenuation.



1.8.5.4 Structure 4

Navigation: SmartCtrl > Three-Phase PFC Boost Converter > EMI Filter >

Structure 4

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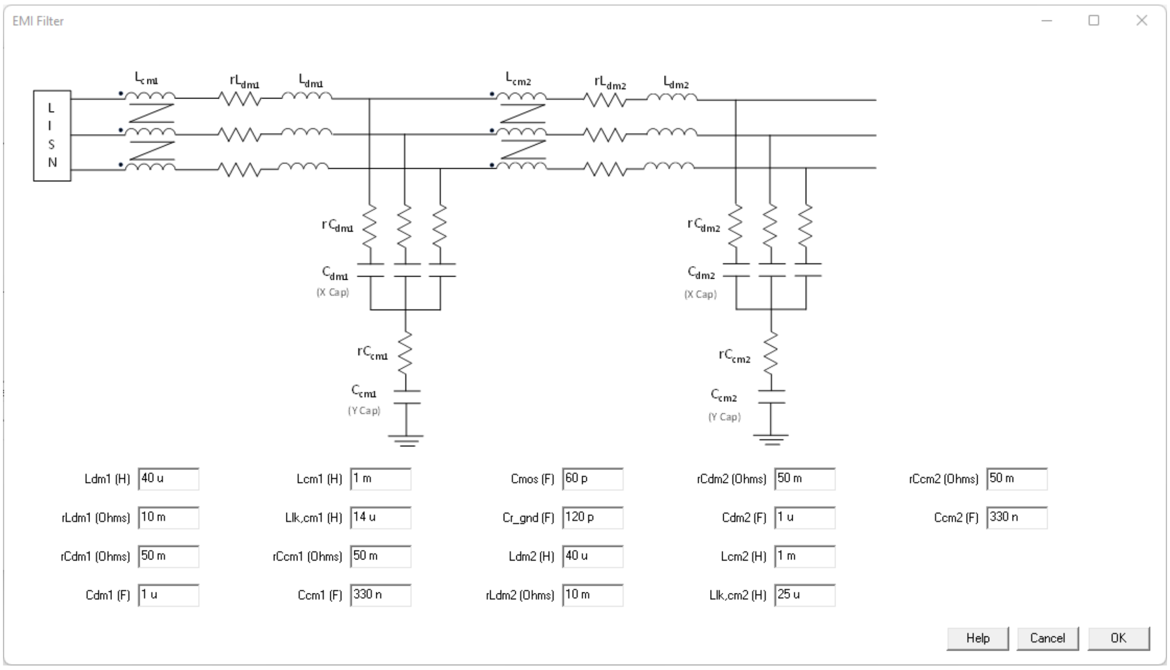
The EMI Filter window allows the user to select the desired input parameters.



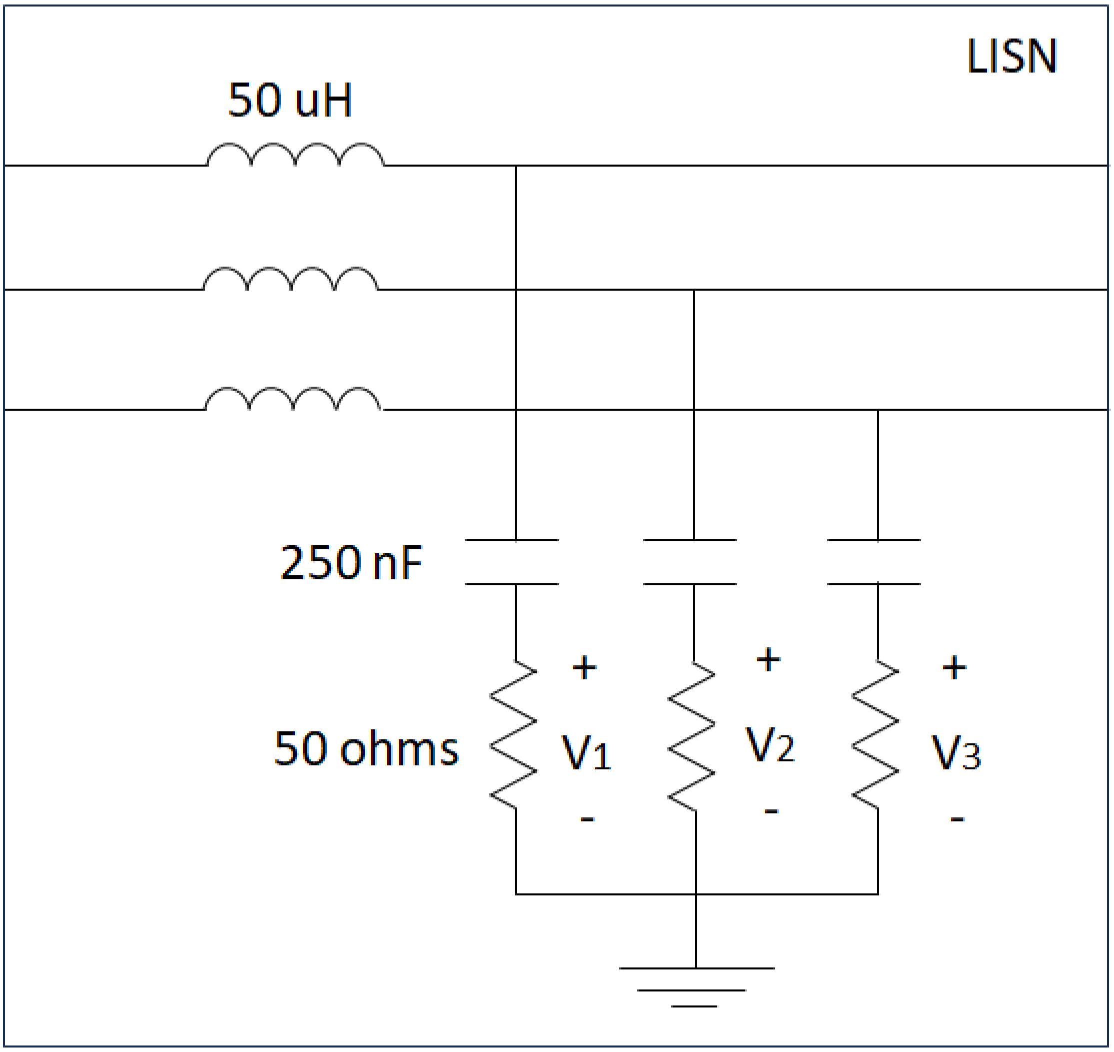
The parameters of the EMI Filter are:

Ldm1	Differential Mode Inductance of the 2nd stage (H)
rLdm1	Equivalent Series Resistor of the differential mode inductance of the 2nd stage (ohms)
rCdm1	Equivalent Series Resistor of the differential mode capacitor of the 2nd stage (ohms)
Cdm1	Differential Mode Capacitor of the 2nd stage (F)
Lcm1	Three-Phase Choke or Common Mode Inductance of the 2nd stage (H)
Llk,cm1	Leakage inductance of Three-Phase Choke of the 2nd stage (H)
rCcm1	Equivalent Series Resistor of the common mode capacitor of the 2nd stage (ohms)
Ccm1	Common Mode Capacitor of the 2nd stage (F)
Ldm2	Differential Mode Inductance of the 1st stage (H)
rLdm2	Equivalent Series Resistor of the differential mode inductance of the 1st stage (ohms)
rCdm2	Equivalent Series Resistor of the differential mode capacitor of the 1st stage (ohms)
Cdm2	Differential Mode Capacitor of the 1st stage (F)
Lcm2	Three-Phase Choke or Common Mode Inductance of the 1st stage (H)
Llk,cm2	Leakage inductance of Three-Phase Choke of the 1st stage (H)
rCcm2	Equivalent Series Resistor of the common mode capacitor of the 1st stage (ohms)
Ccm2	Common Mode Capacitor of the 1st stage (F)

Cmos Stray Capacitance between MOSFET's drain and ground (F)

Cr_gnd Parasitic Capacitance between Positive-Negative Rail and ground (F)

The Line Impedance Stabilization Network (LISN) used for the attenuation calculation consists of a 50 uH inductance, a 250 nF capacitor and a 50 ohms resistor.



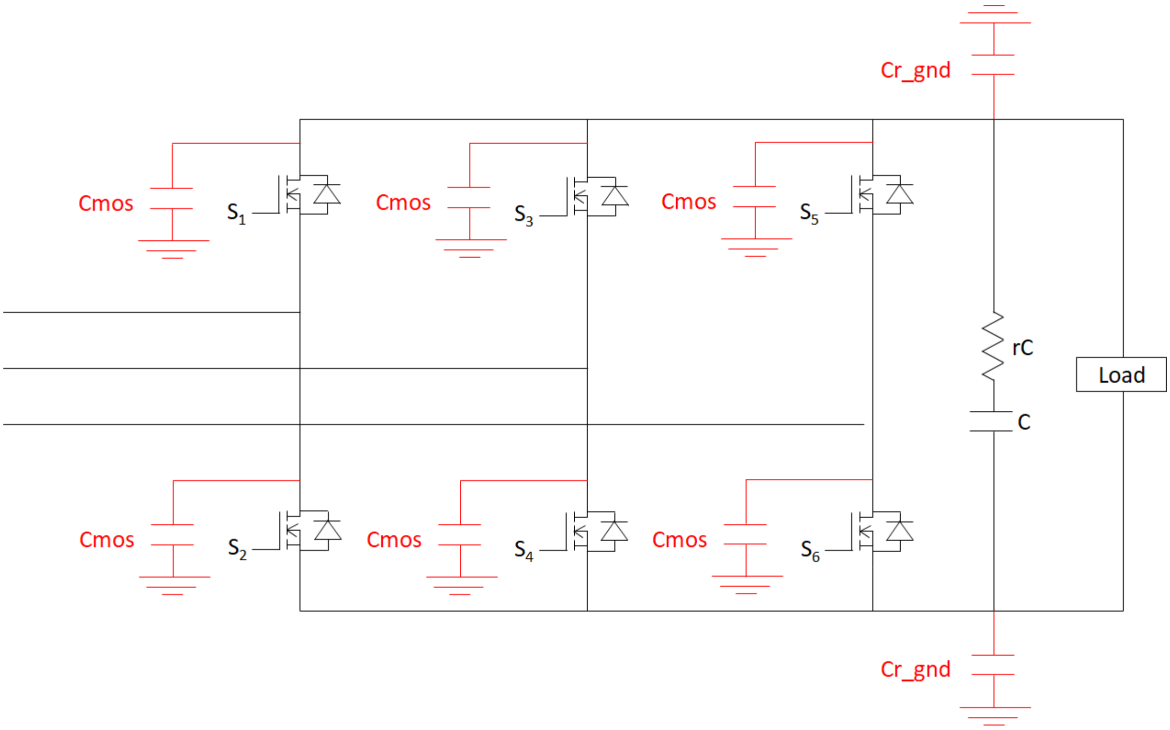
The attenuation of the common mode is considered as:

$$v_{cm} = \frac{1}{3} \cdot (V_1 + V_2 + V_3)$$

The attenuation of the differential mode is considered as:

$$v_{dm} = V_1 - v_{cm}$$

On the other hand, the following grounded parasitic capacitors are considered for the estimation of the common mode attenuation.



1.8.6 Phase-Locked Loop

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Phase-Locked Loop

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1.8.6.1 SRFPLL

Navigation: SmartCtrl > Three-Phase PFC Boost Converter > Phase-Locked Loop >

SRFPLL

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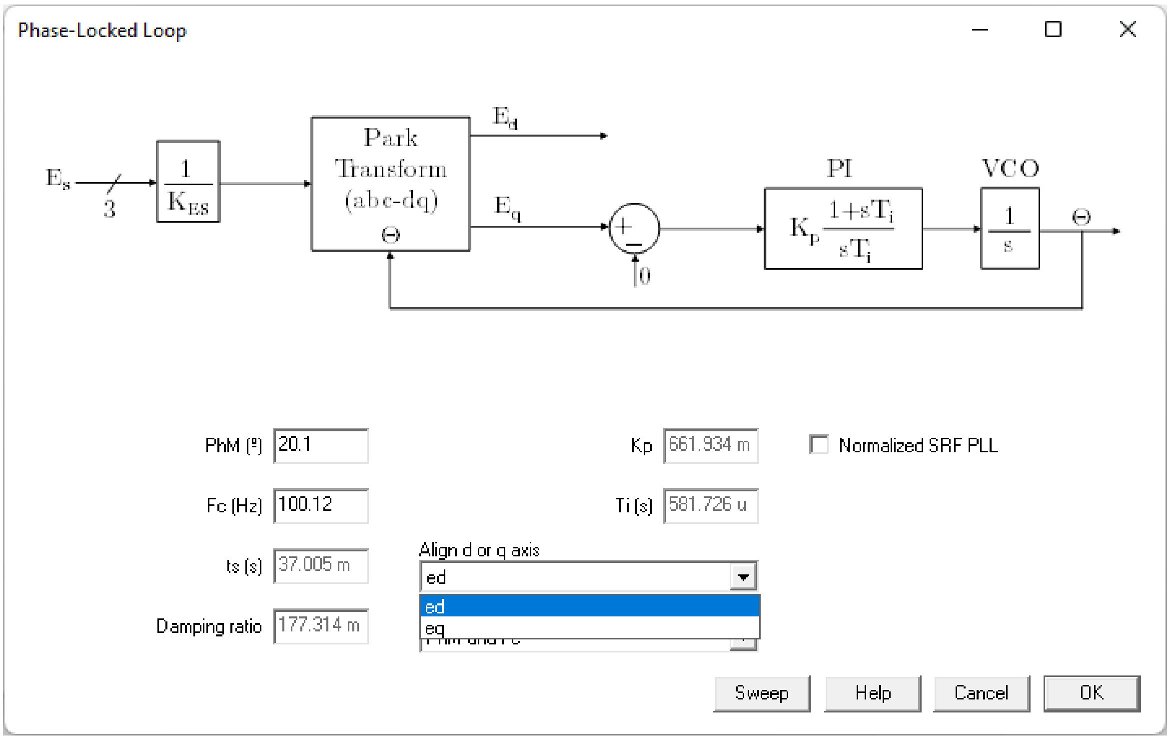
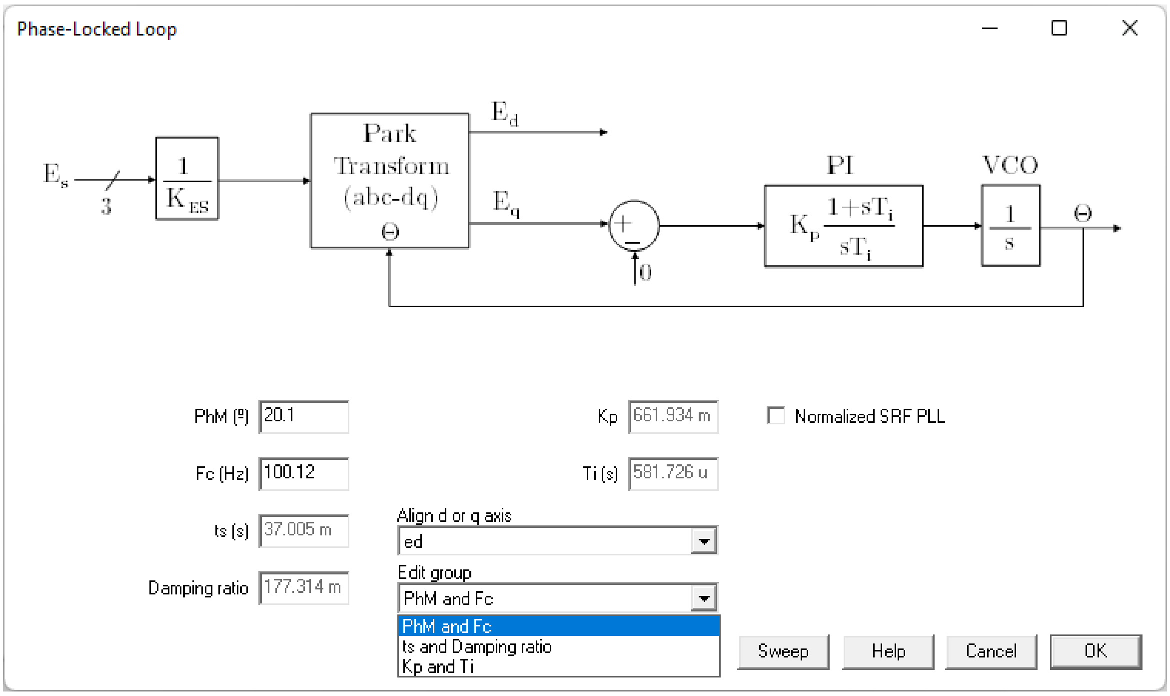
In the PLL window the user can choose the axis alignment. The transformation from abc to dq is defined as invariant in amplitude.

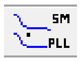
- The alignment with the d-axis means that the active power is controlled with the d-axis and the reactive power is controlled with the q-axis.
- The alignment with the q-axis means that the active power is controlled with the q-axis and the reactive power is controlled with the d-axis.



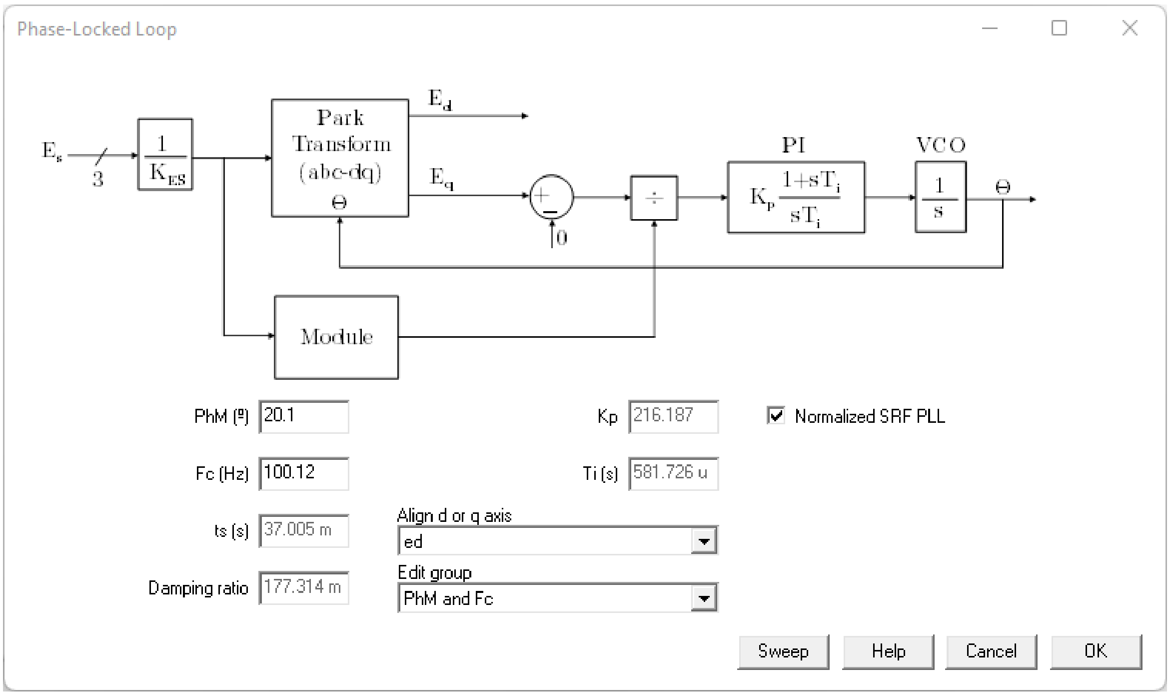
The PLL control loop can be manually designed in several ways:

- **PhM and Fc:** A crossover frequency in Hz (Fc) and phase margin in degrees (PhM).
- **ts and Damping Ratio:** Allows to set a stabilization time in seconds and damping constant.
- **Kp and Ti:** Allows to set the proportional constant and time constant of the PI compensator.



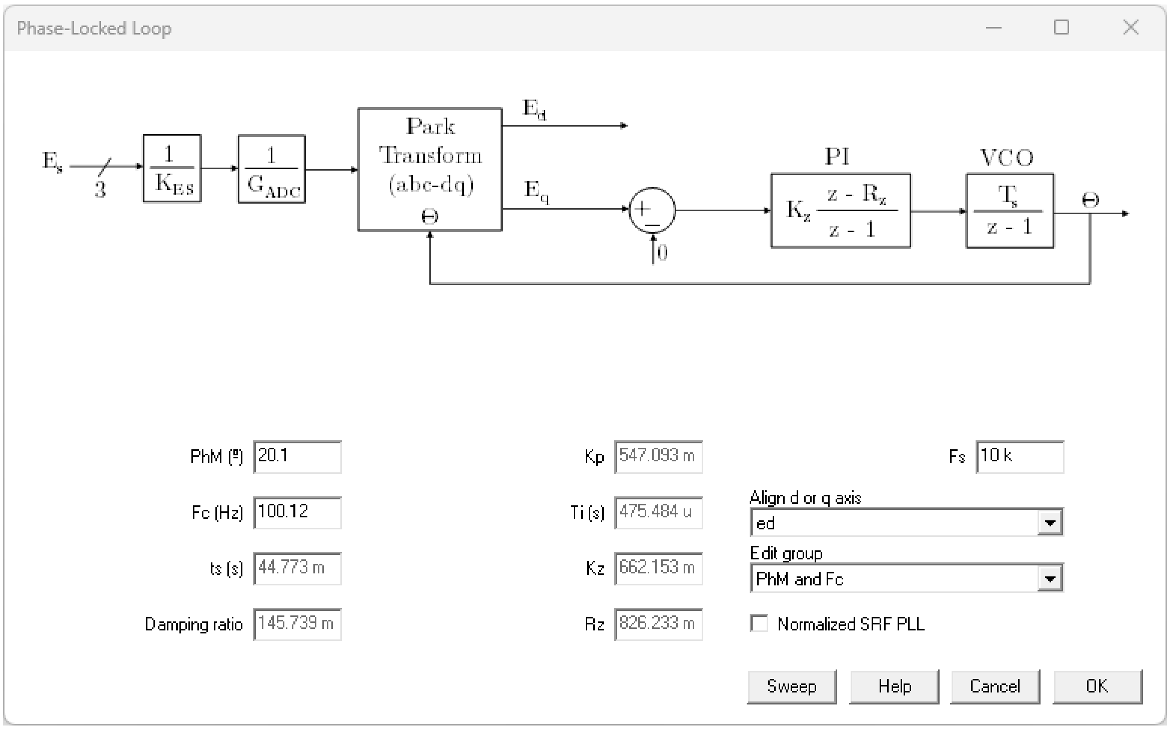
The user can also design the control loop with the solutions map  option that is located in the menu bar. In this case parameters (Fc, PhM, ts, damping ratio, Kp and Ti) will be calculated automatically.

The "Normalized" option allows to consider a PLL with or without unity gain.



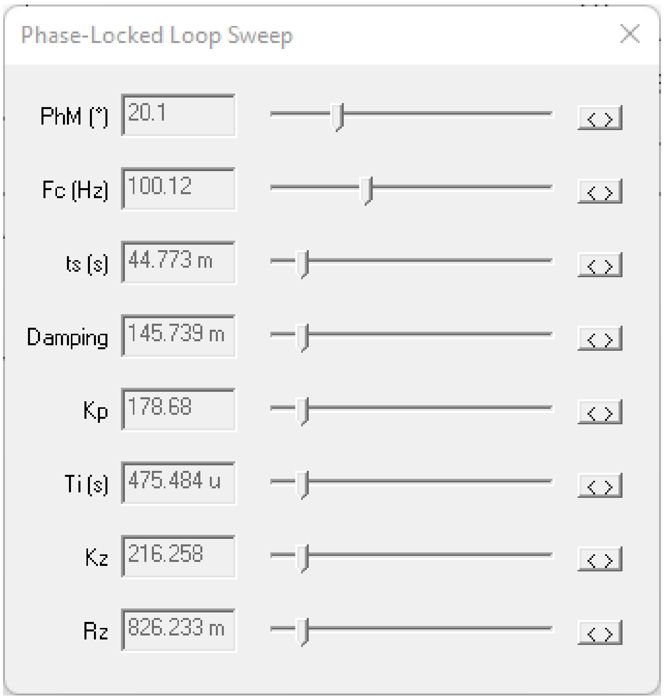
When the PLL is discrete, the sampling frequency (Fs) in Hz must be defined. To consider a discrete PLL, the digital checkbox in the Single-Line Diagram window must be checked.

- Kz: Gain of the transfer function of the PI compensator in z-domain.
- Rz: Zero of the transfer function of the PI compensator in z-domain.



In the discrete PLL, the values of the constants Kp and Ti are estimated using the Backward Euler discretization method.

The Sweep button allows the user to change the input parameters with sliders.



1.8.6.2 QSG-SRFPLL

Navigation: SmartCtrl > Three-Phase PFC Boost Converter > Phase-Locked Loop >

QSG-SRFPLL

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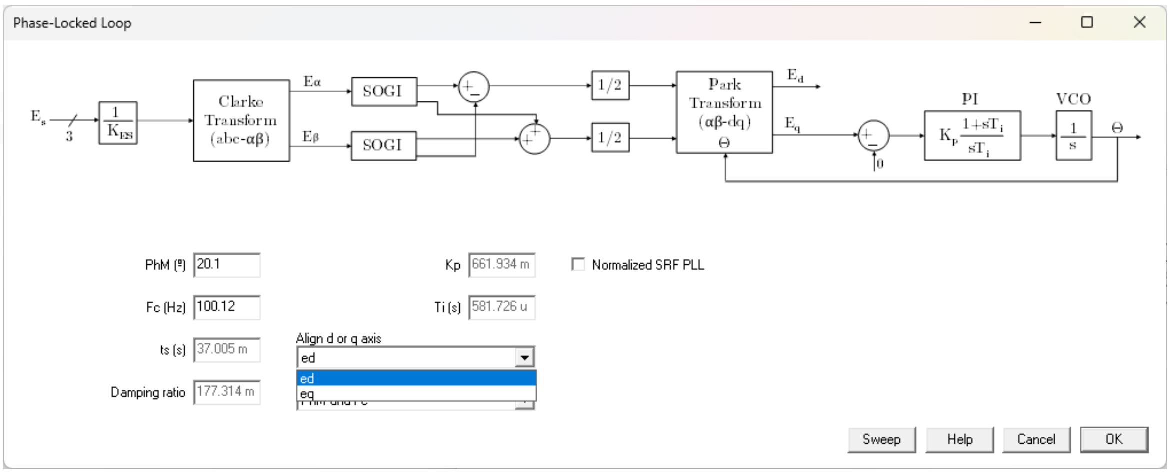
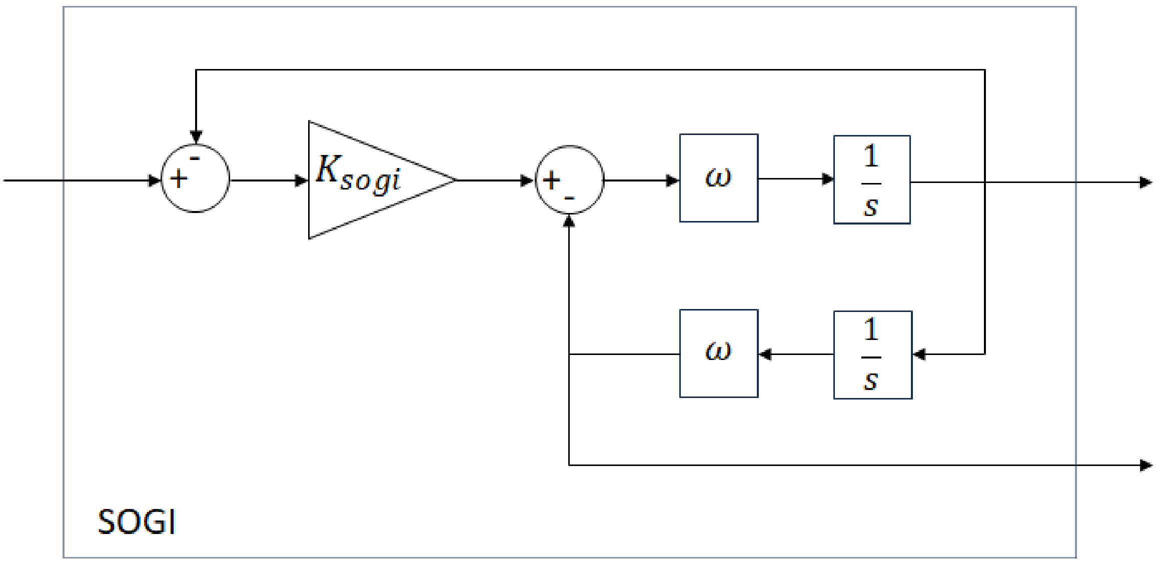
In the PLL window the user can choose the axis alignment. The transformation from abc to dq is defined as invariant in amplitude.

- The alignment with the d-axis means that the active power is controlled with the d-axis and the reactive power is controlled with the q-axis.
- The alignment with the q-axis means that the active power is controlled with the q-axis and the reactive power is controlled with the d-axis.

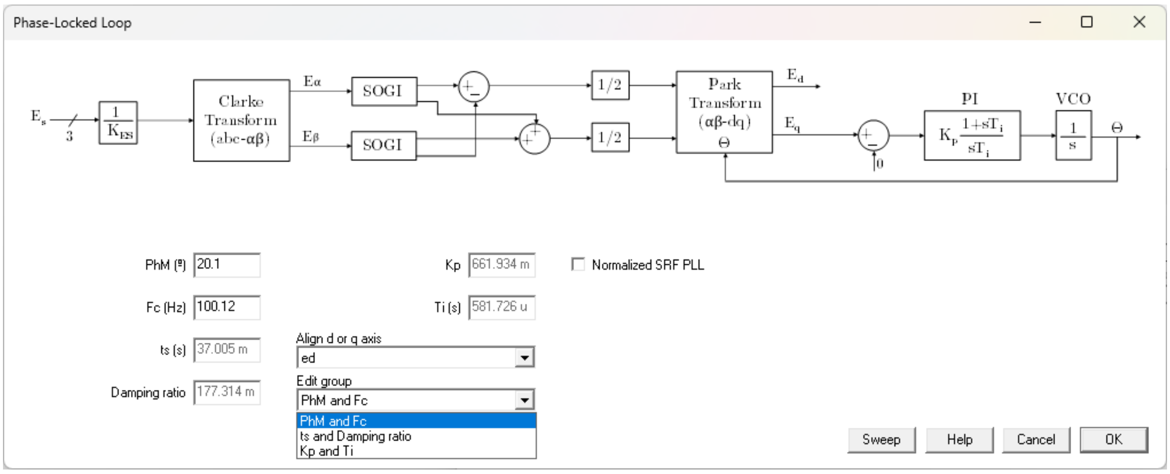


The SOGI means "Second Order Generalized Integrator". The SOGI block diagram is shown in the following figure. The parameter ω represents the line frequency.



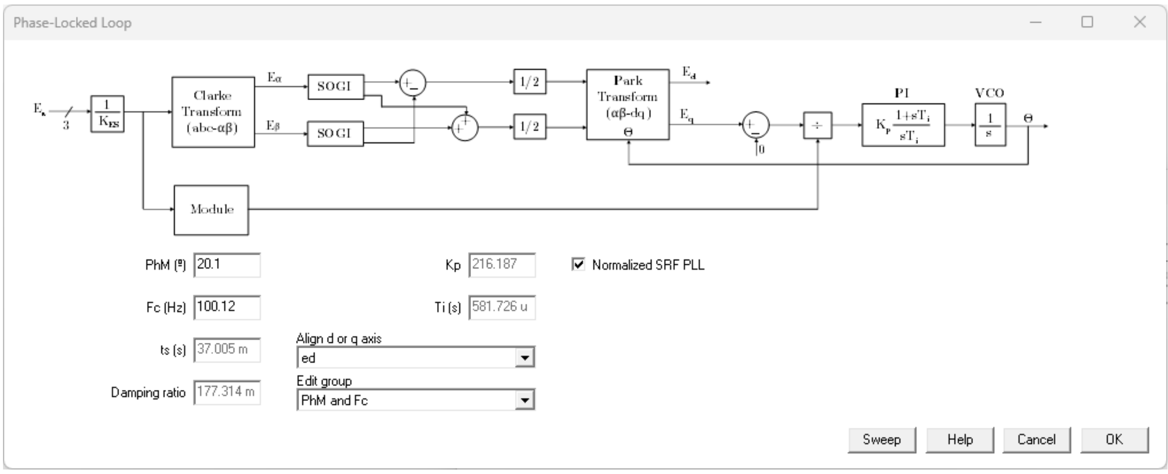
The PLL control loop can be manually designed in several ways:

- **PhM and Fc:** A crossover frequency in Hertz (Fc) and phase margin in degrees (PhM).
- **ts and Damping Ratio:** Allows to set a stabilization time in seconds and damping constant.
- **Kp and Ti:** Allows to set the proportional constant and time constant of the PI compensator.



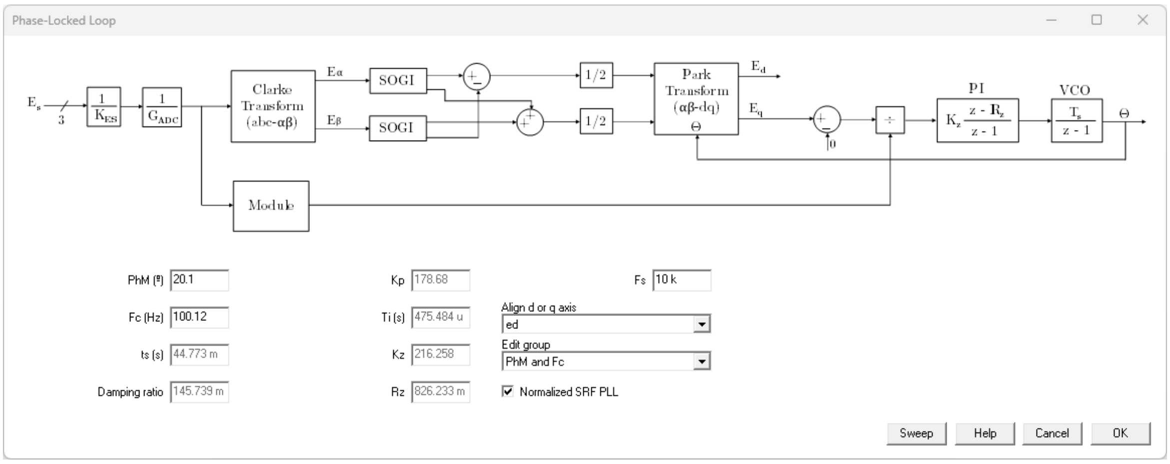
The user can also design the control loop with the solutions map  option that is located in the menu bar. In this case parameters (Fc, PhM, ts, damping ratio, Kp and Ti) will be calculated automatically.

The "Normalized" option allows to consider a PLL with or without unity gain.



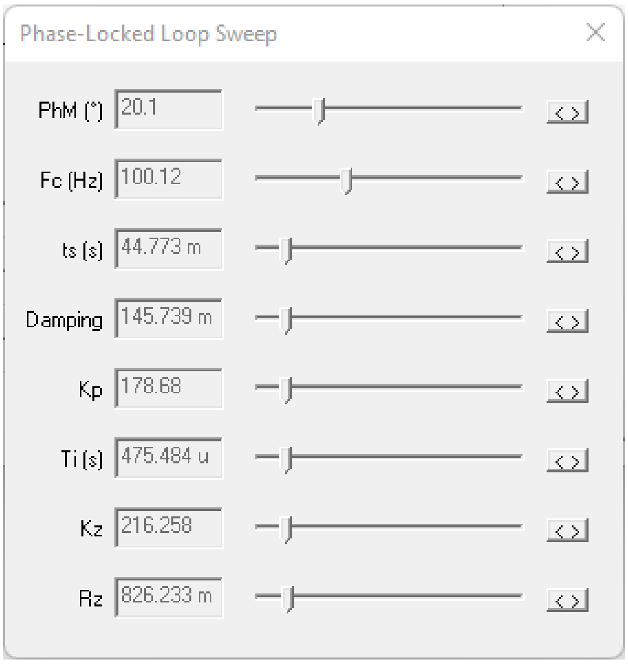
When the PLL is discrete, the sampling frequency (Fs) in Hz must be defined. To consider a discrete PLL, the digital checkbox in the Single-Line Diagram window must be checked.

- Kz: Gain of the transfer function of the PI compensator in z-domain.
- Rz: Zero of the transfer function of the PI compensator in z-domain.



In the discrete PLL, the values of the constants Kp and Ti are estimated using the Backward Euler discretization method.

The Sweep button allows the user to change the input parameters with sliders.



1.8.7 Inductor current sensor

Navigation: SmartCtrl > Three-Phase PFC Boost Converter >

Inductor current sensor

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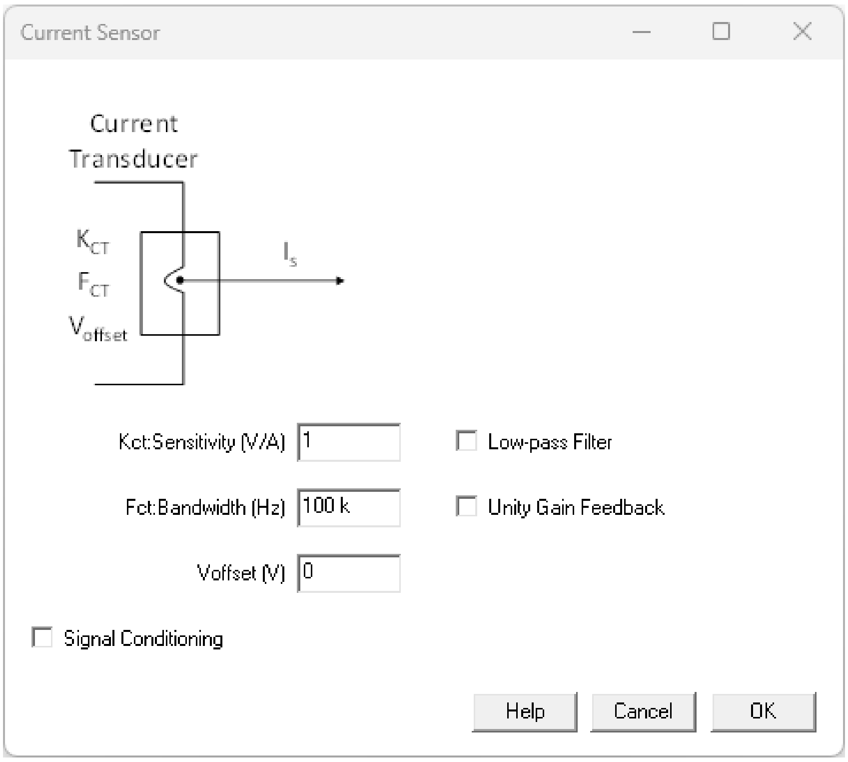
In the current sensor window, the user can define the gain and bandwidth of the current transducer.

- **Kct:** Sensitivity of the current Transducer (V/A)

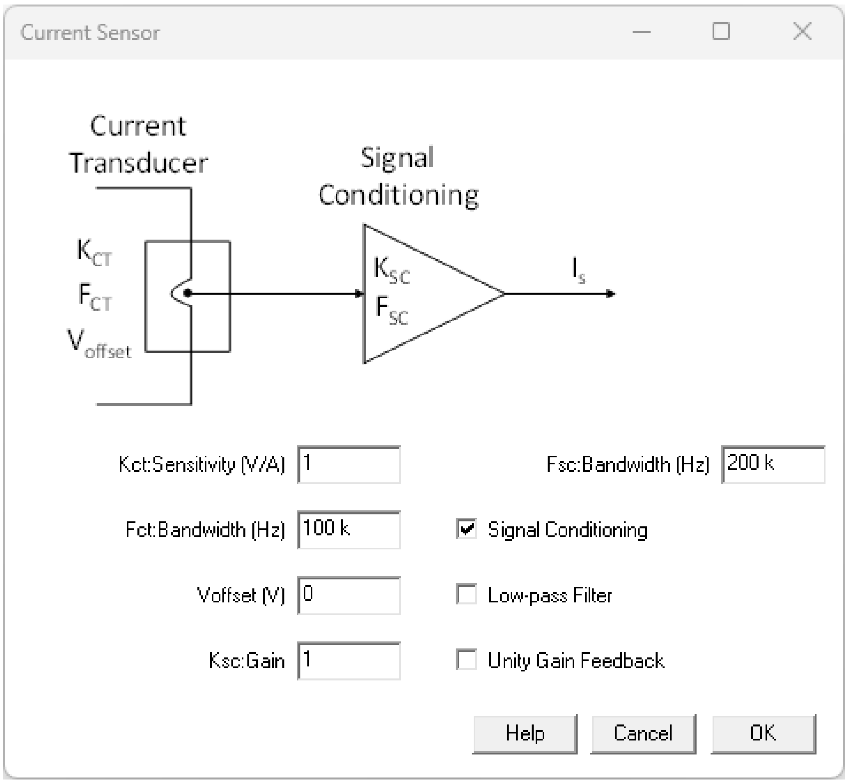
- **Fct:** Bandwidth of the current Transducer (Hz)
- **Voffset:** Offset Voltage of the current Transducer (V)



If the Signal Conditioning option is checked then the user can define:

- **Ksc:** Gain of the signal conditioning stage
- **Fsc:** Bandwidth of the signal conditioning stage (Hz)

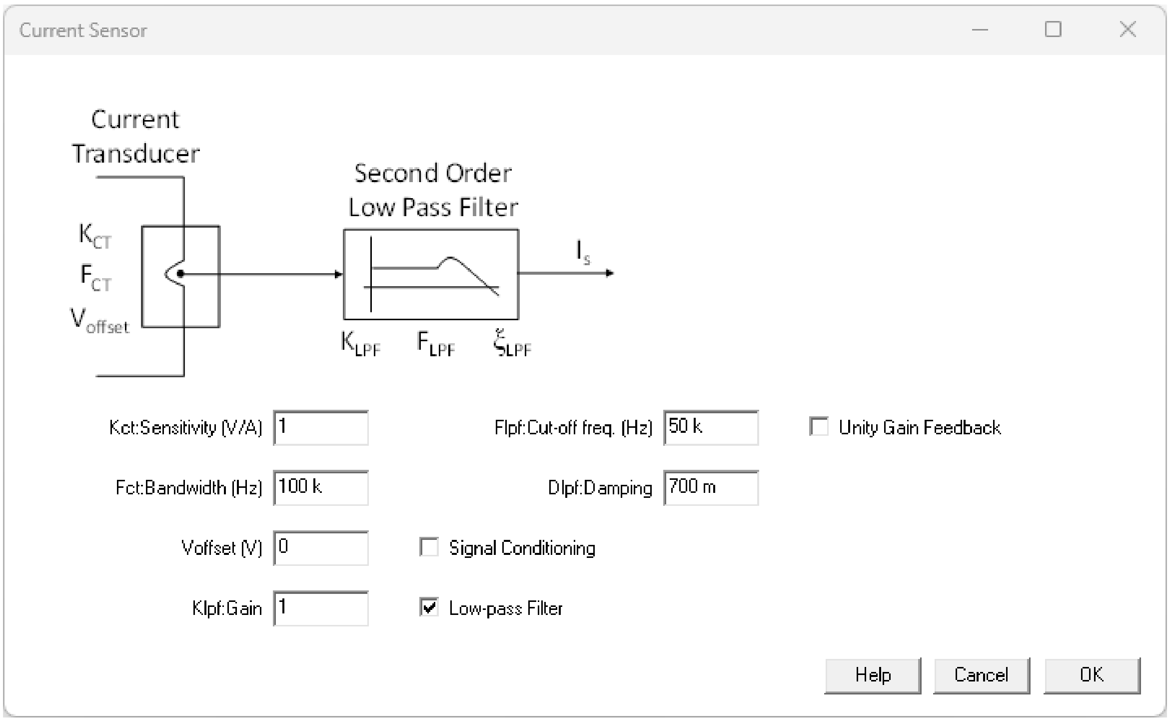
The transfer function contemplated in the signal conditioning stage is a first order low-pass filter.



If the Low-Pass Filter option is checked then the user can define:

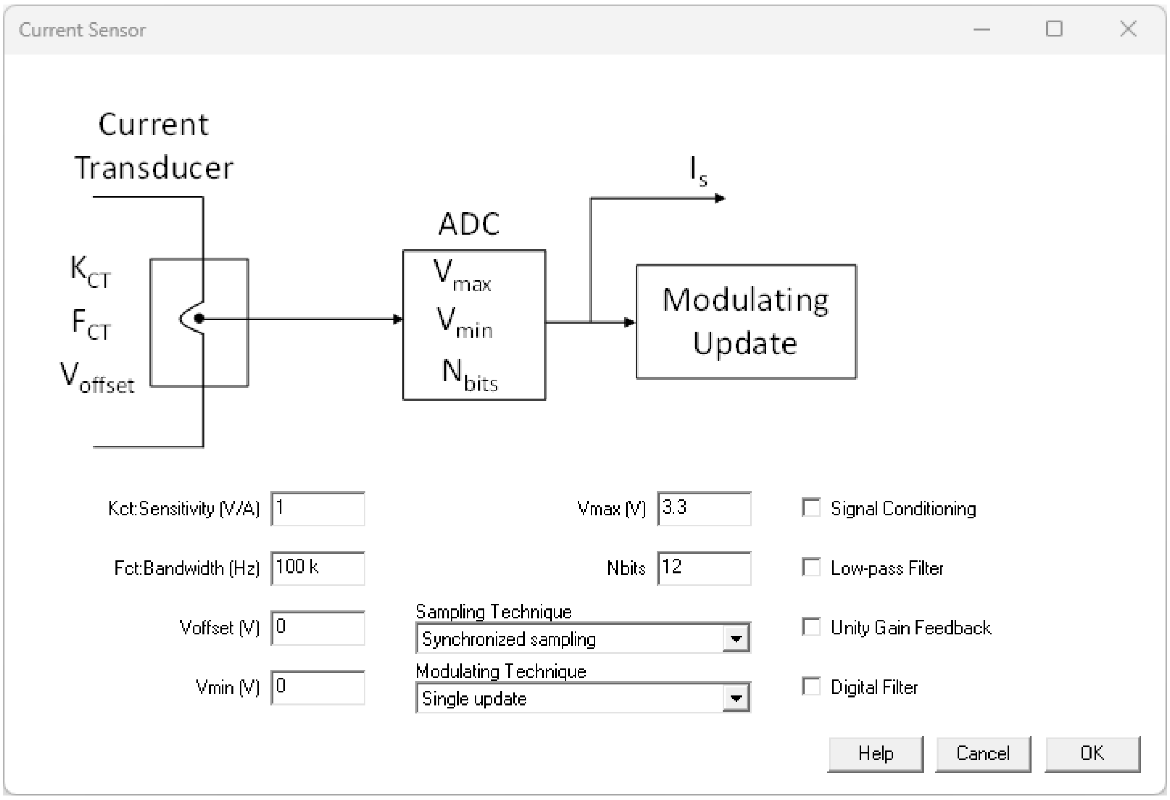
- **Klpf:** Gain of the Low-Pass Filter stage
- **Flpf:** Cutoff frequency of the Low-Pass Filter (Hz)
- **Dlpf:** Damping ratio of the Low-Pass Filter

The transfer function contemplated in the Low-Pass Filter stage is a second order low-pass filter. This stage represents an anti-aliasing filter.

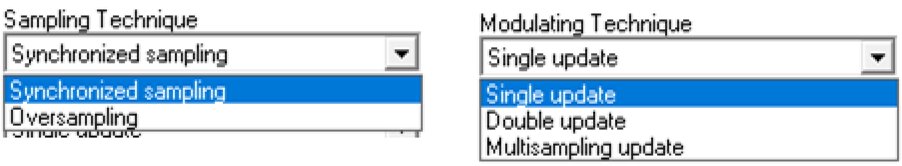


If the Digital option is checked in the Single-Line Diagram window, then the user can define:

- **Vmax:** Maximum voltage of the ADC can read, used to calculate its gain.
- **Vmin:** Minimum voltage of the ADC can read, used to calculate its gain.
- **Nbits:** Number of bits of the ADC to represent the analog input value. This number affects the calculation of the reference.

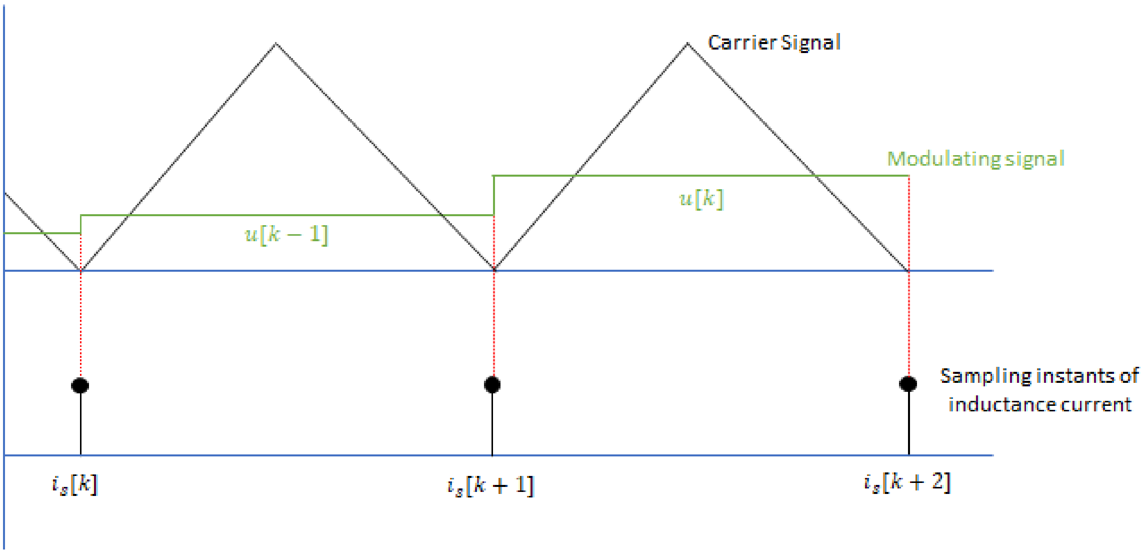


The drop-down list called “Sampling Technique” and “Modulating Technique” allows the user to define the sampling frequency.

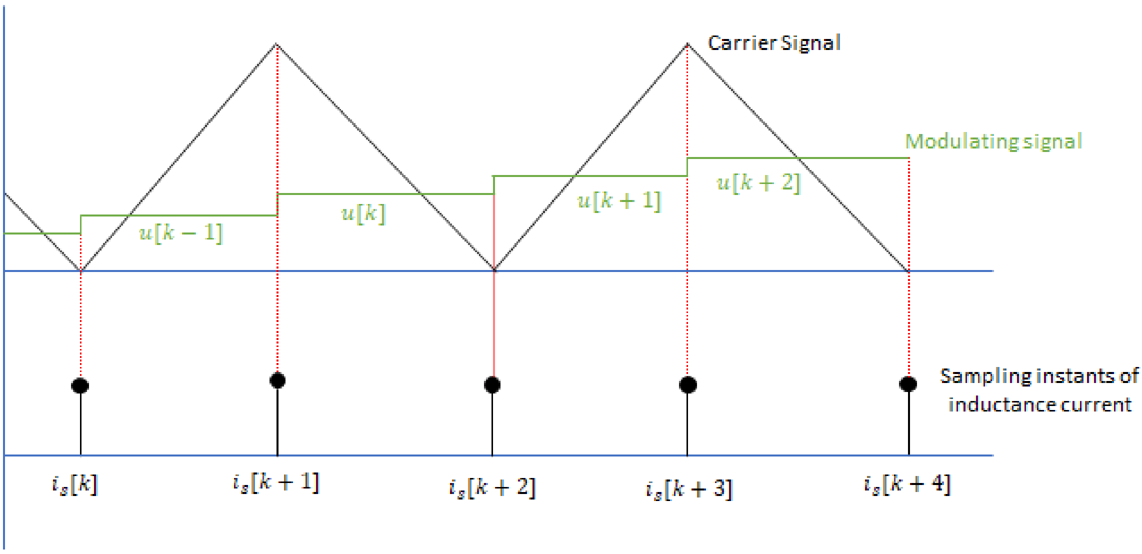


The sampling strategy is shown in the following figures.

“Synchronized sampling” and “Single update”



"Synchronized sampling" and "Double update"

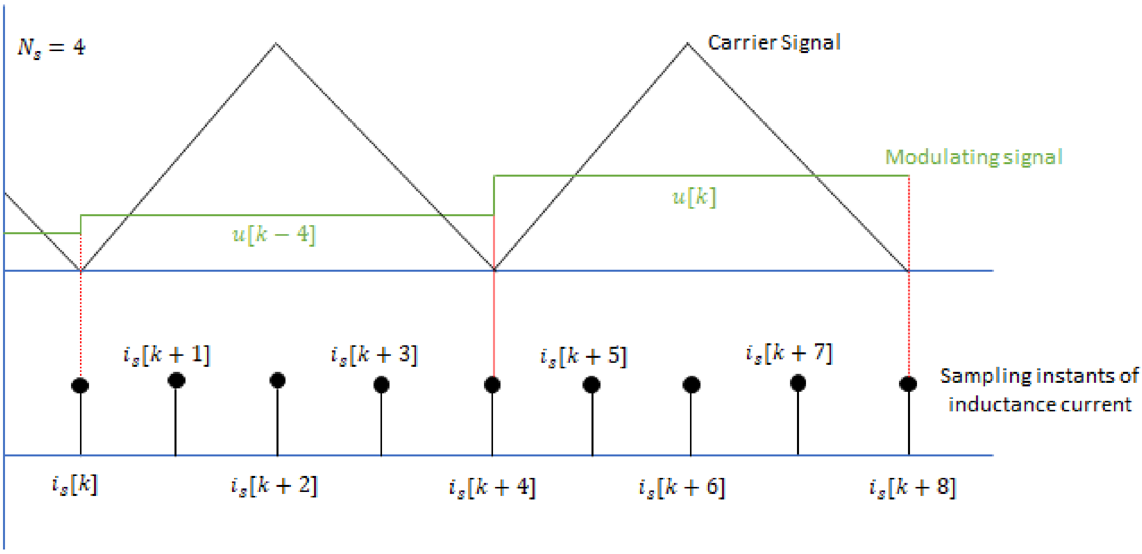


For oversampling cases, the following parameter must be defined:

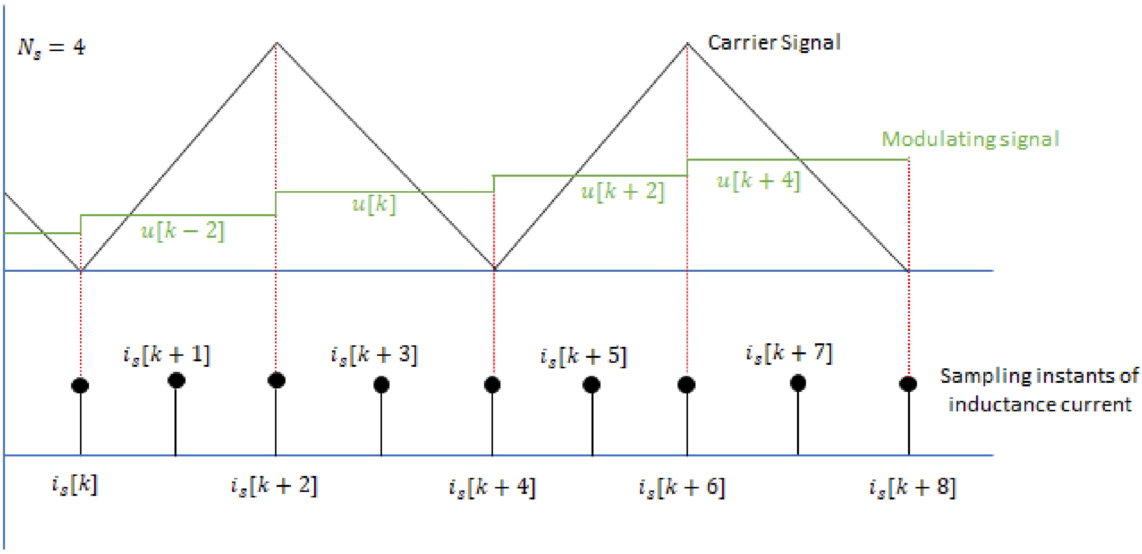
- **Ns:** Number of samples per switching period.

The value of Ns should be in base 2. (i.e. 2, 4, 8, 16)

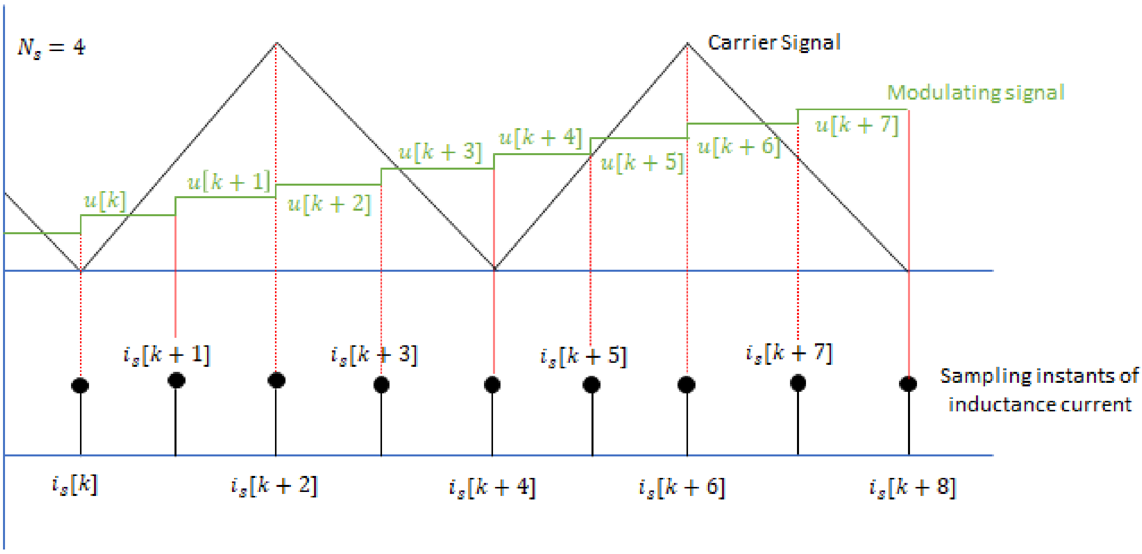
"Oversampling" and "Single update"



"Oversampling" and "Double update"



"Oversampling" and "Multisampling update"



If the Digital Filter option is checked, then the user can define:

<u>IIR First order</u>

- **Kdf:** Gain of the first order Low-Pass Filter.
- **Fdf:** Cutoff frequency of the Low-Pass Filter (Hz).

<u>IIR Second order</u>

- **Kdf:** Gain of the first order Low-Pass Filter.
- **Fdf:** Cutoff frequency of the Low-Pass Filter (Hz).
- **Ddf:** Damping ratio of the Low-Pass Filter.

<u>FIR Moving Average</u>

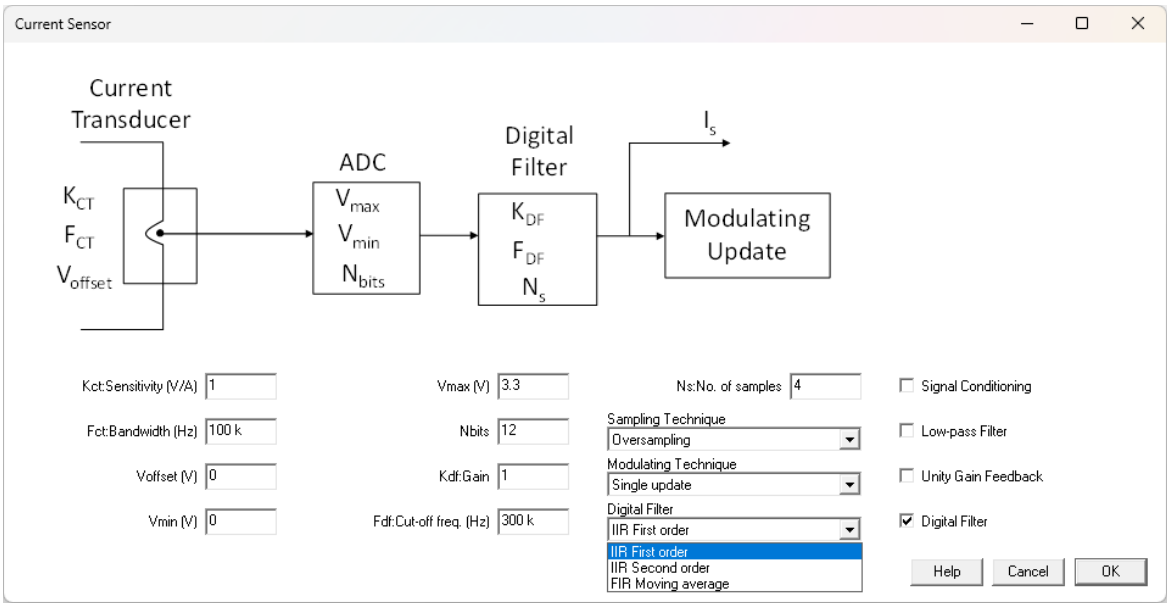
- This option can only be selected when the multisampling technique has been chosen.
- In this transfer function the following calculation is used:

$$i_s = \frac{1}{N_s} \cdot (i[k] + i[k+1] + i[k+2] + \cdots + i[N_s - 1])$$

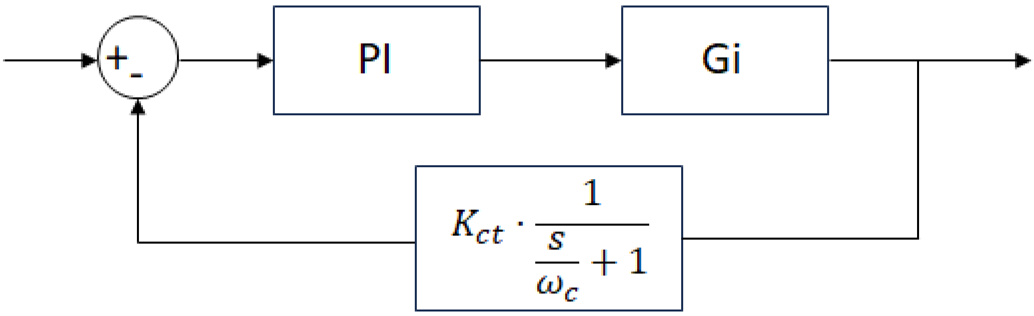
The transfer functions of the IIR first order and IIR second order have been discretized using the Backward Euler method. The sampling period (Ts) of the Digital Filter is equal to:

- Synchronized sampling → single update → Ts = Tsw
- Synchronized sampling → double update → Ts = 0.5·Tsw

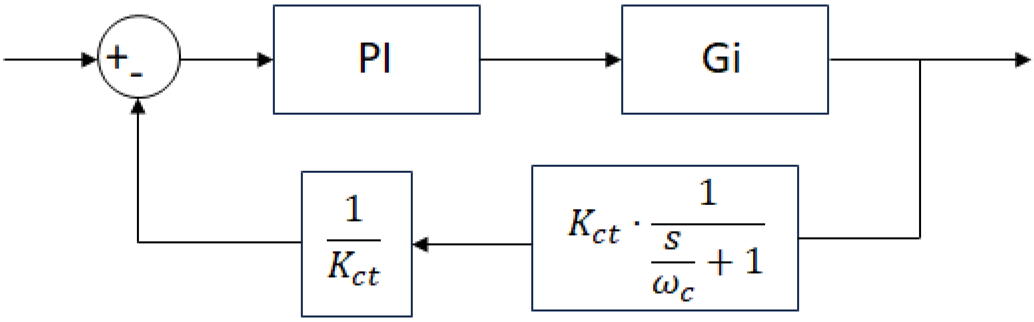
- Oversampling ⟶ Ts = Tsw/Ns



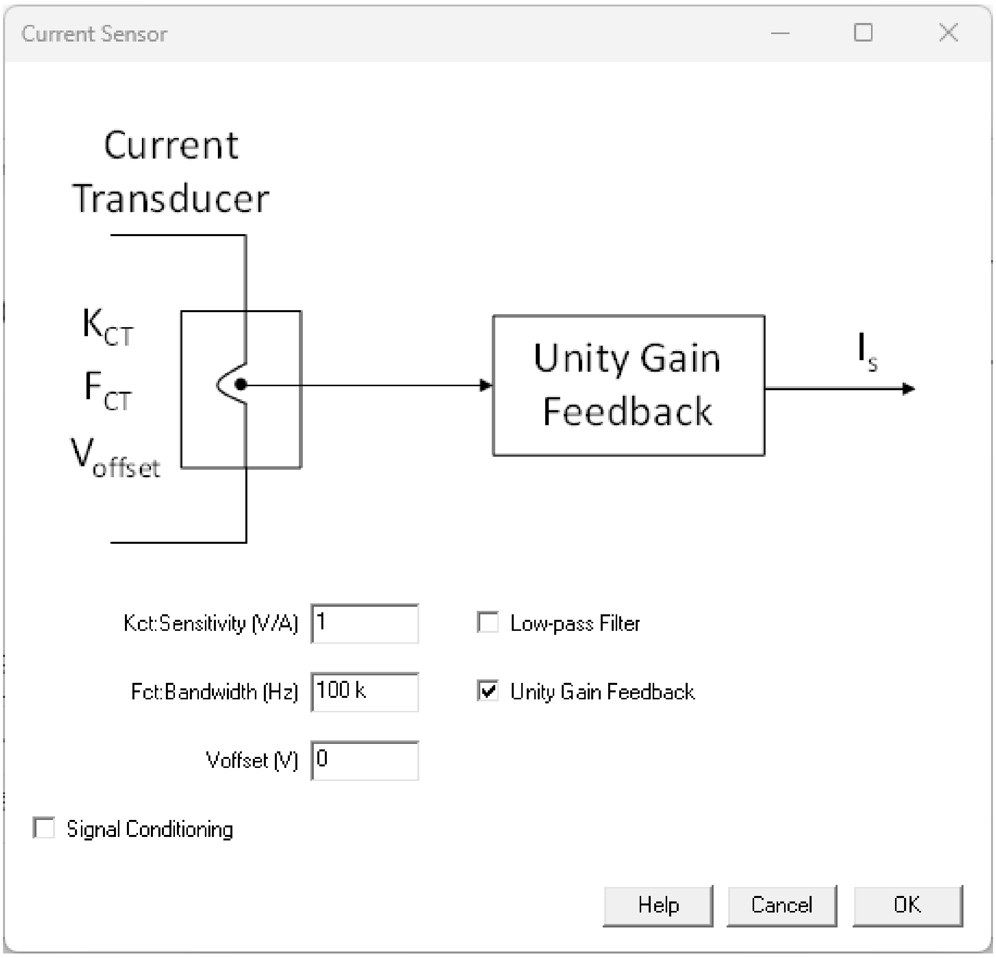
If the unity gain feedback option is checked then the static gain of the entire sensing chain is compensated.



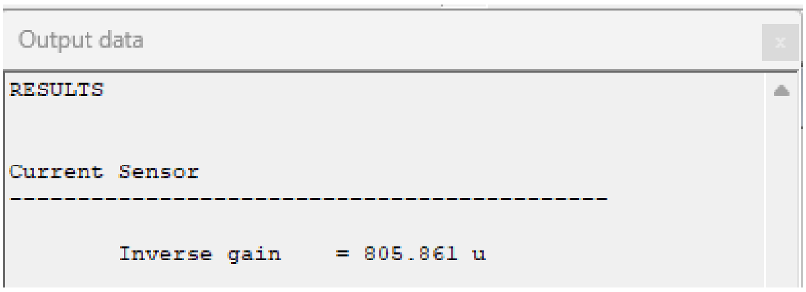
Without unity gain feedback



With unity gain feedback



The total value of the inverse gain is shown in the output report .



1.8.8 Grid Voltage sensor

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Grid Voltage sensor

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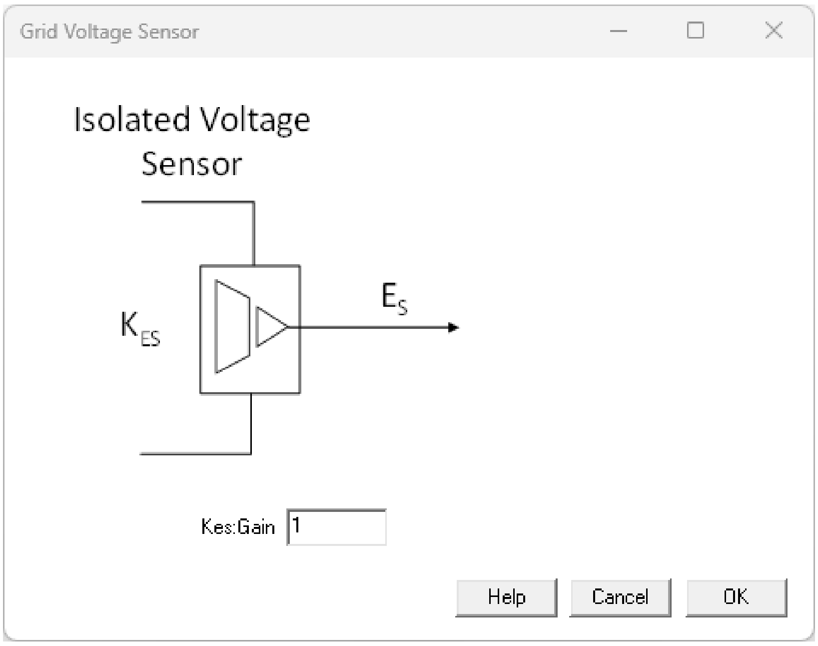
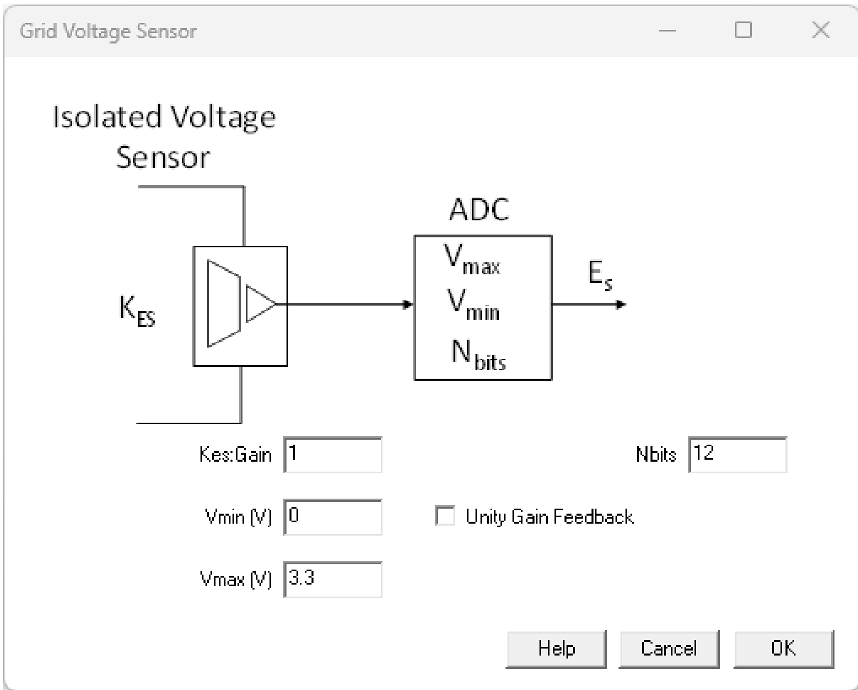
In the grid voltage sensor window, the user can define the gain of the isolated voltage.

- **KES:** Gain of the isolated voltage sensor

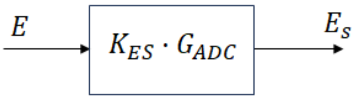


If the Digital option is checked in the Single-Line Diagram window, then the user can define:

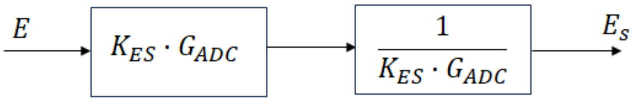
- **Vmax:** Maximum voltage of the ADC can read, used to calculate its gain.
- **Vmin:** Minimum voltage of the ADC can read, used to calculate its gain.
- **Nbits:** Number of bits of the ADC to represent the analog input value.



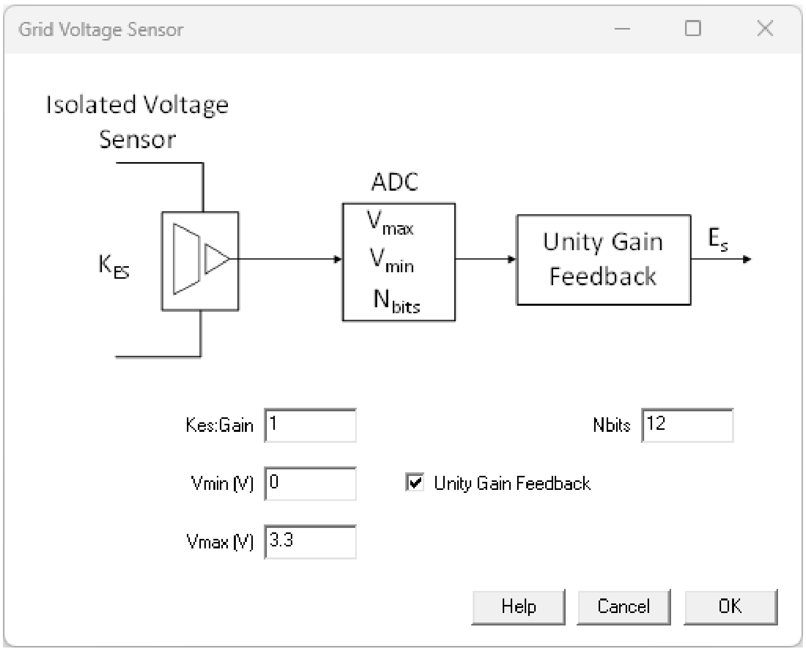
If the unity gain feedback option is checked then the static gain of the entire sensing chain is compensated.



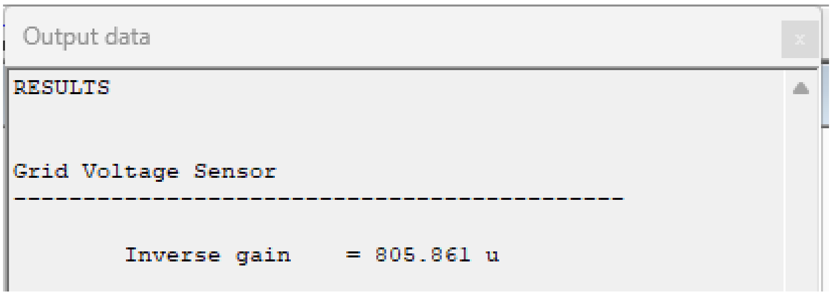
Without unity gain feedback



With unity gain feedback



The total value of the inverse gain is shown in the output report .



1.8.9 Output voltage sensor

Navigation: SmartCtrl > Three-Phase PFC Boost Converter >

Output Voltage sensor

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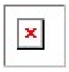
In the output voltage sensor window, the user can define the gain and bandwidth of the isolated voltage sensor.

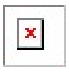
- **Kvs:** Gain of the voltage sensor
- **Fvs:** Bandwidth of the isolated voltage sensor (Hz)



If the Signal Conditioning option is checked then the user can define:

- **Ksc:** Gain of the signal conditioning stage
- **Fsc:** Bandwidth of the signal conditioning stage (Hz)

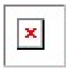
The transfer function contemplated in the signal conditioning stage is a first order low-pass filter.



If the Low-Pass Filter option is checked then the user can define:

- **Klpf:** Gain of the Low-Pass Filter stage
- **Flpf:** Cutoff frequency of the Low-Pass Filter (Hz)
- **Dlpf:** Damping ratio of the Low-Pass Filter

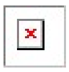
The transfer function contemplated in the Low-Pass Filter stage is a second order low-pass filter. This stage represents an anti-aliasing filter.



If the Digital option is checked in the Single-Line Diagram window, then the user can define:

- **Vmax:** Maximum voltage of the ADC can read, used to calculate its gain.
- **Vmin:** Minimum voltage of the ADC can read, used to calculate its gain.
- **Nbits:** Number of bits of the ADC to represent the analog input value. This number affects the calculation of the reference.

The user can choose the sampling technique between synchronized and oversampling.



If the Digital Filter option is checked, then the user can define:

<u>IIR First order</u>

  - **Kdf:** Gain of the first order Low-Pass Filter.

○ **Fdf:** Cut off frequency of the Low-Pass Filter (Hz).

IIR Second order

○ **Kdf:** Gain of the first order Low-Pass Filter.

○ **Fdf:** Cutoff frequency of the Low-Pass Filter(Hz).

○ **Ddf:** Damping ratio of the Lowe-Pass Filter.

FIR Moving Average

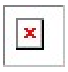
○ This option can only be selected when the multisampling technique has been chosen.

○ In this transfer function the following calculation is used:

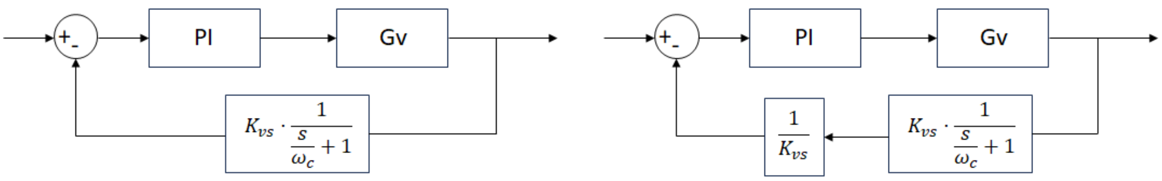
$$v_s = \frac{1}{N_s} \cdot (v[k] + v[k+1] + v[k+2] + \cdots + v[N_s - 1])$$

The transfer functions of the IIR first order and IIR second order have been discretized using the Backward Euler method. The sampling period (Ts) of the Digital Filter is equal to:

- Synchronized sampling → single update → Ts = Tsw
- Synchronized sampling → double update → Ts = 0.5·Tsw
- Oversampling → Ts = Tsw/Ns

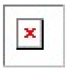


If the unity gain feedback option is checked then the static gain of the entire sensing chain is compensated.

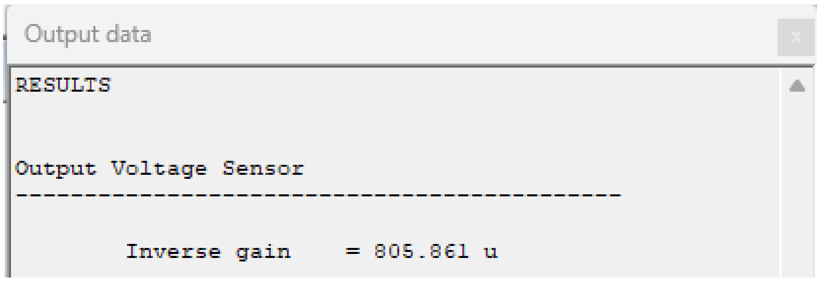


Without unity gain feedback

With unity gain feedback



The total value of the inverse gain is shown in the output report .



1.8.10 Modulator

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Modulators

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1.8.10.1 Digital

Navigation: SmartCtrl > Three-Phase PFC Boost Converter > Modulator >

Digital

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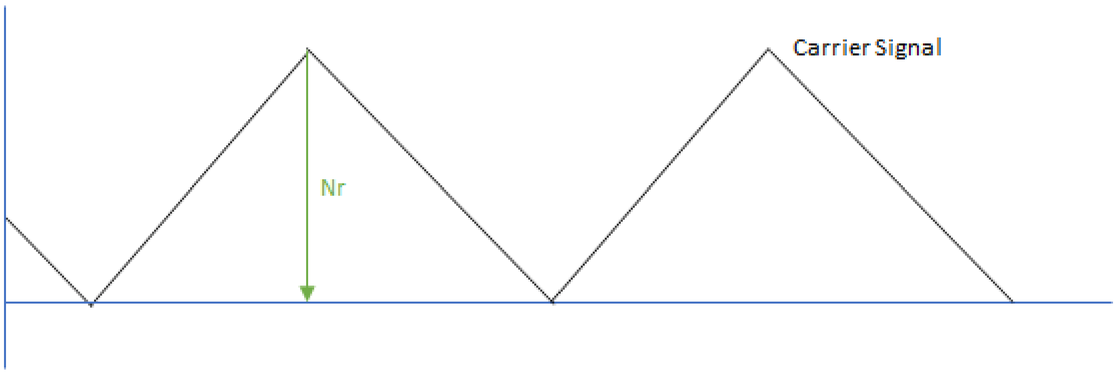
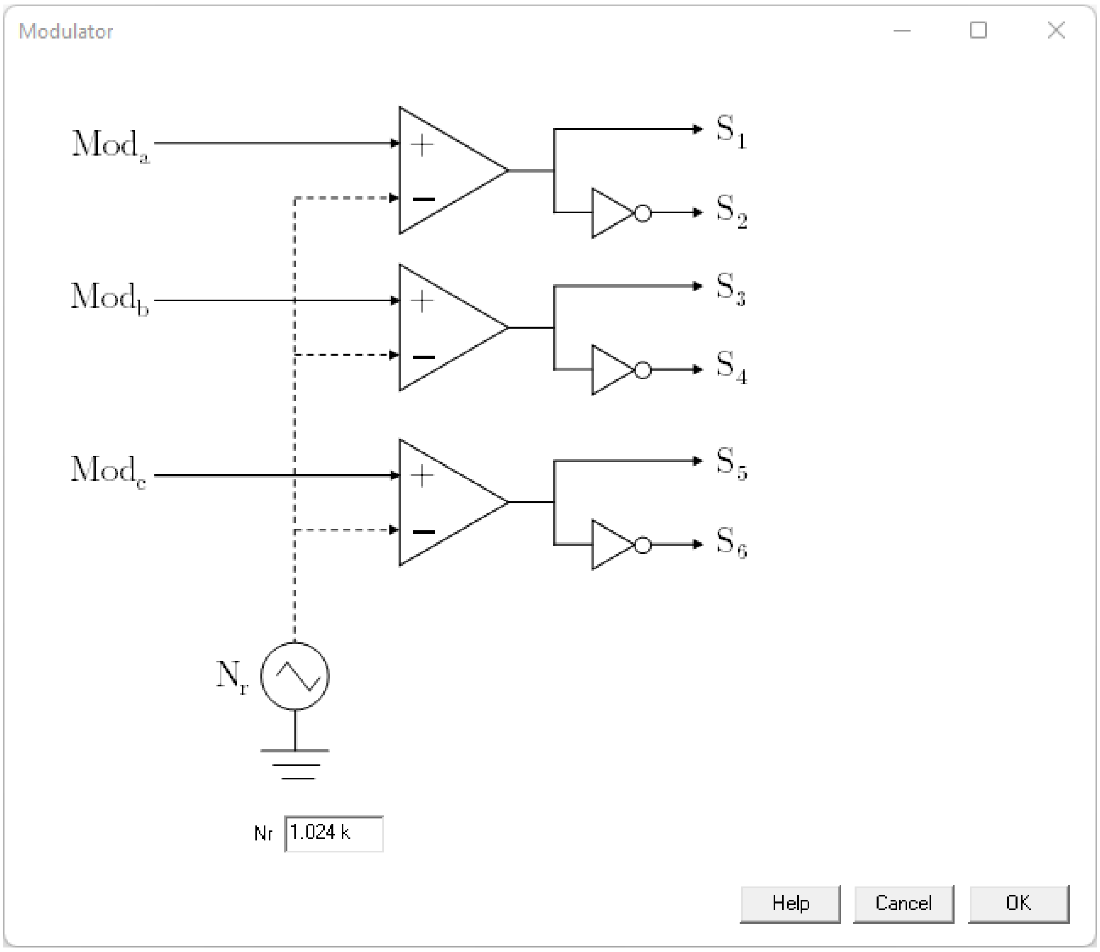
In the modulator window, the user can define:

- **Nr:** Number of steps of the carrier signal





1.8.10.2 Analog

Navigation: SmartCtrl > Three-Phase PFC Boost Converter > Modulator >

Analog

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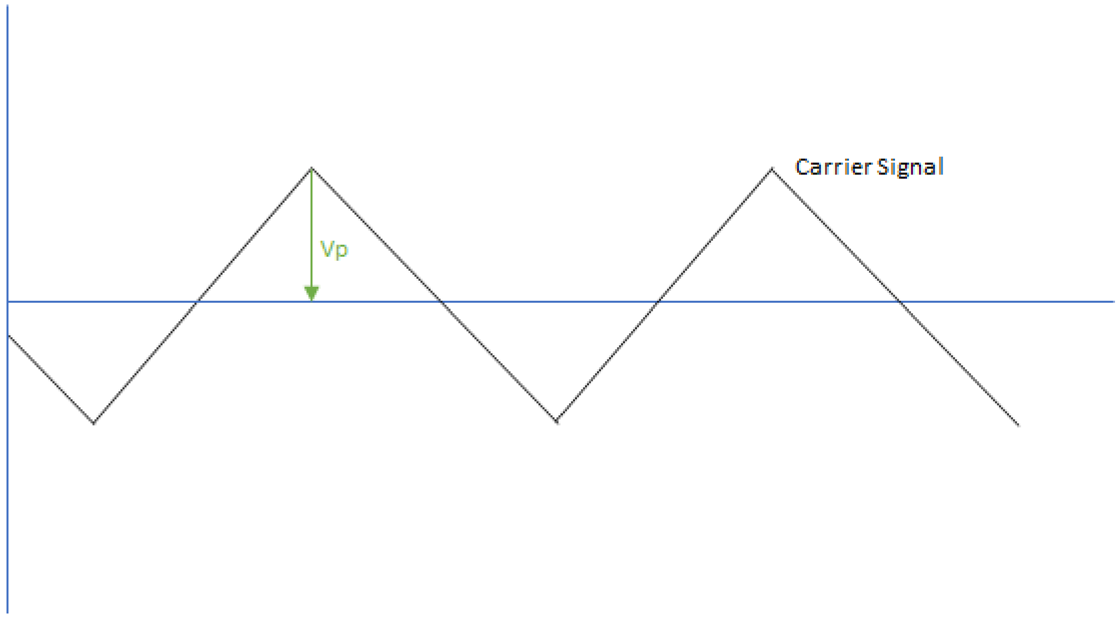
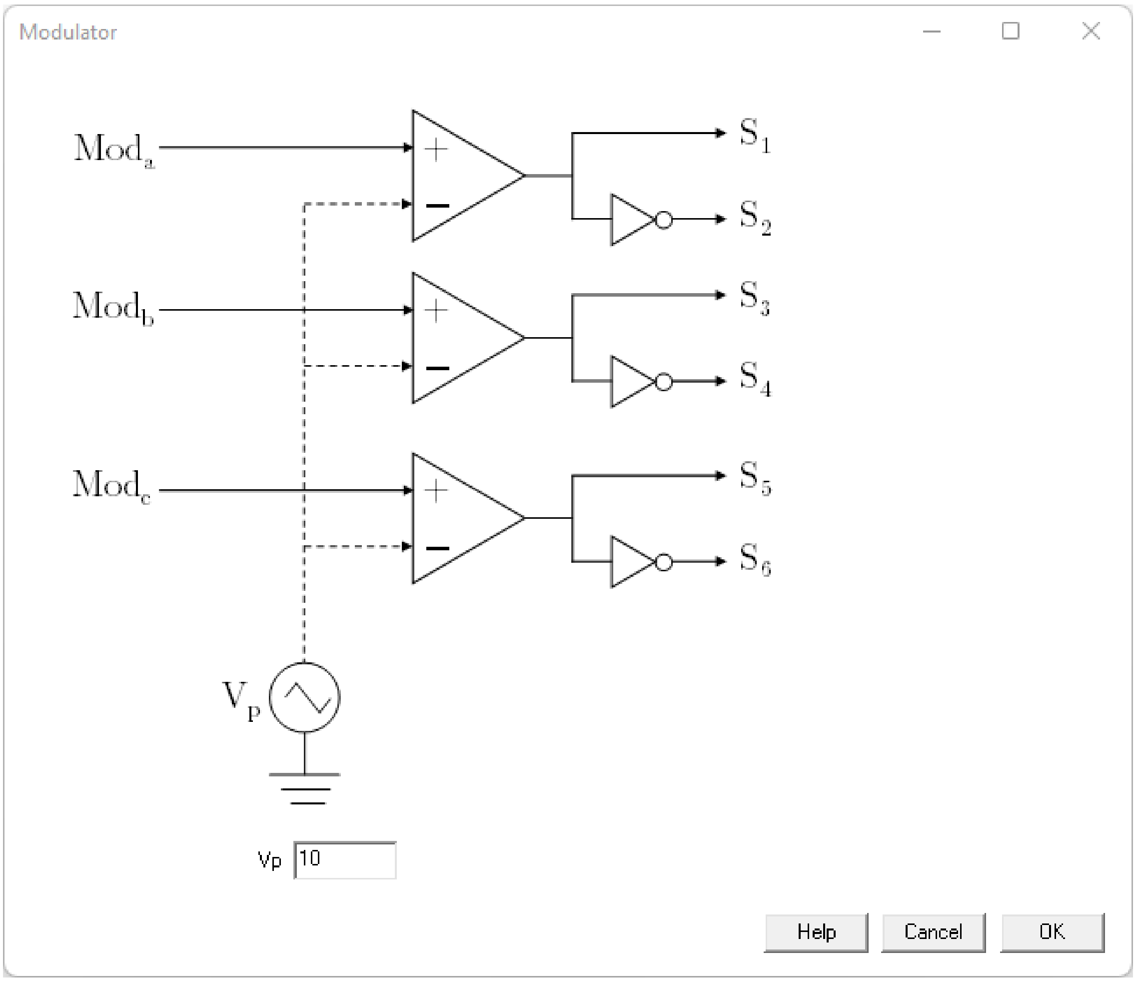
In the modulator window, the user can define:

- **Vp**: Peak value of the carrier signal


Carrier Signal
Vp


Modulator
Mod_a
Mod_b
Mod_c
S1
S2
S3
S4
S5
S6
Vp
Vp 10
Help
Cancel
OK

1.8.11 Inductor Current Compensator

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Inductor Current Compensator

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1.8.11.1 PI

Navigation: SmartCtrl > Three-Phase PFC Boost Converter > Inductor Current Compensator >

PI

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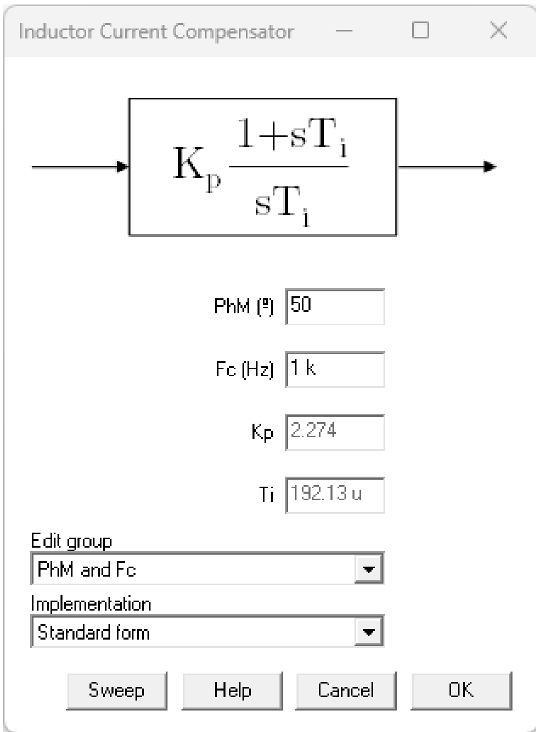
In the inductor current compensator window, the user can select standard or parallel implementation.

If standard implementation is selected, then the user can modify:

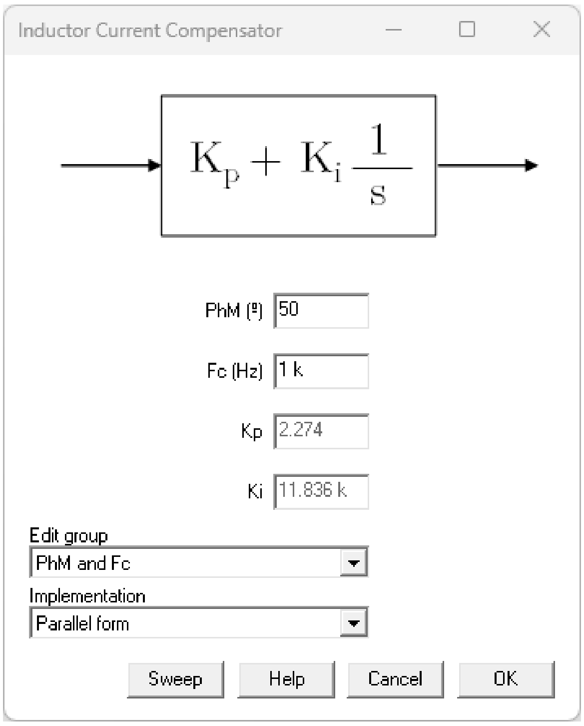
- **PhM:** Phase margin in degrees
- **Fc:** Crossover frequency in Hz
- **Kp:** Proportional constant of the PI
- **Ti:** Time constant of the PI



If parallel implementation is selected, then the user can modify:

- **PhM:** Phase margin in degrees

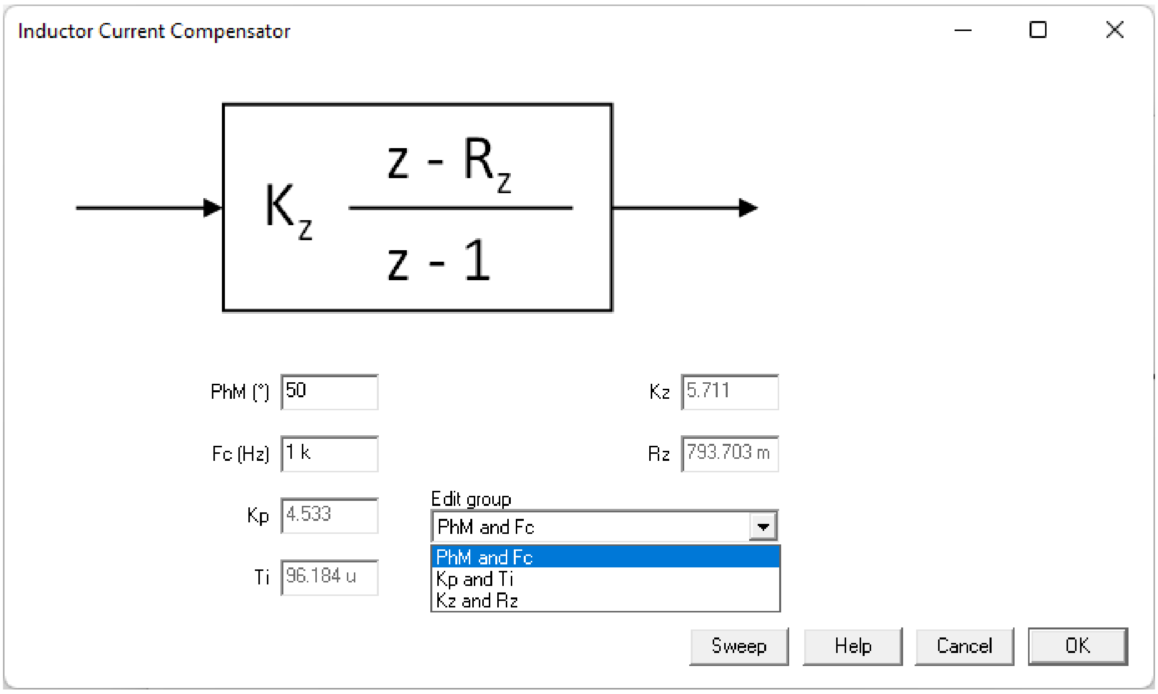
- **Fc:** Crossover frequency in Hz
- **Kp:** Proportional constant of the PI
- **Ki:** Integral constant of the PI



When the PI compensator is discrete, the user can modify:

- **PhM:** Phase margin in degrees
- **Fc:** Crossover frequency in Hz
- **Kp:** Proportional constant of the PI (s-domain)
- **Ti:** Time constant of the PI (s-domain)
- **Kz:** Gain of the transfer function of the PI compensator (z-domain)
- **Rz:** Zero of the transfer function of the PI compensator (z-domain)

To consider a discrete compensator, the digital checkbox in the Single-Line Diagram window must be checked.



The sampling frequency of the compensator is related to the update of the modulating signal that is defined in the current sensor window.

The sampling period (Ts) of the inductor current compensator is equal:

- Single update → Ts = Tsw
- Double update → Ts = 0.5·Tsw
- Multisampling update → Ts =Tsw/Ns

The user can also design the current control loop with the solutions map  option that is located in the menu bar.

1.8.11.2 P-Resonant

Navigation: SmartCtrl > Three-Phase PFC Boost Converter > Inductor Current Compensator >

P-Resonant Previous Top Next

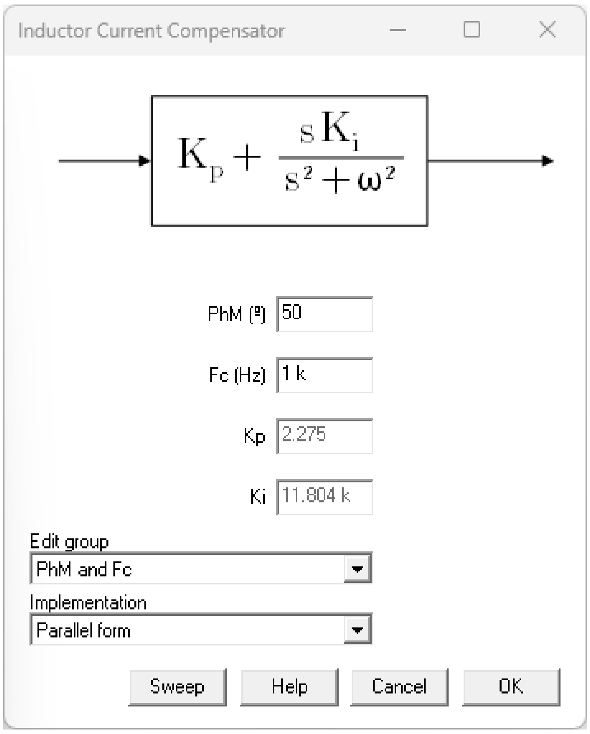
In the inductor current compensator window, the user can modify:

- **PhM:** Phase margin in degrees
- **Fc:** Crossover frequency in Hz
- **Kp**: Proportional constant of the PI

- **Ki**: Integral constant of the PI

In this compensator the ω is calculated as follows:

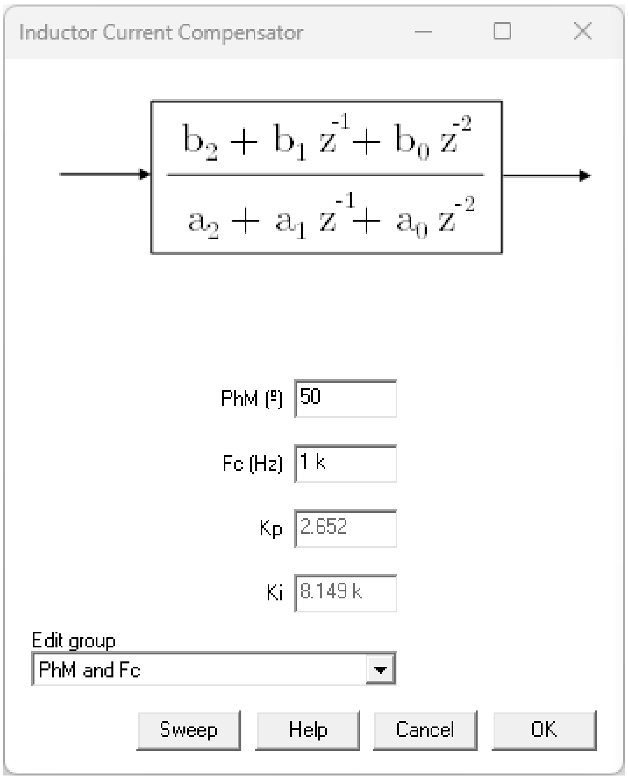
$$\omega = 2 \cdot \pi \cdot f_{line}$$



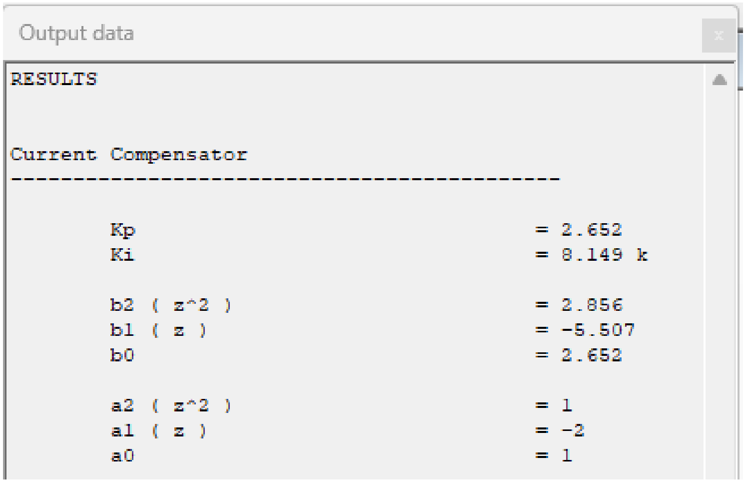
When the P-Resonant compensator is discrete, the user can modify:

- **PhM**: Phase margin in degrees
- **Fc**: Crossover frequency in Hz
- **Kp**: Proportional constant of the PI
- **Ki**: Integral constant of the PI

To consider a discrete compensator, the digital checkbox in the Single-Line Diagram window must be checked.



The values of the coefficients are displayed in the output data window that is in the menu bar. The transfer function of the compensator has been discretized using Backward Euler method.



The sampling frequency of the compensator is related to the update of the modulating signal that is defined in the current sensor window.

The sampling period (Ts) of the inductor current compensator is equal:

- Single update → Ts = Tsw
- Double update → Ts = 0.5·Tsw

- Multisampling update → Ts =Tsw/Ns

1.8.12 Output Voltage Compensator

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Output Voltage Compensator

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1.8.12.1 PI

Navigation: SmartCtrl > Three-Phase PFC Boost Converter > Output Voltage Compensator >

PI

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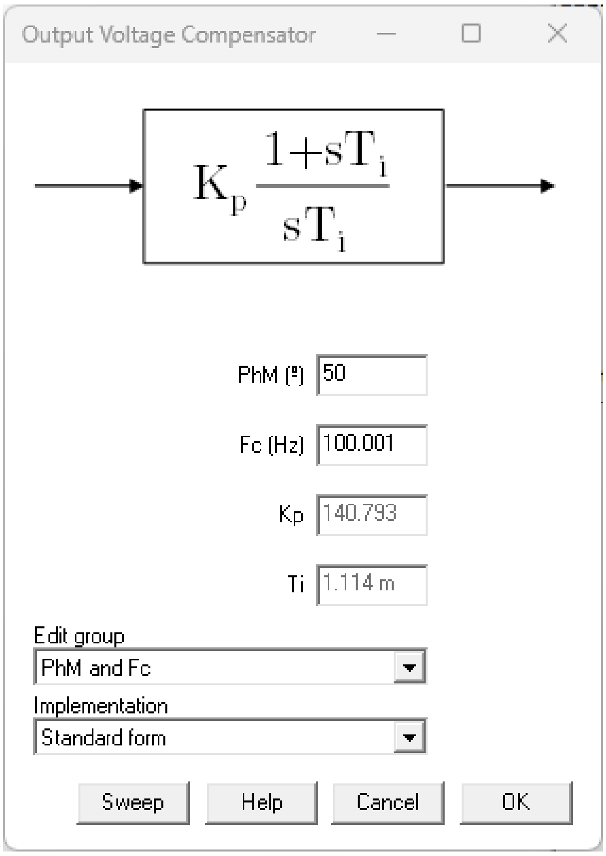
In the output voltage compensator window, the user can select standard or parallel implementation.

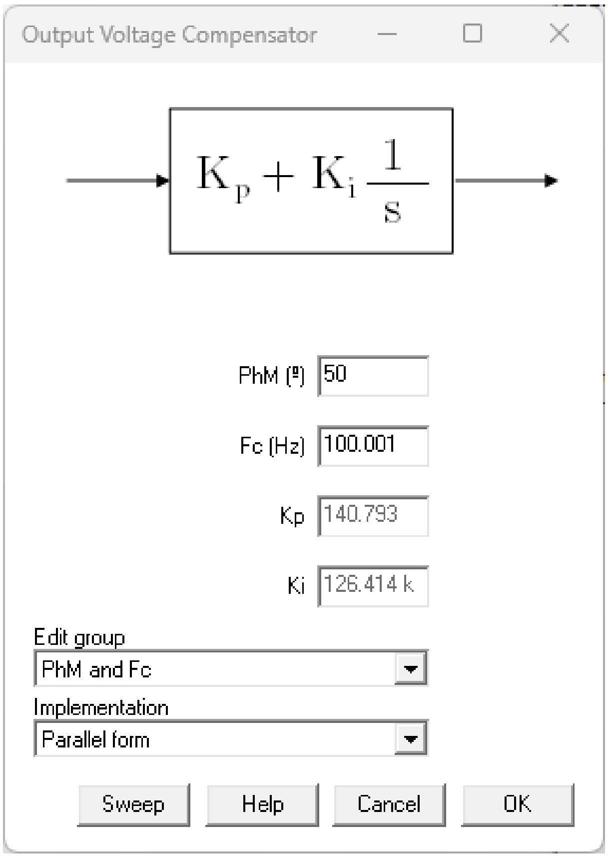
If standard implementation is selected, then the user can modify:

- **PhM**: Phase margin in degrees
- **Fc**: Crossover frequency in Hz
- **Kp**: Proportional constant of the PI
- **Ti**: Time constant of the PI



If parallel implementation is selected, then the user can modify:

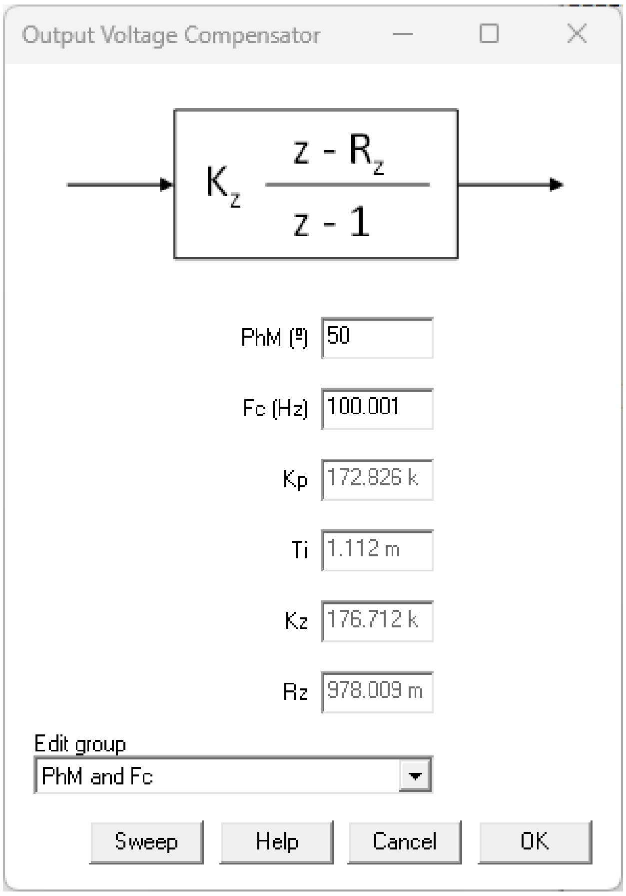
- **PhM**: Phase margin in degrees
- **Fc**: Crossover frequency in Hz
- **Kp**: Proportional constant of the PI
- **Ki**: Integral constant of the PI



When the PI compensator is discrete, the user can modify:

- **PhM**: Phase margin in degrees
- **Fc**: Crossover frequency in Hz
- **Kp**: Proportional constant of the PI (s-domain)
- **Ti**: Time constant of the PI (s-domain)
- **Kz**: Gain of the transfer function of the PI compensator (z-domain)
- **Rz**: Zero of the transfer function of the PI compensator (z-domain)

To consider a discrete compensator, the digital checkbox in the Single-Line Diagram window must be checked.



The sampling frequency of the compensator is related to the update of the modulating signal that is defined in the current sensor window.

The sampling period (Ts) of the output voltage compensator is equal:

- Single update → Ts = Tsw
- Double update → Ts = 0.5·Tsw
- Multisampling update → Ts =Tsw/Ns

The user can also design the output voltage control loop with the solutions map  option that is located in the menu bar.

1.8.13 Export

Navigation: SmartCtrl > Three-Phase PFC Boost Converter >

Export

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1.8.13.1 PSIM

Navigation: SmartCtrl > Three-Phase PFC Boost Converter > Export >

PSIM

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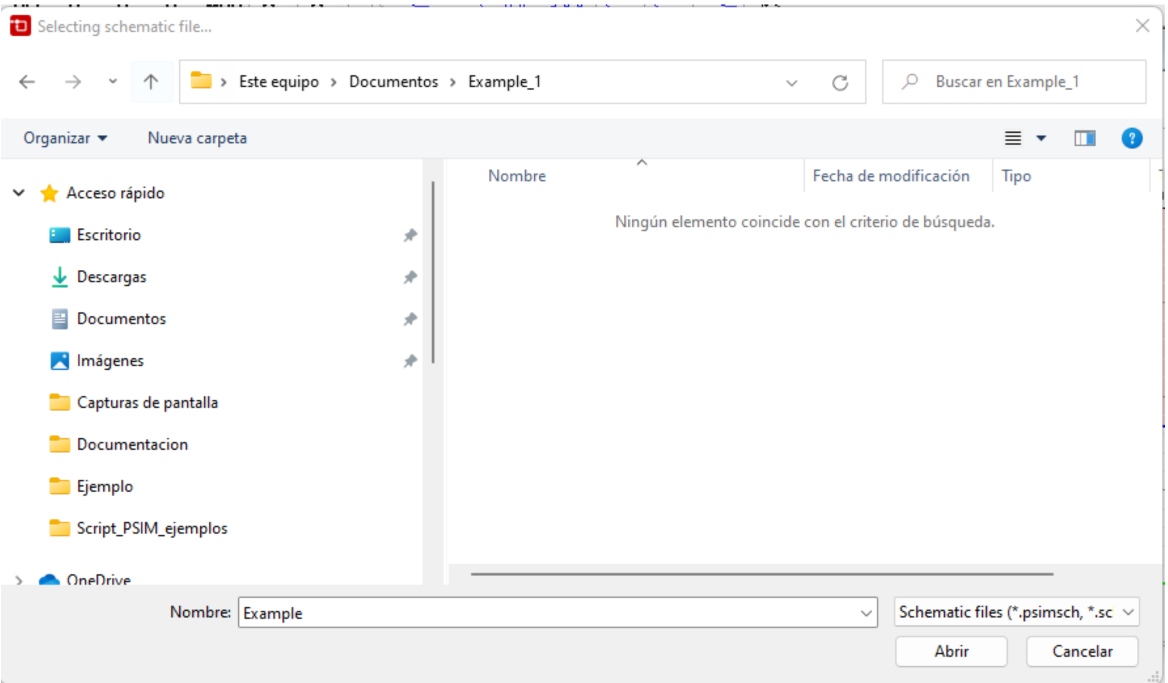
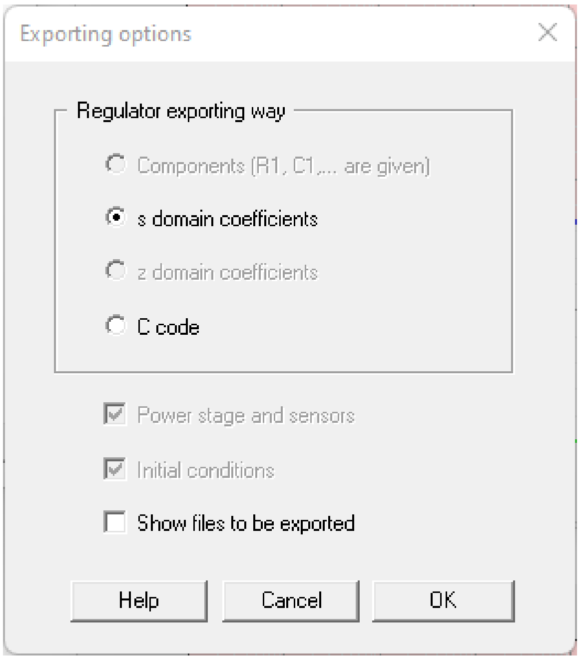
SmartCtrl provides a link with PSIM software. Once the regulator has been designed, the power stage and the compensator can be exported to PSIM, providing an automatic generation of the schematic and/or an exportation of the parameters of the design performed in SmartCtrl. This schematic can be used to validate the design using PSIM.

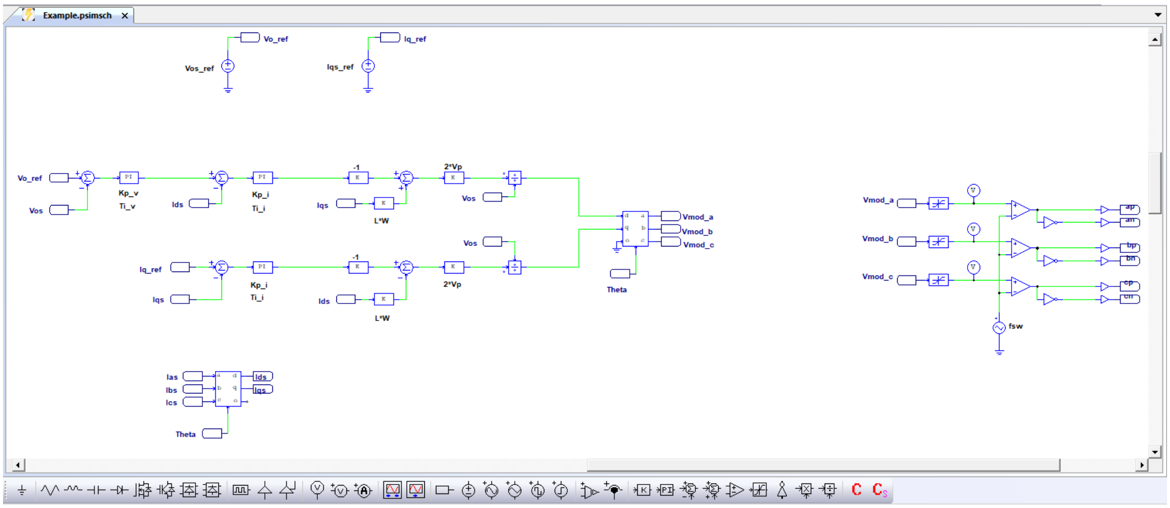
In the first step the user will be asked to select the path and the name of the PSIM file in which the schematic will be inserted. If the file has not already been created, a new PSIM file will be created with the name provided by the user.



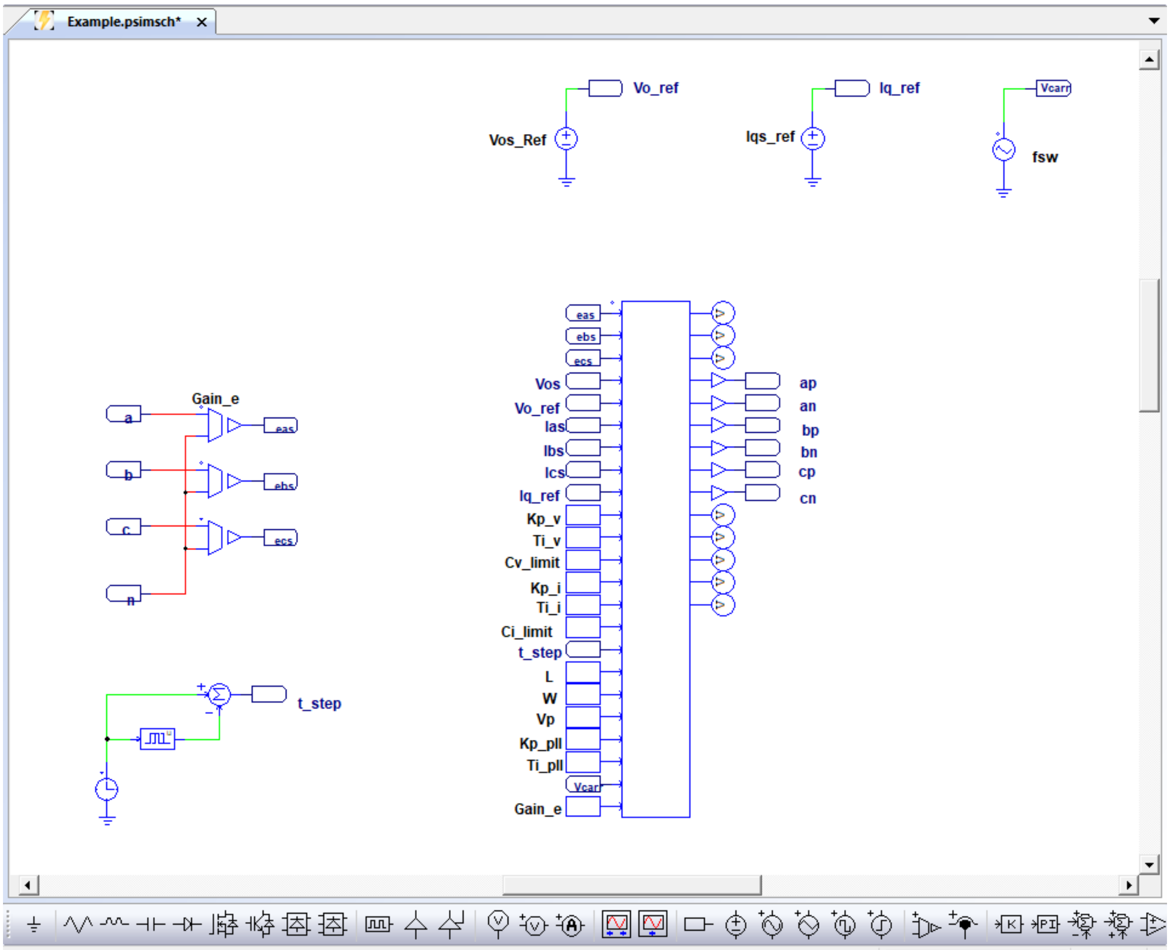
In the next step, the user will be asked to choose between different options:



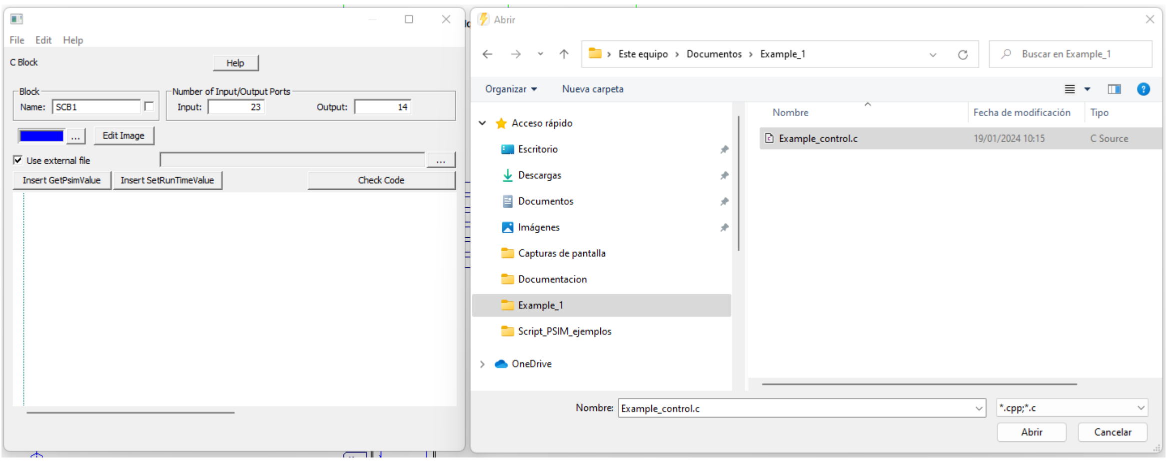
- “s-domain coefficients”: the schematic and parameters of the compensator will be exported in the form of PSIM control blocks, like in the following example.



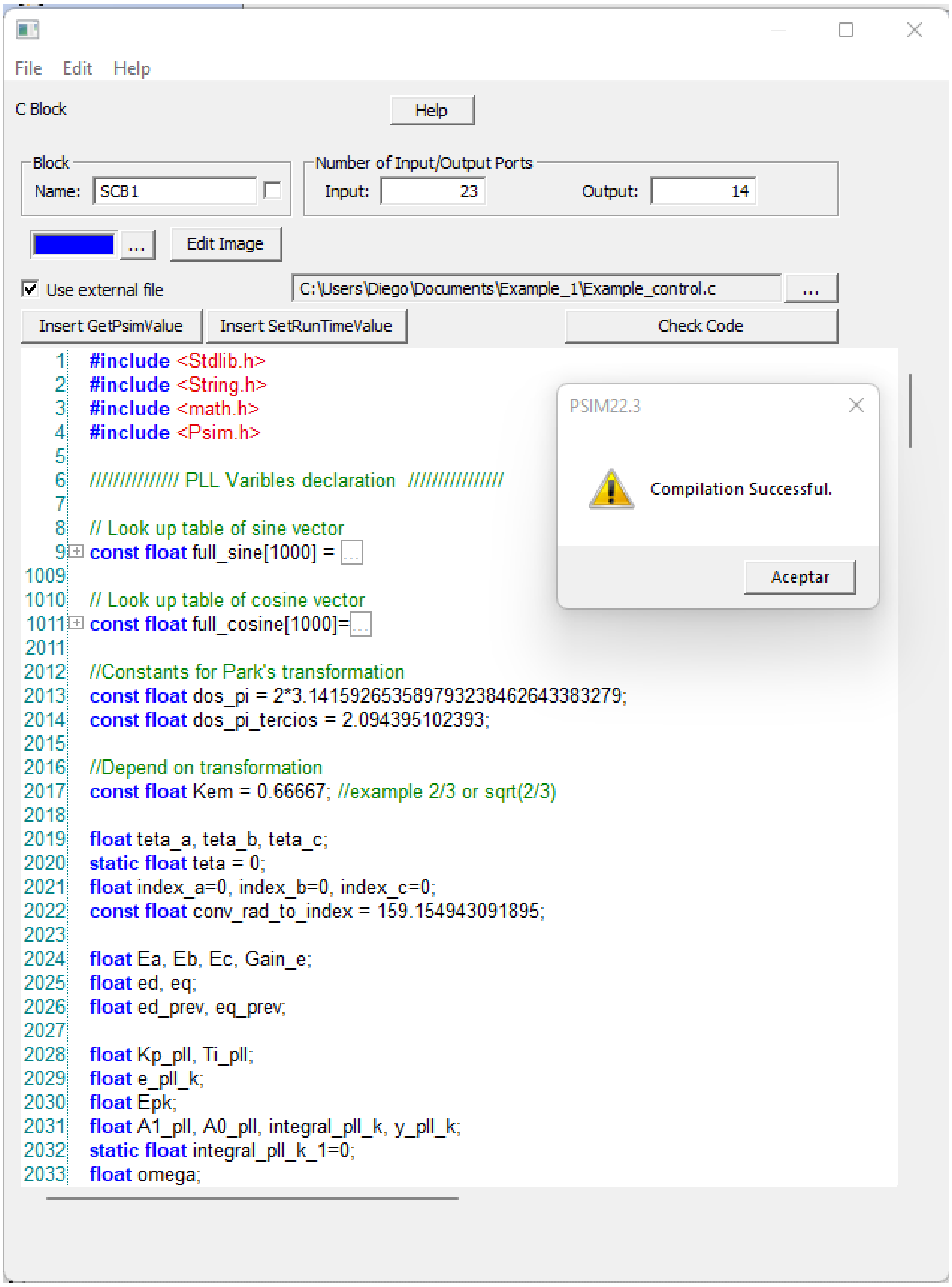
- “C code”: the power stage and the sensing stage will be exported in the form of PSIM control blocks. The control stage and modulator will be exported in a DLL.



Once the simulation schematic has been created, the .c file must be loaded into the DLL. Double-click on the DLL block and select the option “Use external file”. Then select the path where the .c file was saved.



The user can check that the code has been loaded correctly. Finally, the user can proceed to run the simulation.


File Edit Help
C Block
Help
Block
Name: SCB1
Number of Input/Output Ports
Input: 23
Output: 14
Edit Image
Use external file
C:\Users\Diego\Documents\Example_1\Example_control.c
Insert GetPsimValue
Insert SetRunTimeValue
Check Code
#include <Stdlib.h>
#include <String.h>
#include <math.h>
#include <Psim.h>
////////////// PLL Varibles declaration ///////////////
// Look up table of sine vector
const float full_sine[1000] =
// Look up table of cosine vector
const float full_cosine[1000]=
//Constants for Park's transformation
const float dos_pi = 2*3.14159265358979323846264338327 9;
const float dos_pi_tercios = 2.094395102393;
//Depend on transformation
const float Kem = 0.66667; //example 2/3 or sqrt(2/3)
float teta_a, teta_b, teta_c;
static float teta = 0;
float index_a=0, index_b=0, index_c=0;
const float conv_rad_to_index = 159.154943091895;
float Ea, Eb, Ec, Gain_e;
float ed, eq;
float ed_prev, eq_prev;
float Kp_pll, Ti_pll;
float e_pll_k;
float Epk;
float A1_pll, A0_pll, integral_pll_k, y_pll_k;
static float integral_pll_k_1=0;
float omega;
PSIM22.3
Compilation Successful.
Aceptar

1.8.13.2 SIMBA

Navigation: SmartCtrl > Three-Phase PFC Boost Converter > Export >

SIMBA

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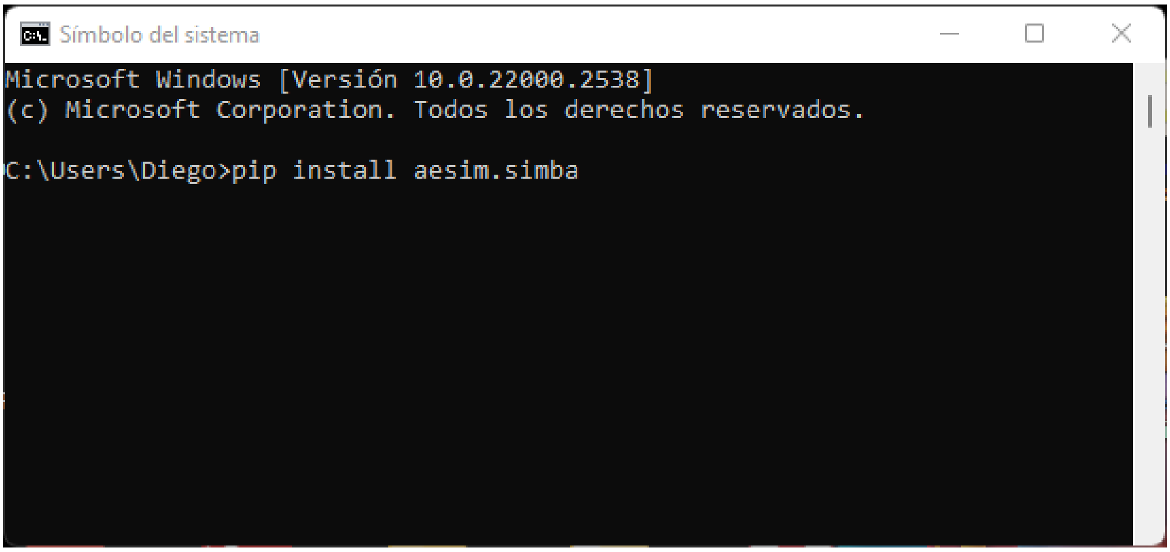
The requirements to use this function are:

- Python 3.10 or later.

- The SIMBA Python API must be installed. The easiest way to install the Python API is using pip install aesim.simba in command windows.



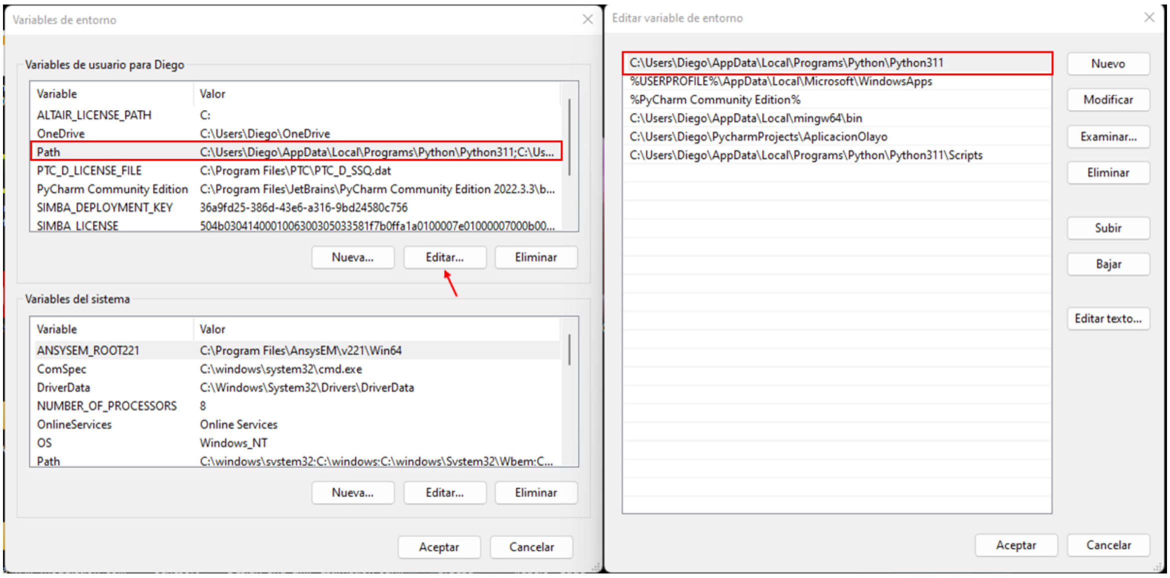
More information:

https://pypi.org/project/pip/

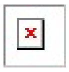
https://pypi.org/project/aesim.simba/

- Have a valid license and the SIMBA executable file (SIMBA.exe).

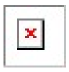
In order to SmartCtrl can create the .jsimba file, it is necessary to go to the system environment variables. Then, select the variable called “Path” and click on edit button. Finally, at the top, the path to the version of Python that the user has installed must be entered.



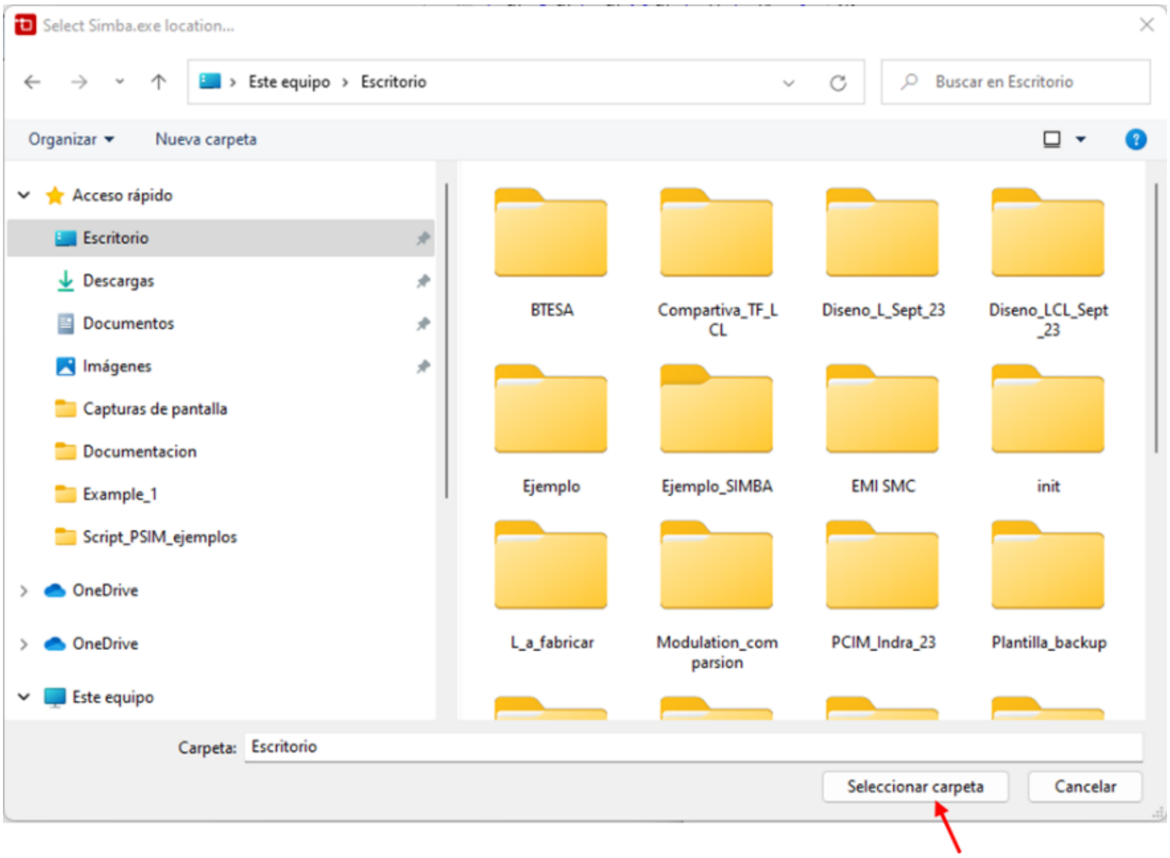
SmartCtrl provides a link with SIMBA software. Once the regulator has been designed, the power stage and the compensator can be exported to SIMBA, providing an automatic generation of the schematic and/or an exportation of the parameters of the design performed in SmartCtrl. This schematic can be used to validate the design using SIMBA.



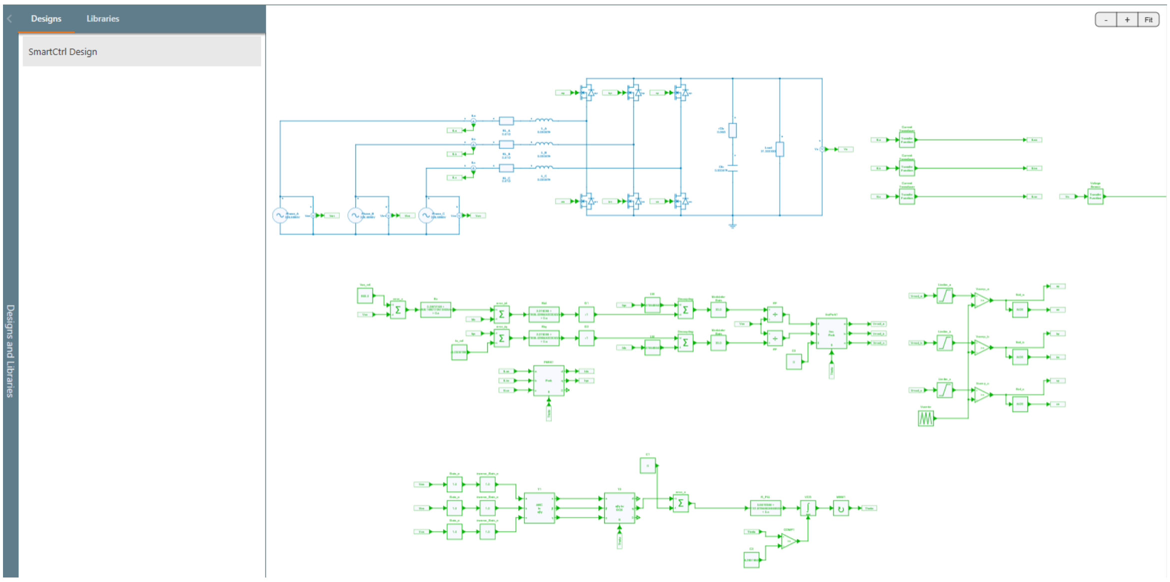
In the first step the user will be asked to select the path and the name of the SIMBA file in which the schematic will be inserted. If the file has not already been created, a new SIMBA file will be created with the name provided by the user.



The first time this option is used, it is necessary to specify the path where the SIMBA.exe file is located. Then click on Select folder button.



The schematic and parameters of the compensator will be exported in the form of SIMBA control blocks, like in the following example. Finally, the user can proceed to run the simulation.



1.8.14 Graphics

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Graphics

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1.8.14.1 Bode diagrams

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Bode diagrams

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The Bode plot is used to characterize the frequency response of the system. It consists of two different graphs, the magnitude plot and the phase plot versus frequency. Frequency is plotted in a log axe.

The cross over frequency of the open loop is shown by means of a pair of dashed lines on the open loop transfer function of the system.

In SmartCtrl there are twenty-two different transfer functions that can be plotted in the Bode plot window.

G_{PLL}: Phase-Locked-Loop Plant

T_{PLL}: Phase-Locked-Loop Open Loop

G_{PLL}^{CL}: Phase-Locked-Loop Closed Loop

G_i: Current Plant

H_i: Current Sensor

H_E: Grid Voltage Sensor

H_v: Output Voltage Sensor

GH_i: Current Open Loop without Compensator

C_i: Current Compensator

T_i: Current Open Loop

G_i^{CL}: Current Closed Loop

G_v: Voltage Plant

GH_v: Voltage Open Loop without Compensator

C_v: Voltage Compensator

T_v: Voltage Open Loop

G_v^{CL}: Voltage Closed Loop

G_{vvd}: Closed Loop d-axis Audiosusceptibility

G_{vvq}: Closed Loop q-axis Audiosusceptibility

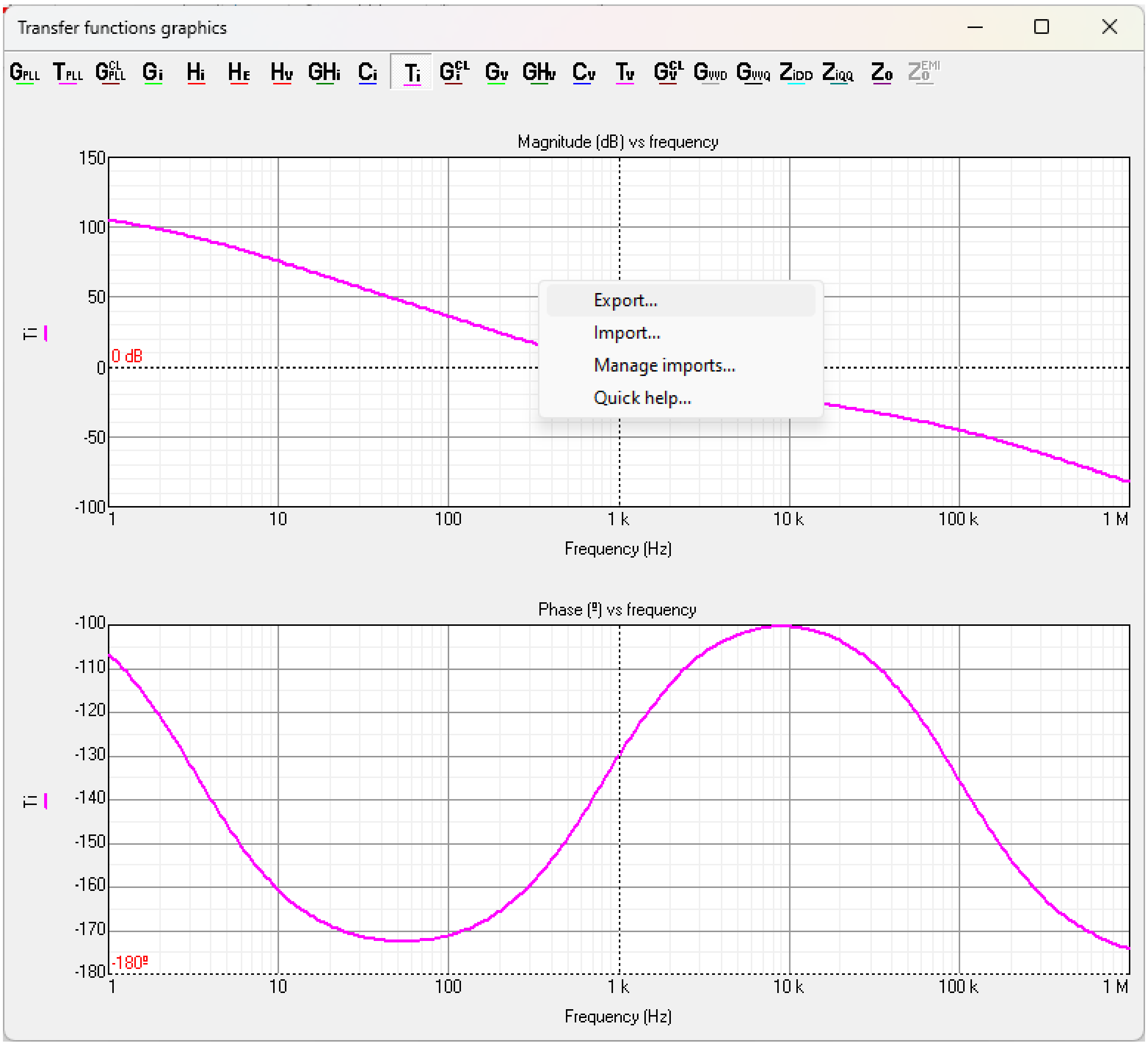
Z_{idd}: Closed Loop d-axis Input Impedance

Z_{iqq}: Closed Loop q-axis Input Impedance

Z_o: Closed Loop Output Impedance

Z_o^{EMI}: Output Impedance of EMI Filter

By right clicking on the bode diagram to export or import transfer functions.

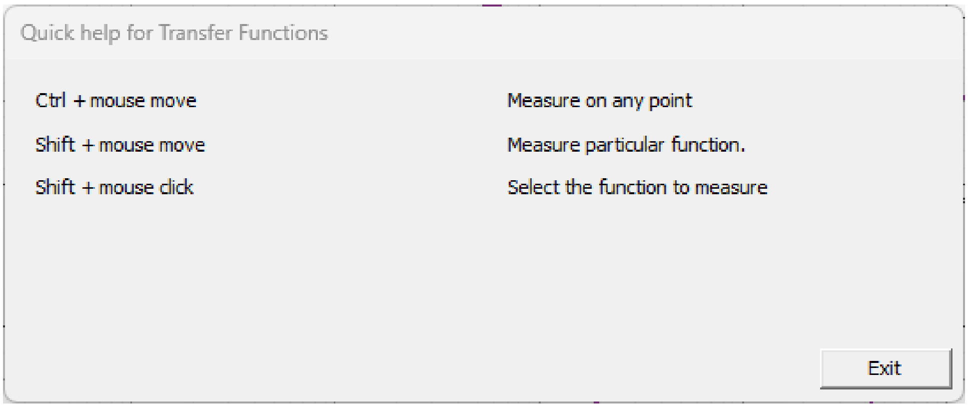


Export: This option allows exporting the data of the different frequency responses in several formats.

Import: Import data from an external file.

Manage imports: Allows the user to change the color, thickness and style of the trace representing the imported transfer function.

Quick help: Shows the keyboard shortcuts to measure directly on the plot.



1.8.14.2 Waveforms of PLL

Navigation: SmartCtrl > Three-Phase PFC Boost Converter > Graphics >

Waveforms of PLL

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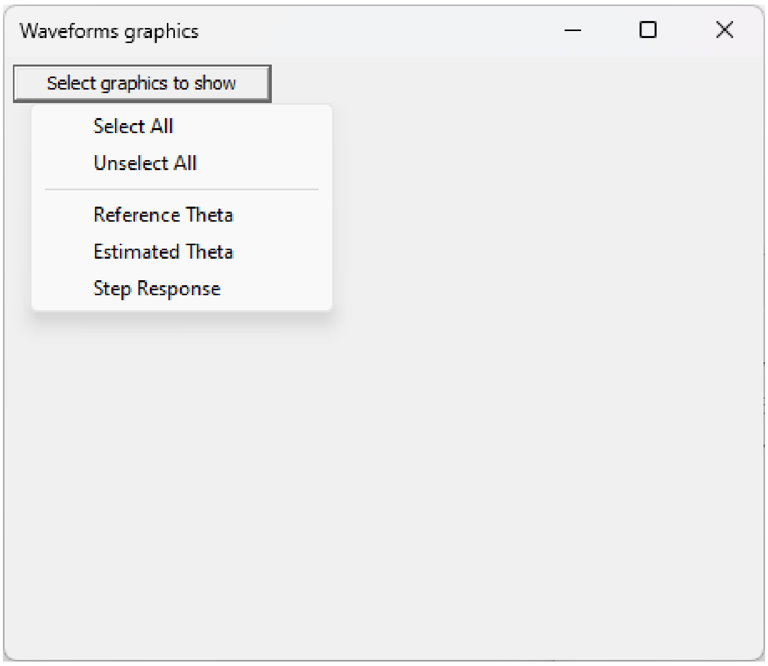
In the waveform window, the user can visualize the transient response of the PLL control loop when a phase step is injected at the reference angle.

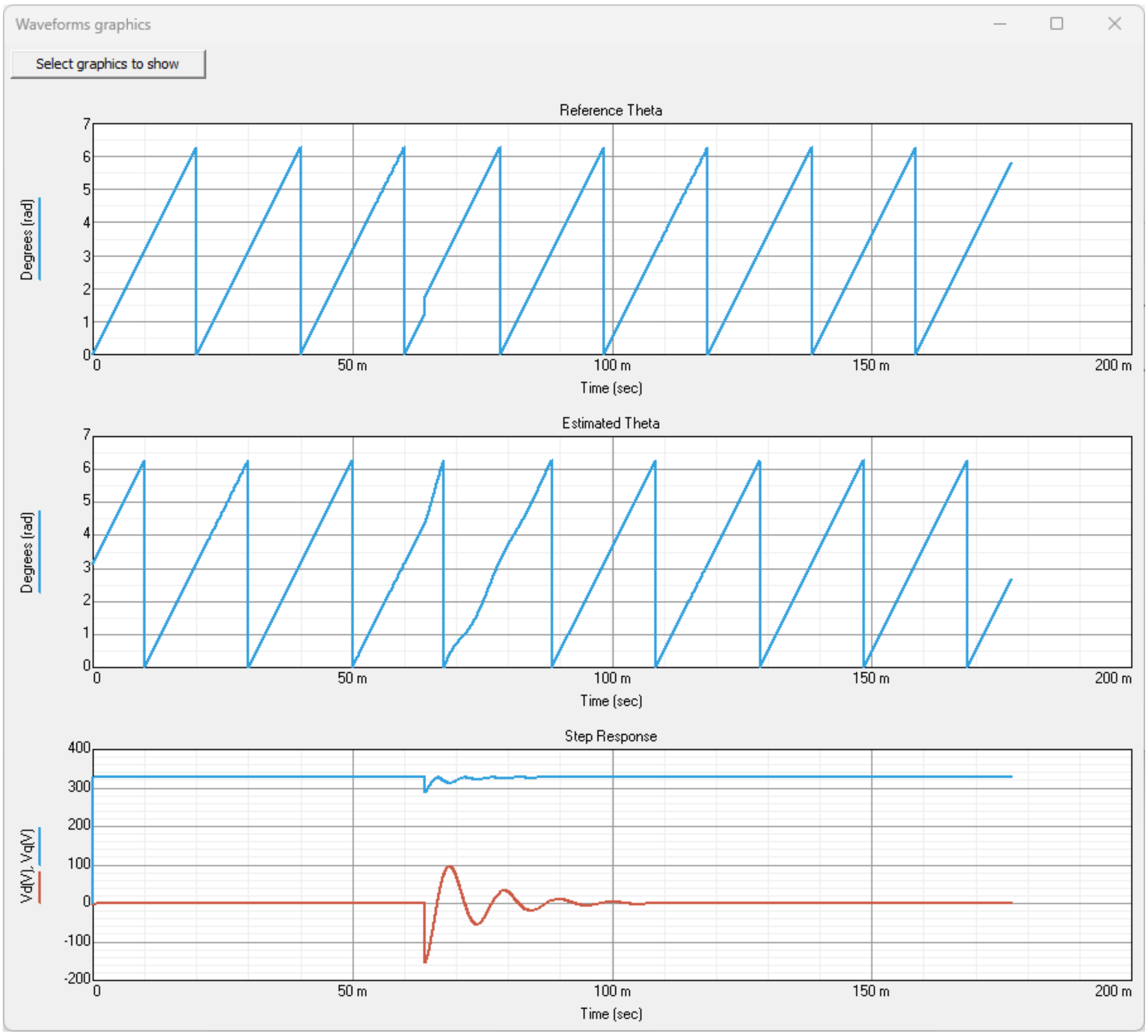
In the select option, the user can choose which waveform to display. This window allows to plot three waveforms.



Reference Theta: represents the phase of the grid in radians.

Estimated Theta: represents the phase that the PLL is able to follow.

Step Response: represents the transient response of the grid voltage in dq coordinate.



1.8.14.3 Schematic

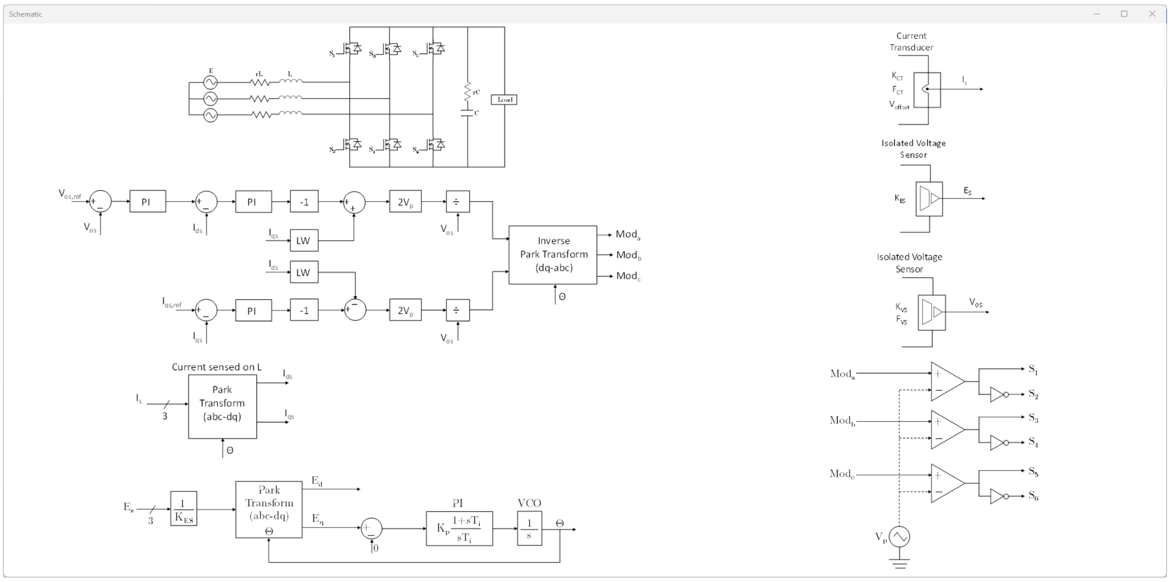
Navigation: SmartCtrl > Three-Phase PFC Boost Converter > Graphics >

Schematic

Previous Top Next

The schematic window shows a general overview of the topology, sensing chain, control structure and modulator selected by the user. This window is for information purposes only.

To call this window the user needs to click on the schematic icon  located in the menu bar.



1.8.14.4 EMI Filter Attenuation

Navigation: SmartCtrl > Three-Phase PFC Boost Converter > Graphics >

EMI Filter Attenuation

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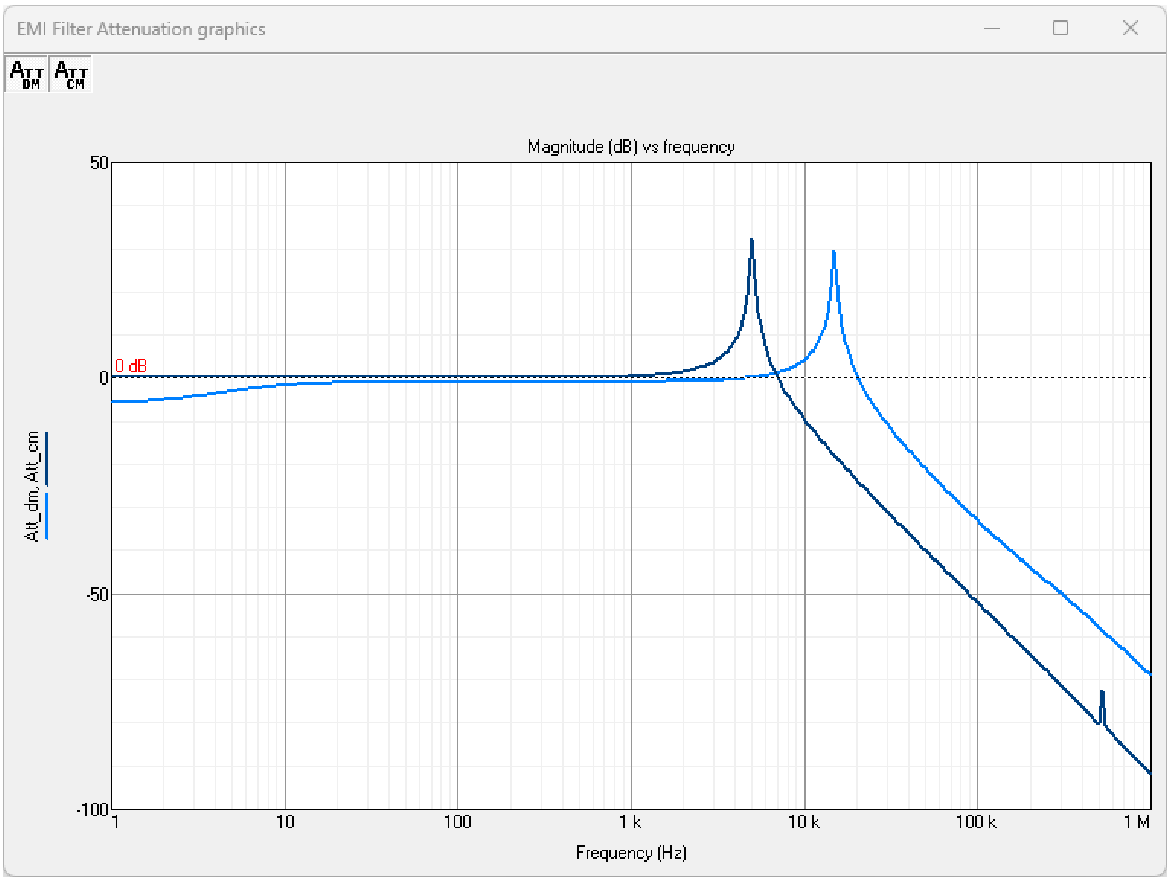
This window represents the frequency response of the equivalent transfer function of the EMI filter chosen in the Single-Line Diagram window. The attenuation is estimated on the 50 ohm resistance of the LISN. To see how the attenuation varies, the parameters in the EMI Filter window must be varied.

ATT_{DM} represents the attenuation of the differential mode filter.

ATT_{CM} represents the attenuation of the common mode filter.



1.9 Sensors

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Sensors Previous Top Next

1.9.1 Voltage divider

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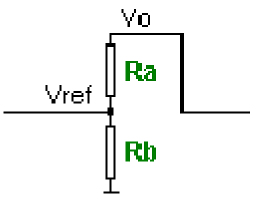
Voltage divider Previous Top Next



The **Voltage Divider** measures and adapts the output voltage level to the regulator voltage reference level.
Its transfer function corresponds to the following equation:

$$K(s) = \frac{V_{ref}}{V_O}$$

Where:

V_{ref} is the compensator reference voltage

V_o is the DC-DC converter output voltage

1.9.2 Embedded voltage divider

Navigation: SmartCtrl > Sensors >

Embedded voltage divider

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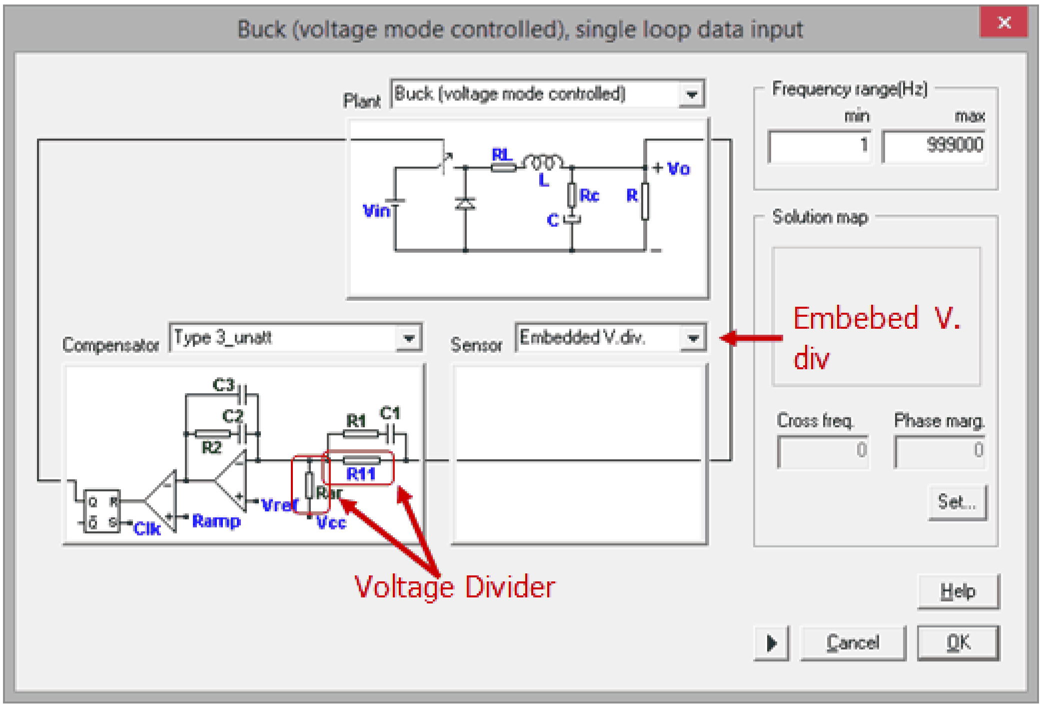
The two resistors that form the voltage divider **(R11,Rar) are embedded within the compensator**. So, no sensor is represented in the corresponding box. And the voltage divider resistors are highlighted in the compensator figure:



Given the desired output voltage, the compensator reference voltage and the value of R11, SmartCtrl calculates the resistor Rar. the transfer function of the voltage divider at 0Hz is the following:

$$\frac{V_o}{V_{ref}} = \frac{R_{ar}}{R_{ar} + R_{11}}$$

1.9.3 Isolated Voltage Sensor

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Isolated voltage sensor

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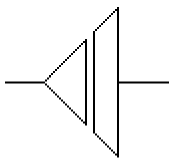
The **Isolated voltage sensor** is a voltage sensor that provides electrical isolation. Its transfer function is described below. It is available for the forward and the flyback DC-DC topologies.



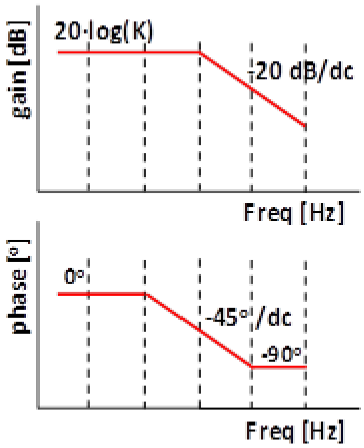
$$K(s) = \frac{Gain}{1 + \dfrac{s}{2 \cdot \pi \cdot fpK}}$$

Where:

Gain is the sensor gain at 0dB, its given by the output and the reference voltage.

Gain= Vo/Vref

fpK is the pole frequency in Hertz



1.9.4 Resistive Sensor (Power Factor Corrector)

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Resistive sensor (Power factor corrector)

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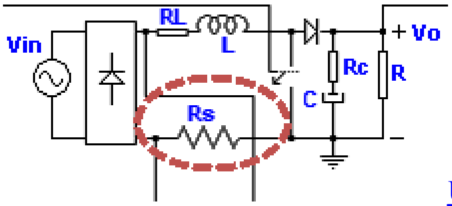
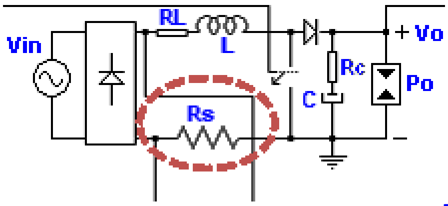
If the current is sensed using a resistor Rs, the current sensor gain will be the value of this resistor: Rs.

$K(s) = Rs$

This resistor is represented in the picture of the power plant, Rs:



UC3854A multiplier + Boost PFC (Resistive load)



UC3854A multiplier + Boost PFC (Constant power load)

1.9.5 Resistive Sensor (Peak Current Mode Control)

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Resistive Sensor (Peak Current Mode control)

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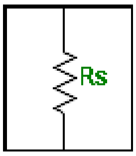

The resistor measures the inductor current and transforms the current into an equivalent voltage.
The sensor gain corresponds to its characteristic resistance value (Rs).

$$G = Rs$$

1.9.6 Hall effect sensor

Navigation: SmartCtrl > Sensors >

Hall effect sensor

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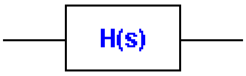
The **Hall effect** is a current sensor represented through a generic transfer function box. Internally, its transfer function corresponds to the following equation:

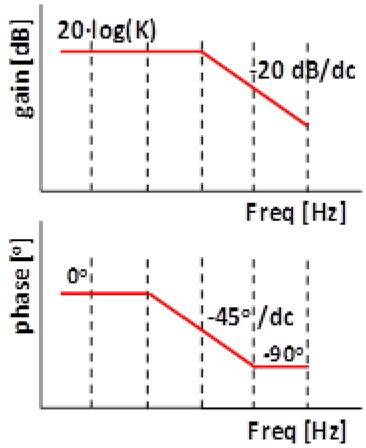


$$K(s) = \frac{Gain}{1 + \frac{s}{2 \cdot \pi \cdot fpK}}$$

Where:

Gain is the sensor gain at 0dB.

fpK is the pole frequency in Hertz



1.9.7 Current sensor

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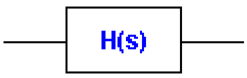
Current sensor [Previous](#) [Top](#) [Next](#)



The **current sensor** is represented by a generic transfer function box. Internally, the transfer function corresponds to a constant gain in V/A.

$$K(s) = Gain$$

For example, if the current is sensed using a resistor Rs, the current sensor gain will be the value of this resistor:

$$K(s) = Rs$$

1.9.8 User defined sensor

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User defined sensor [Previous](#) [Top](#) [Next](#)

When the user is designing a Generic Control System using the Equation Editor, for the sensor custom design details please go to [Sensor (equation editor)](#)

1.10 Modulator

1.10.1 Modulator (Peak Current Mode Control)

Navigation: SmartCtrl > Modulator >

Modulator (Peak Current Mode Control)

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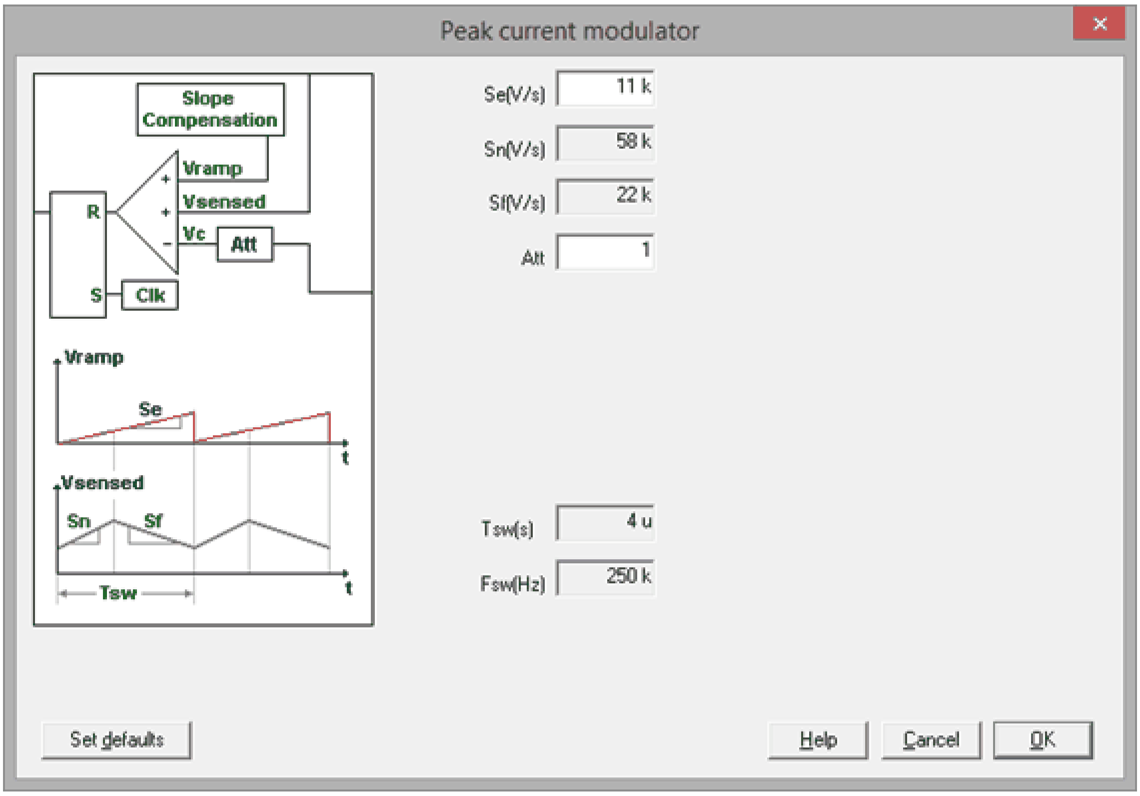
From top to bottom, the modulator input signals are defined as follows:

Vramp · Is the characteristic compensation slope used with this type of this control technique. This compensation slope is added to the sensed current in order to ensure the system stability with duty cycles above 50%.
Vsensed · Is the equivalent voltage of the sensed inductor current.
Vc · Is the sensed regulator output voltage.



From top to bottom, the modulator design criteria are defined as follow:

Sn · The inductor charge slope.
Sf · The inductor discharge slope.
Se · Is the slope of the compensation ramp, it is computed as function of Sn and S
Att · Is the attenuation applied to the regulator output voltage.

1.10.2 Modulator (PWM)

Navigation: SmartCtrl > Modulator >

Modulator (PWM)

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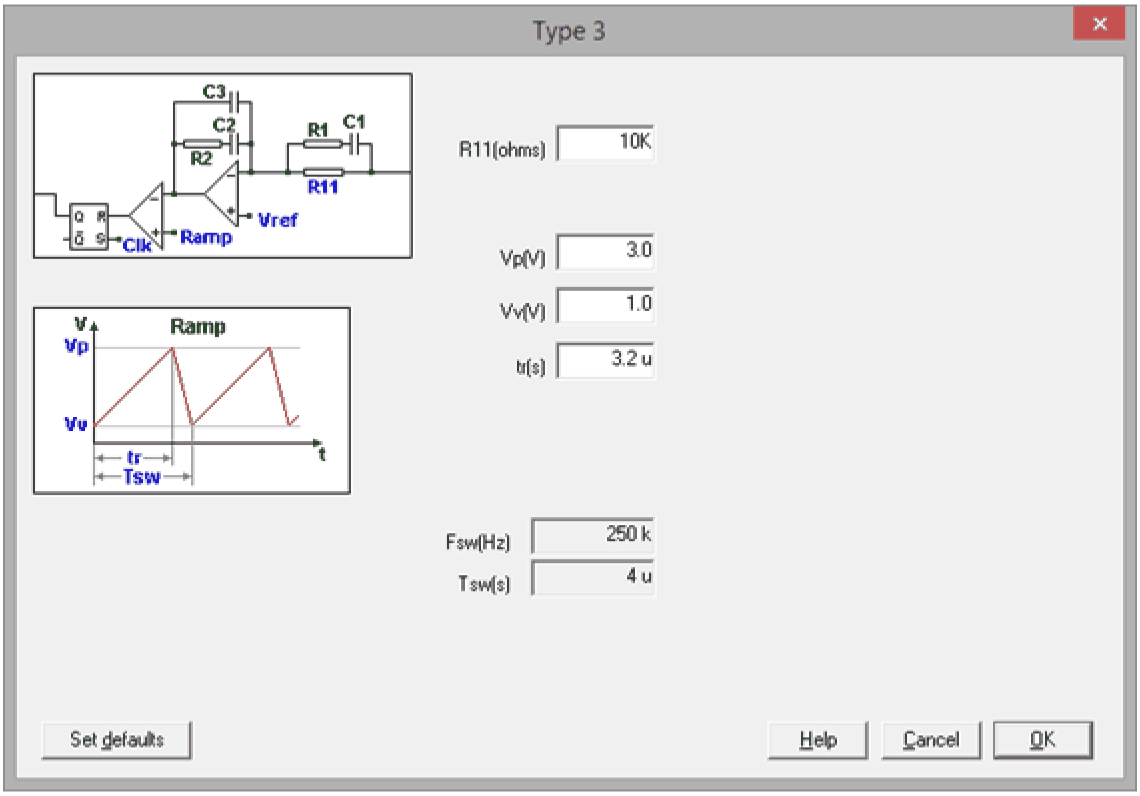
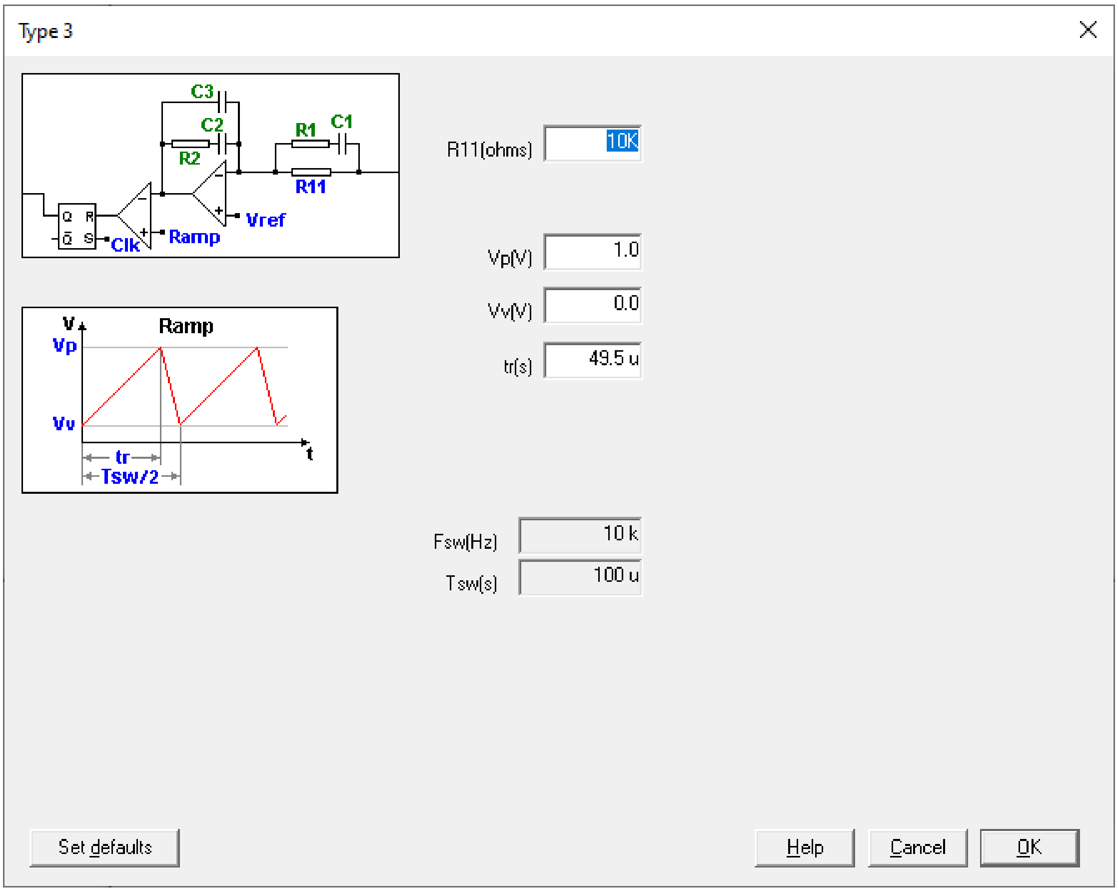
The **PWM modulator** can be displayed as part of the regulator, for the predefined topologies.



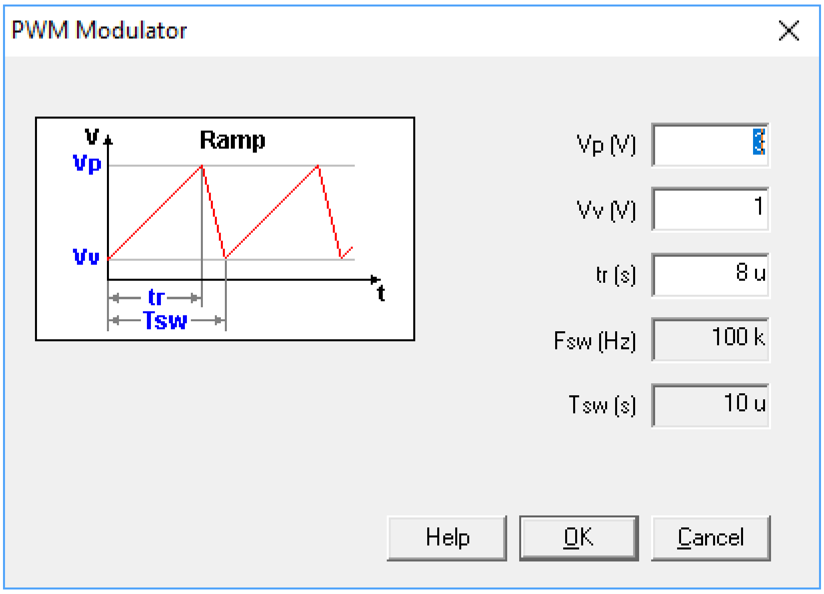
Signal Ramp is defined by:

- **Vp**, Peak voltage
- **Vv**, Valley voltage
- **tr**, Rising time
- **Fsw**, Switching frequency
- **Tsw**, Switching period



For the **Phase Shifted Full Bridge converter** please consider tthat the Signal Ramp period is Tsw/2.

When the user is designing a Generic Control System using the Equation Editor, for the compensator custom design the PWM modulator should be configured:



The values are:

Vp, Peak voltage
Vv, Valley voltage
tr, Rising time
Fsw, Switching frequency
Tsw, Switching period

1.10.3 User modulator

Navigation: SmartCtrl > Modulator >

User modulator

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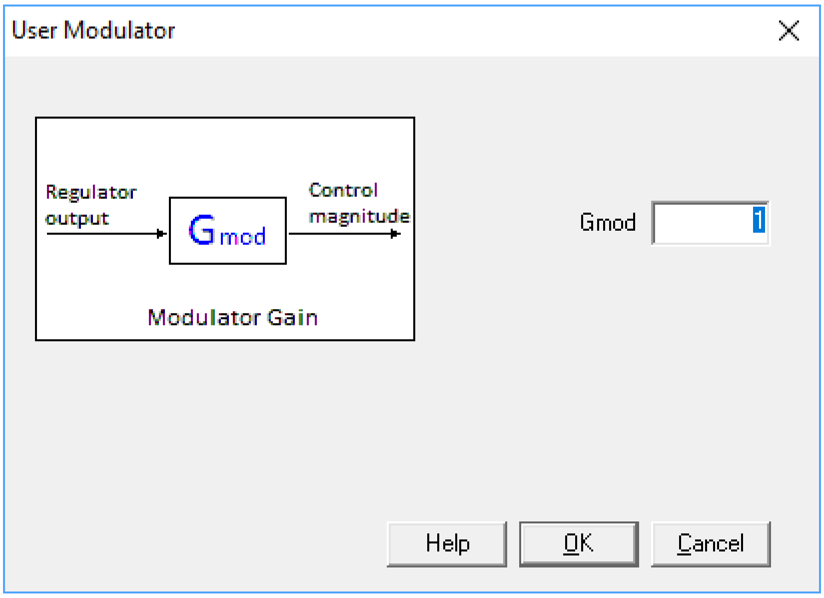
When the user is designing a Generic Control System using the Equation Editor, for the compensator custom design it is also possible to define a User Modulator:



The user should define the modulator desired gain.

1.11 Compensators

1.11.1 Analog compensators

Navigation: SmartCtrl > Compensators >

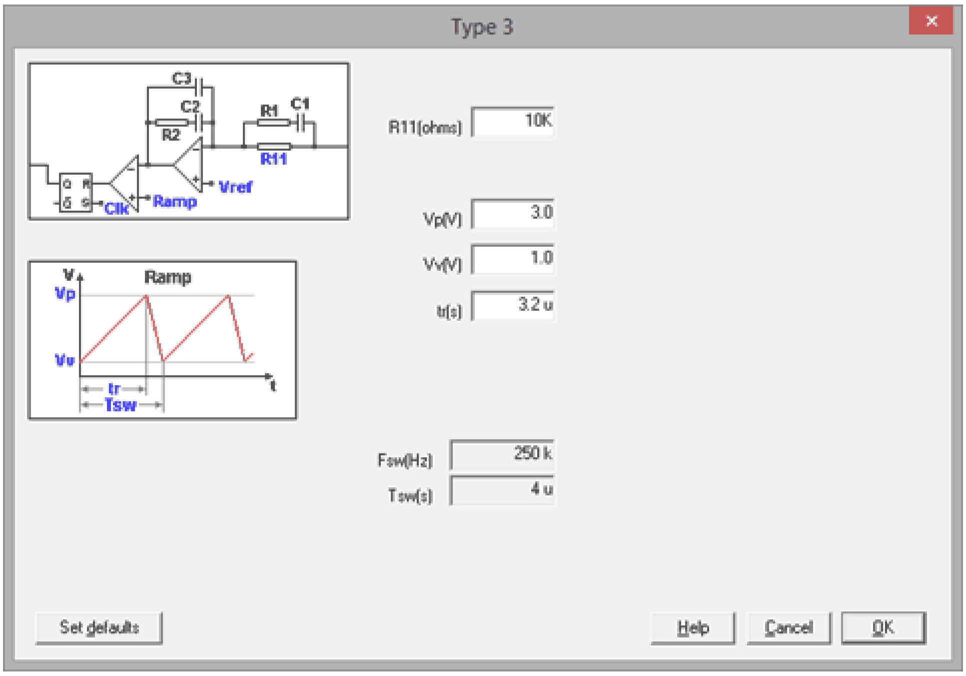
1.11.1.1 Single loop or inner loop

Type 3 compensator

Navigation: SmartCtrl > Compensators > Analog compensators > Single loop or inner loop >

Type 3 compensator Previous Top Next

Note that the PWM modulator design and parameters are included in this window.



Input Data

R11(ohms)	Its default value is 10 $k\Omega$
Vp(V)	Peak value of the ramp voltage (carrier signal of the **PWM modulator**)
Vv(V)	Valley value of the ramp voltage
Tr(s)	Rise time of the ramp voltage
Tsw(s)	Switching period

Output Data

The regulator components values (***C1, C2, C3, R1, R2***) are calculated by the program and displayed in the corresponding **text panel**

Type 3 compensator unattenuated

Navigation: SmartCtrl > Compensators > Analog compensators > Single loop or inner loop >

Type 3 compensator unattenuated

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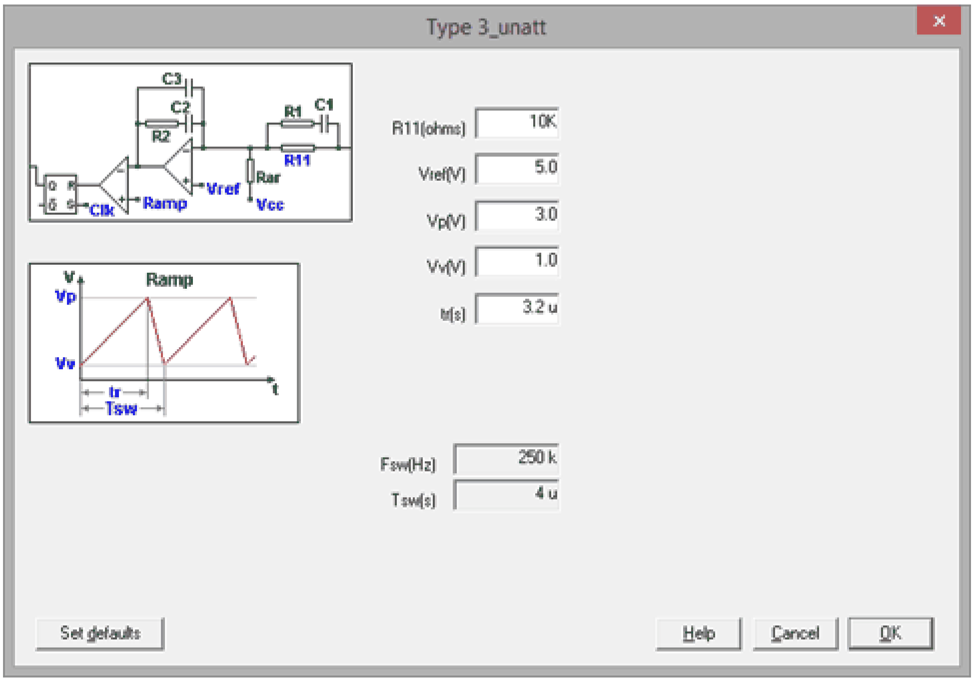
The voltage divider needed in order to adapt the sensed output voltage to the reference voltage is embedded within the compensator. It corresponds to R11 and Rar. This compensator configuration eliminates the attenuation due to the external voltage divider.

Note that the PWM modulator design and parameters are included in this window.



Input Data

R11(ohms)	Its default value is $10 k\Omega$
Vref(V)	Reference voltage
Vp(V)	Peak value of the ramp voltage (carrier signal of the **PWM modulator**)
Vv(V)	Valley value of the ramp voltage
Tr(s)	Rise time of the ramp voltage
Tsw(s)	Switching period

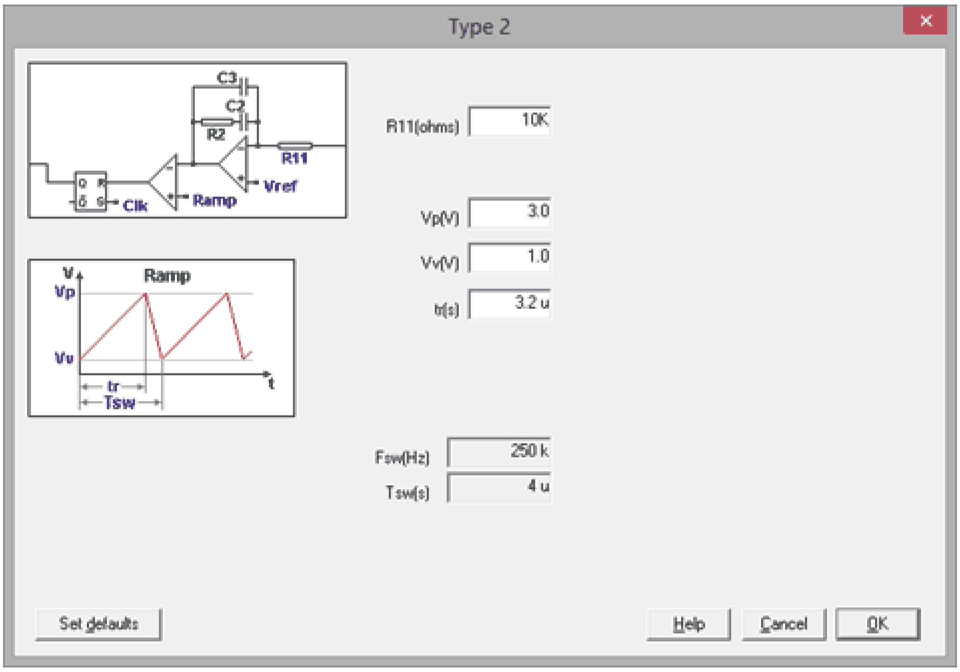
Output Data

The compensator components values (***C1, C2, C3, R1, R2***) and the resistor **R_{ar}** are calculated by the program and displayed in the corresponding **text panel**

Type 2 compensator

Type 2 compensator

Note that the PWM modulator design and parameters are included in this window.



Input Data

R11(ohms) Its default value is $10k\Omega$

Vp(V) Peak value of the ramp voltage (carrier signal of the **PWM modulator**)

Vv(V)	Valley value of the ramp voltage
Tr(s)	Rise time of the ramp voltage
Tsw(s)	Switching period

Output Data

The compensator components values (***C2, C3, R2***) are calculated by the program and displayed in the corresponding **text panel**

Type 2 compensator unattenuated

Navigation: SmartCtrl > Compensators > Analog compensators > Single loop or inner loop >

Type 2 compensator unattenuated

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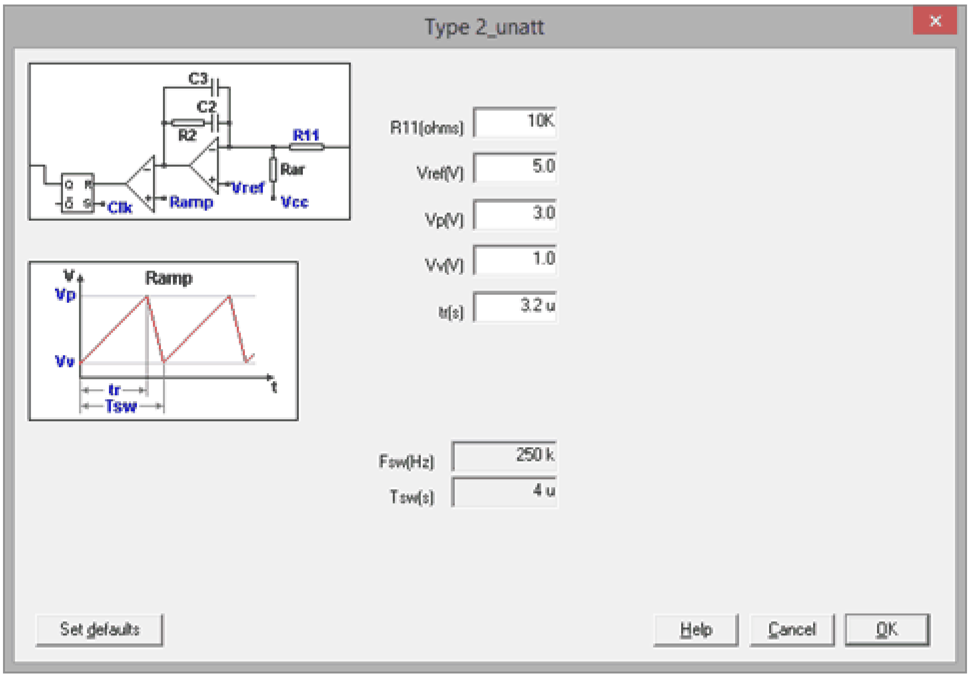
The voltage divider needed in order to adapt the sensed output voltage to the reference voltage is embedded within the compensator. It corresponds to R11 and Rar. This compensator configuration eliminates the attenuation due to the external voltage divider.

Note that the PWM modulator design and parameters are included in this window.



Input Data

R11(ohms)	Its default value is 10 $k\Omega$
Vref(V)	Reference voltage
Vp(V)	Peak value of the ramp voltage (carrier signal of the **PWM modulator**)
Vv(V)	Valley value of the ramp voltage
Tr(s)	Rise time of the ramp voltage
Tsw(s)	Switching period

Output Data

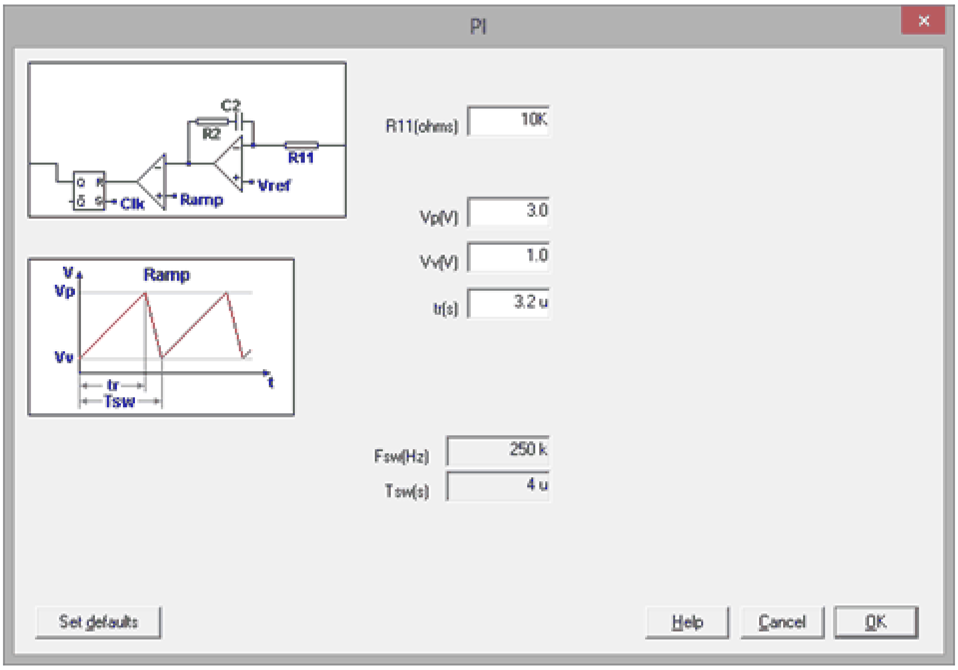
The compensator components values (***C1, C2, C3, R1, R2***) and the resistor **R_{ar}** are calculated by the program and displayed in the corresponding **text panel**

PI analog compensator

Navigation: SmartCtrl > Compensators > Analog compensators > Single loop or inner loop >

PI analog compensator

Note that the PWM modulator design and parameters are included in this window.



Input Data

R11(ohms)	Its default value is 10 $k\Omega$
Vp(V)	Peak value of the ramp voltage (carrier signal of the **PWM modulator**)
Vv(V)	Valley value of the ramp voltage
Tr(s)	Rise time of the ramp voltage
Tsw(s)	Switching period

Output Data

The compensator components values (***C2, R2***) are calculated by the program and displayed in the corresponding **text panel**

PI compensator

Navigation: SmartCtrl > Compensators > Analog compensators > Single loop or inner loop >

PI compensator

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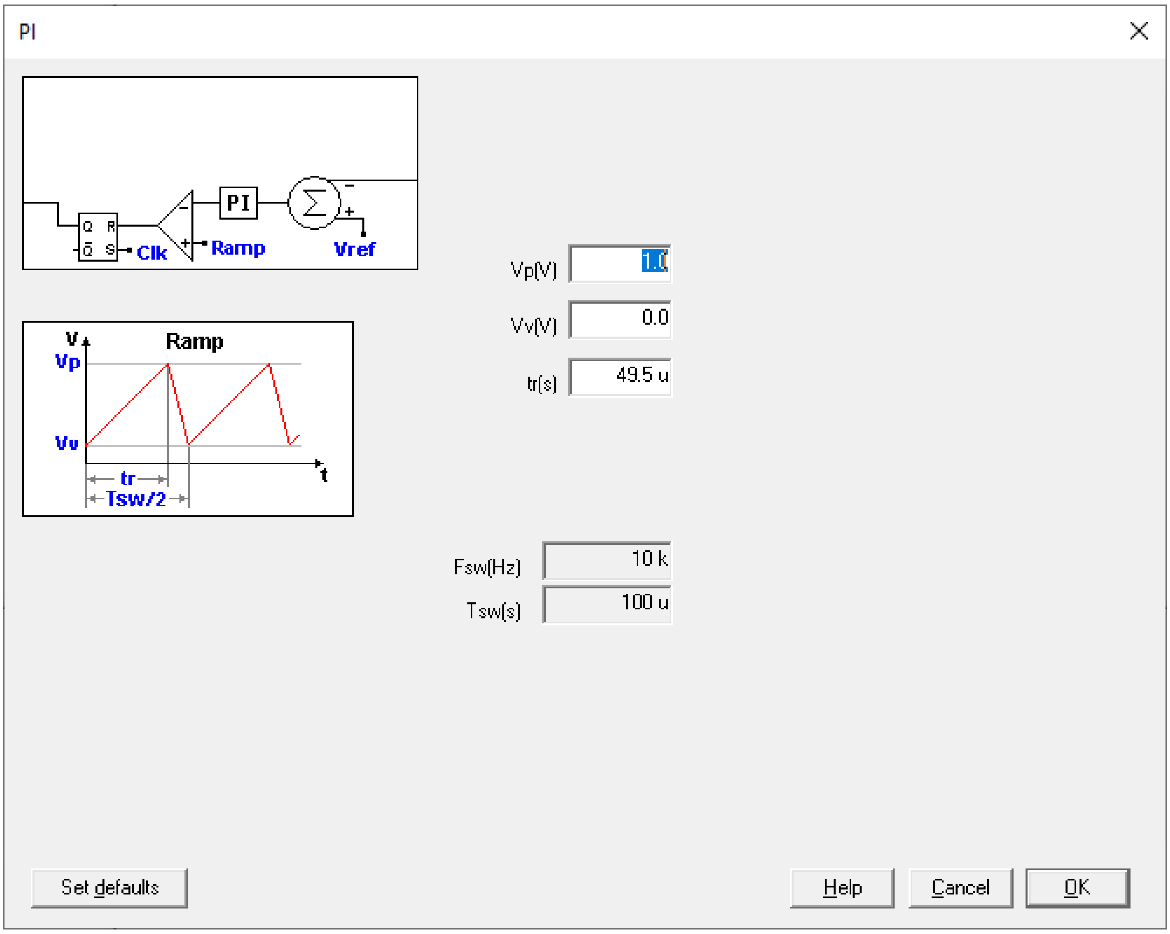
Note that the PWM modulator design and parameters are included in this window.



Input Data

Vp(V)	Peak value of the ramp voltage (carrier signal of the **PWM modulator**)
Vv(V)	Valley value of the ramp voltage
tr(s)	Rise time of the ramp voltage

Tsw(s) Switching period

Output Data

Considering the PI compensator transfer function:

$$Kp\,\frac{(1 + s\,Ti)}{s\,Ti}$$

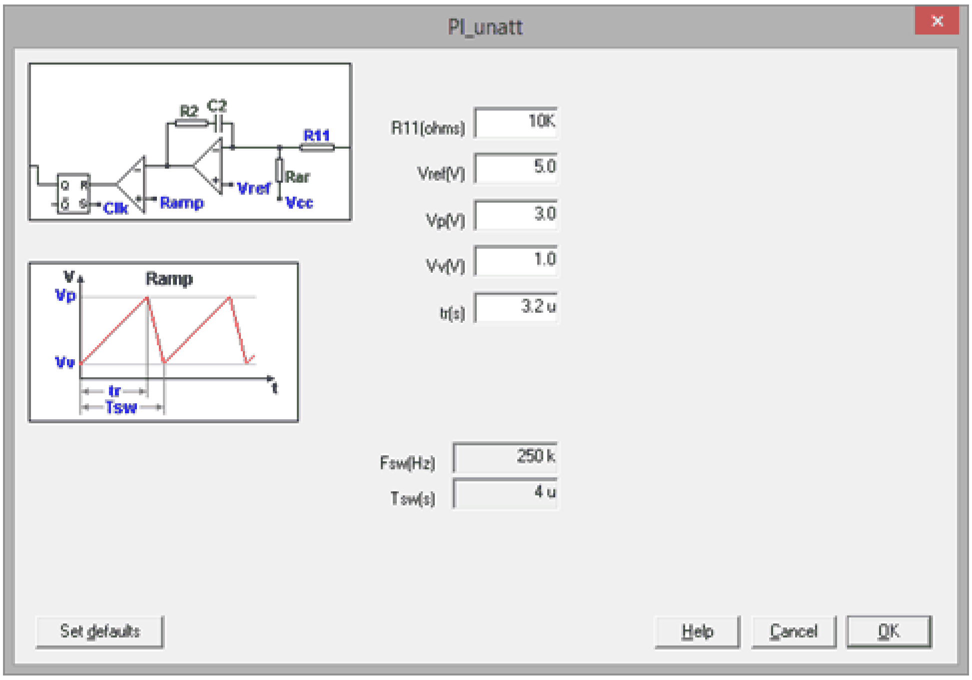
The compensator values (***Kp, Ti(s)***) are calculated by the program and displayed in the corresponding **text panel**

PI compensator unattenuated

PI compensator unattenuated

The voltage divider needed in order to adapt the sensed output voltage to the reference voltage is embedded within the compensator. It corresponds to R11 and Rar. This compensator configuration eliminates the attenuation due to the external voltage divider.

Note that the PWM modulator design and parameters are included in this window.



Input Data

R11(ohms)	Its default value is 10$k\Omega$
Vref(V)	Reference voltage
Vp(V)	Peak value of the ramp voltage (carrier signal of the PWM modulator)
Vv(V)	Valley value of the ramp voltage
Tr(V)	Rise time of the ramp voltage
Tsw(s)	Switching period

Output Data

The compensator components values (**C2, R2**) and the resistor R_{ar} are calculated by the program and displayed in the corresponding **text panel**.

1.11.1.2 Outer Loop and Peak Current Mode Control

Single Pole compensator

Navigation: SmartCtrl > Compensators > Analog compensators > Outer Loop and Peak Current Mode Control >

Single Pole compensator

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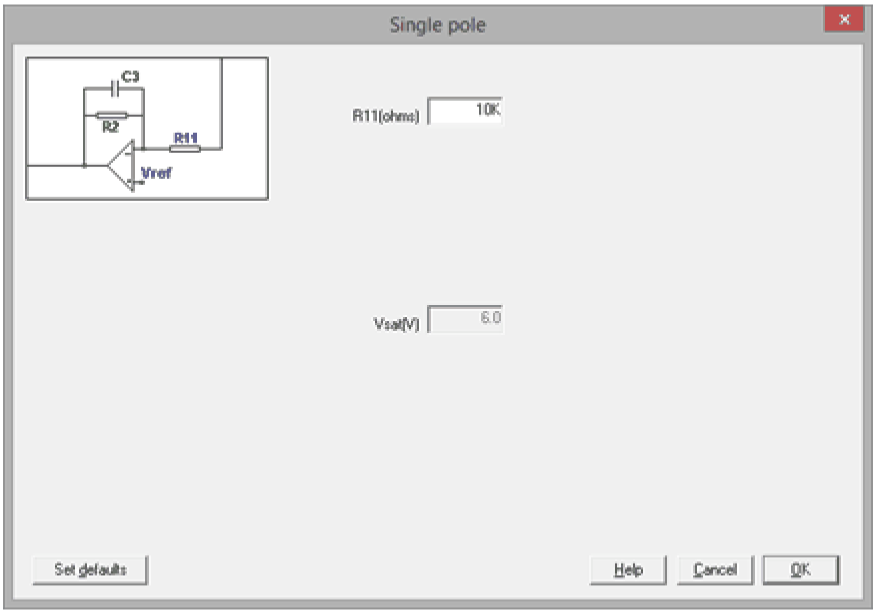

Input Data

R11	Its default value is 10 $k\Omega$
Vsat	Saturation voltage of the op-amp. In the case of the power factor corrector using a UC3854A multiplier, this value is equal to 6.0 V

Output Data

The compensator components values (***C3*** and ***R2***) is calculated by the program and displayed in the corresponding **text panel**

Single Pole unattenuated

Navigation: SmartCtrl > Compensators > Analog compensators > Outer Loop and Peak Current Mode Control >

Single Pole regulator unattenuated

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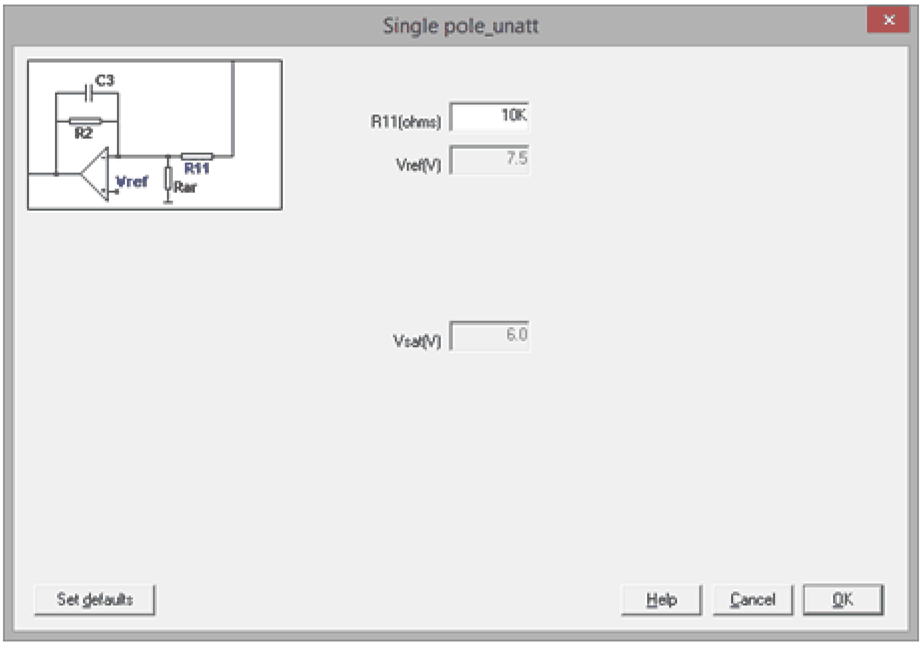
The voltage divider needed in order to adapt the sensed output voltage to the reference voltage is embedded within the compensator. It corresponds to R11 and Rar. This compensator configuration eliminates the attenuation due to the external voltage divider.



Input Data

R11	Its default value is 10$k\Omega$
Vref	Reference voltage. In the case of the power factor corrector using a UC3854A multiplier, this value is equal to 7.5 V
Vsat	Saturation voltage of the op-amp. In the case of the power factor corrector using a UC3854A multiplier, this value is equal to 6.0 V

Output Data

The compensator component value (***C3*** and ***R2***) and the resistor **R_{ar}** are calculated by the program and displayed in the corresponding **text panel**

Type 3 compensator

Navigation: SmartCtrl > Compensators > Analog compensators > Outer Loop and Peak Current Mode Control >

Type 3 compensator

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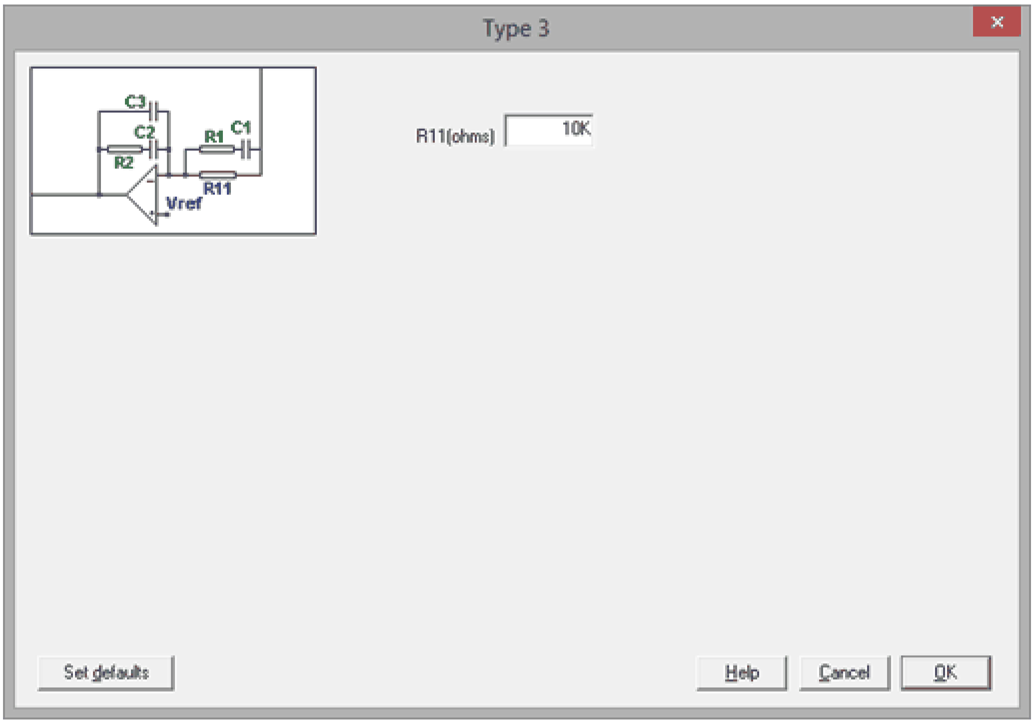


Input Data

R11(ohms)	Its default value is 10 $k\Omega$

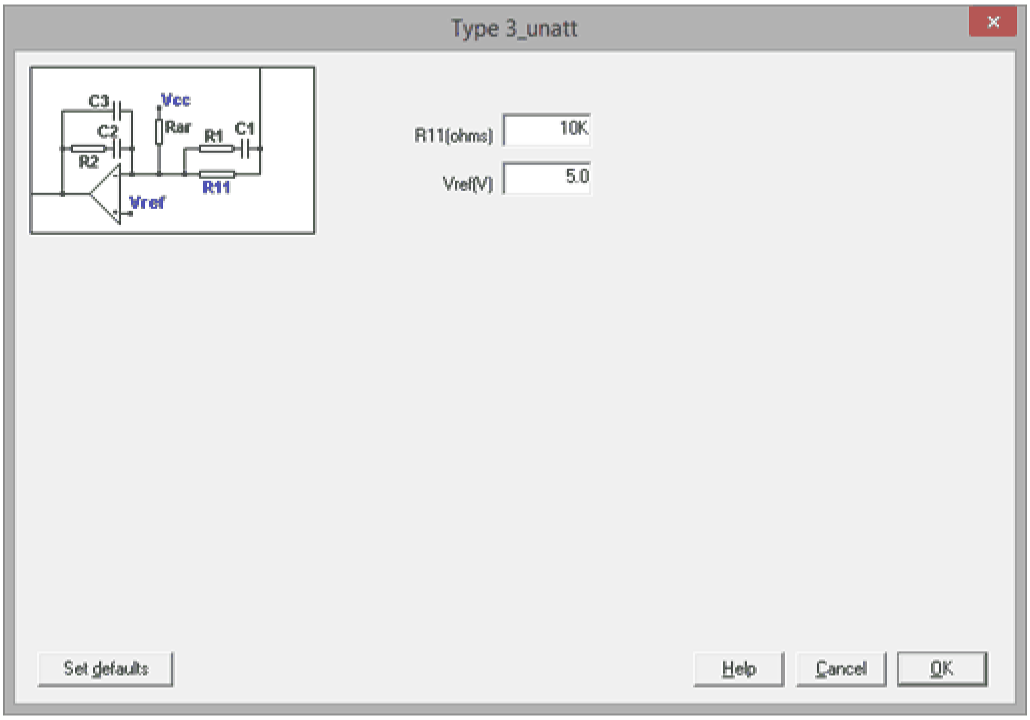
Output Data

The compensator components values (***C1, C2, C3, R1, R2***) are calculated by the program and displayed in the corresponding **text panel**

Type 3 compensator unattenuated

Type 3 compensator unattenuated

The voltage divider needed in order to adapt the sensed output voltage to the reference voltage is embedded within the compensator. It corresponds to R11 and Rar. This compensator configuration eliminates the attenuation due to the external voltage divider.



Input Data

R11(ohms)	Its default value is 10 $k\Omega$
Vref(V)	Reference voltage

Output Data

The compensator components values (***C1, C2, C3, R1, R2***) are calculated by the program and displayed in the corresponding text panel

Type 2 compensator

Navigation: SmartCtrl > Compensators > Analog compensators > Outer Loop and Peak Current Mode Control >

Type 2 compensator

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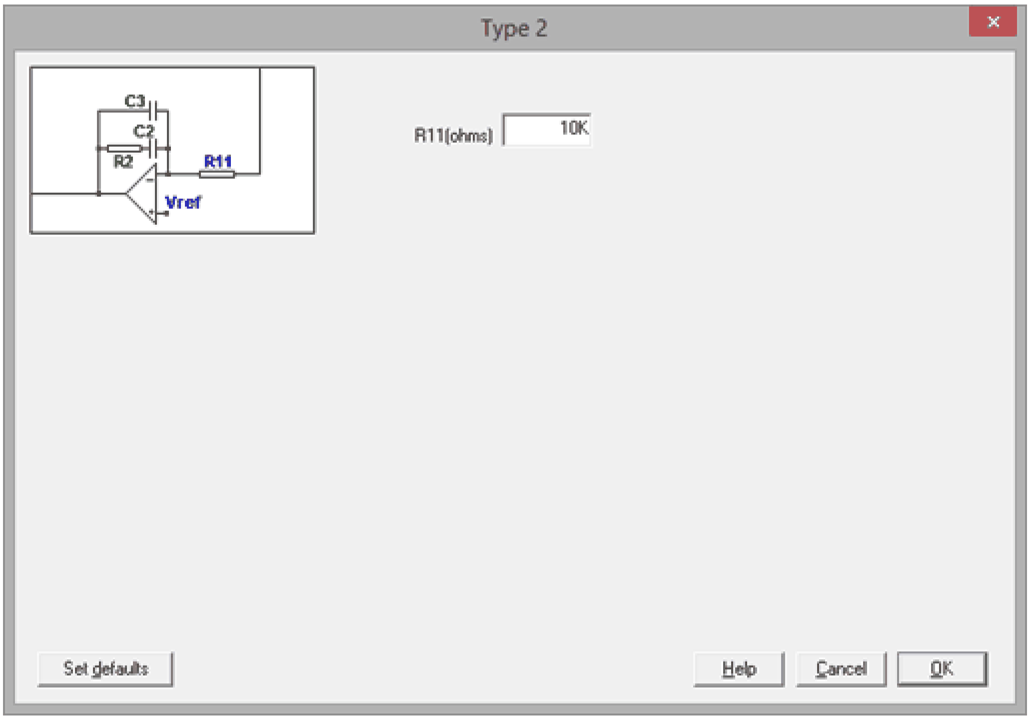

Input Data

R11(ohms) Its default value is 10 $k\Omega$

Output Data

The compensator components values (***C2, C3, R2***) are calculated by the program and displayed in the corresponding text panel

Type 2 compensator unattenuated

Navigation: SmartCtrl > Compensators > Analog compensators > Outer Loop and Peak Current Mode Control >

Type 2 compensator unattenuated

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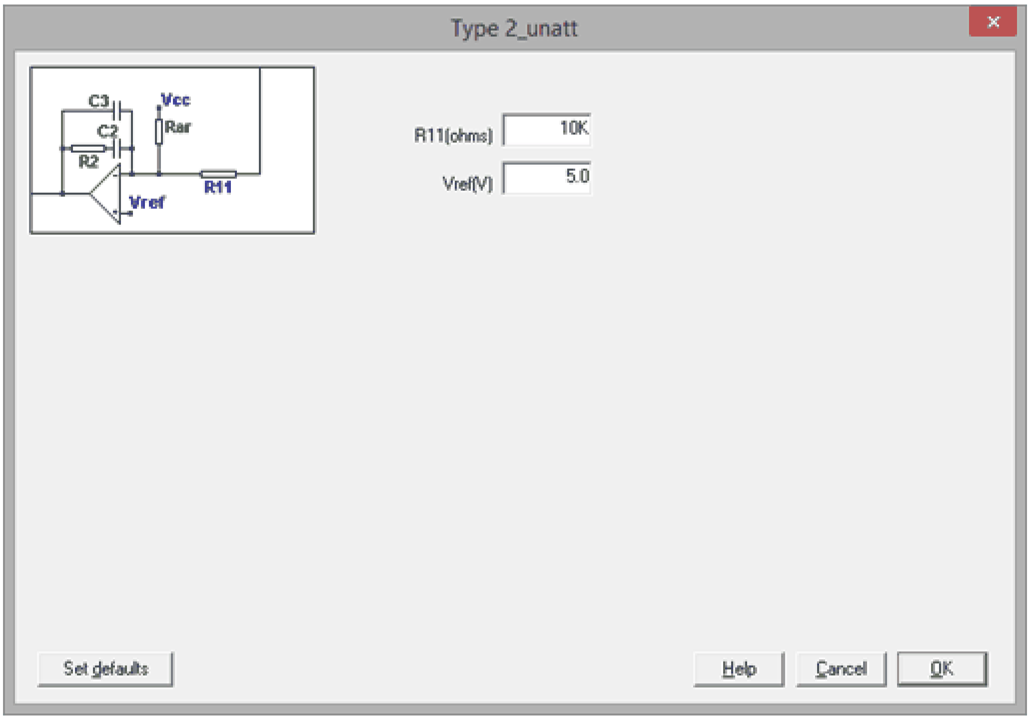
The voltage divider needed in order to adapt the sensed output voltage to the reference voltage is embedded within the compensator. It corresponds to R11 and Rar. This compensator configuration eliminates the attenuation due to the external voltage divider.



Input Data

R11(ohms)	Its default value is $10 k\Omega$
Vref(V)	Reference voltage

Output Data

The compensator components values (***C1, C2, C3, R1, R2***) and the resistance $\mathbf{R_{ar}}$ are calculated by the program and displayed in the corresponding text panel

PI analog compensator

Navigation: SmartCtrl > Compensators > Analog compensators > Outer Loop and Peak Current Mode Control >

PI analog compensator

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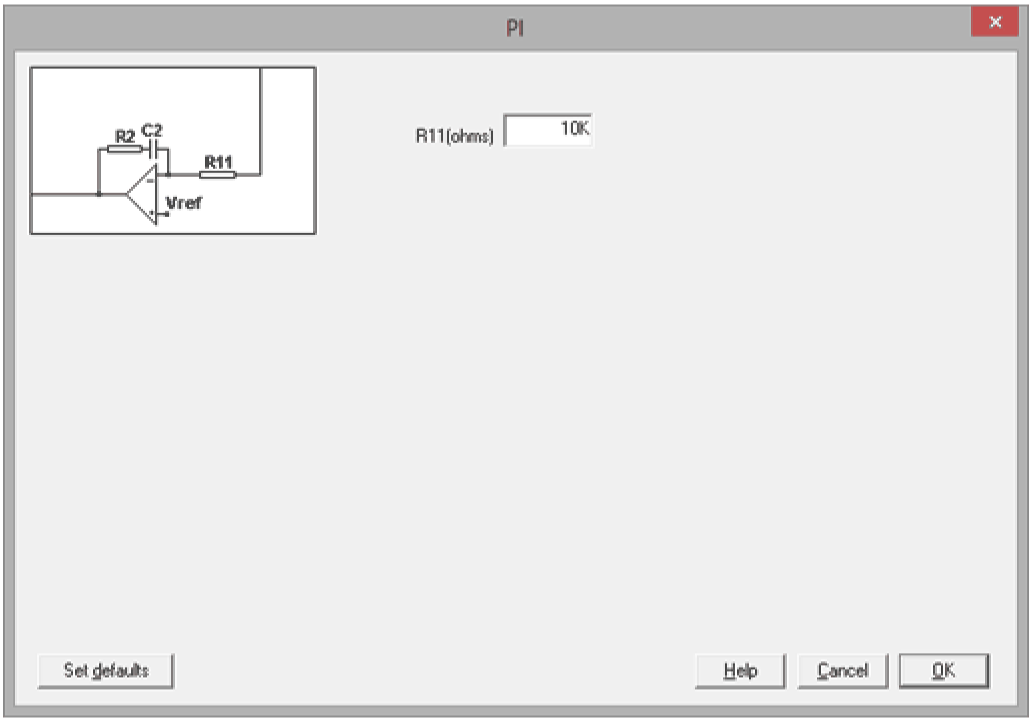

Input Data

R11(ohms) Its default value is 10 $k\Omega$

Output Data

The compensator components values (***C2, R2***) are calculated by the program and displayed in the corresponding text panel

PI compensator

Navigation: SmartCtrl > Compensators > Analog compensators > Outer Loop and Peak Current Mode Control >

PI compensator

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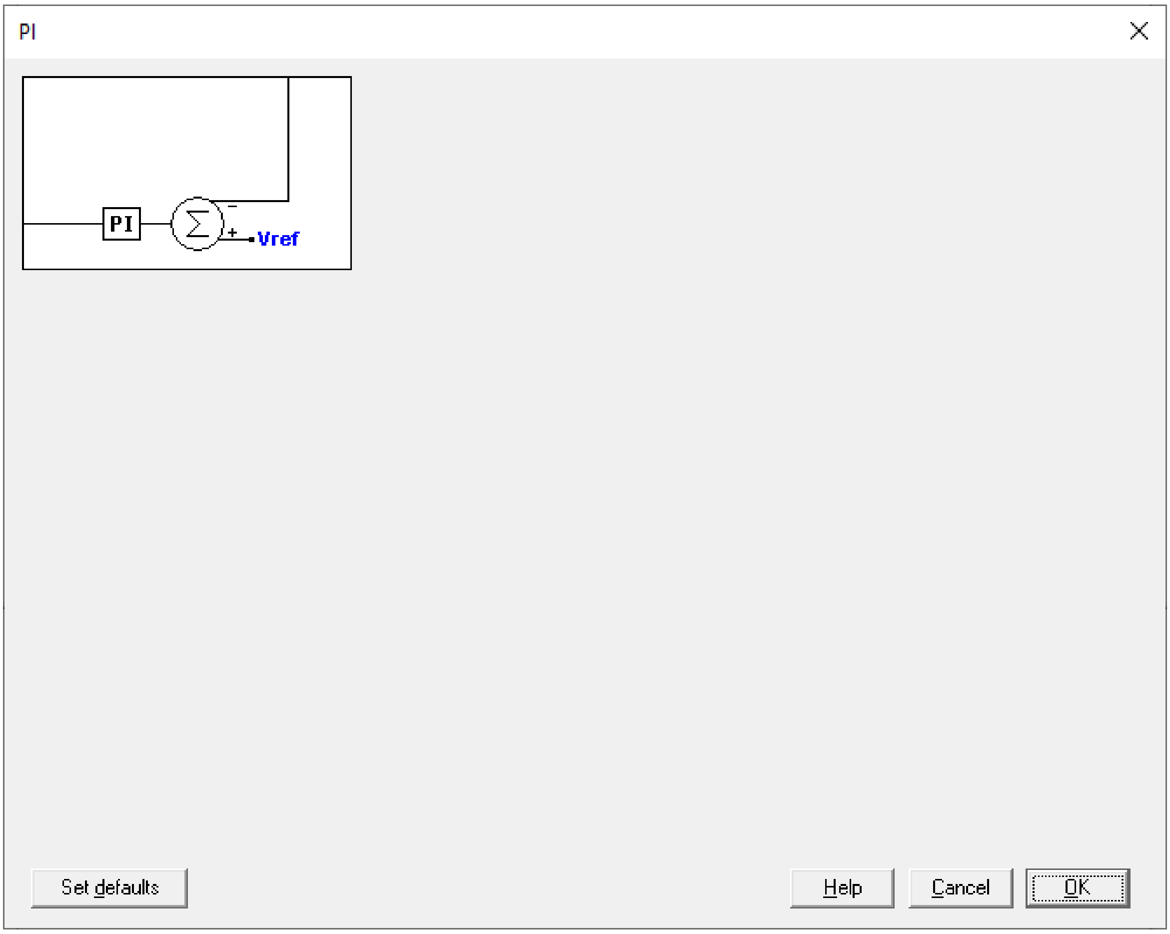
The PI compensator values are calculated using the following transfer function:

$$Kp\,\frac{(1+s\,Ti)}{s\,Ti}$$



Output Data

The compensator values (***Kp, Ti(s)***) are calculated by the program and displayed in the corresponding text panel

PI compensator unattenuated

Navigation: SmartCtrl > Compensators > Analog compensators > Outer Loop and Peak Current Mode Control >

PI compensator unattenuated

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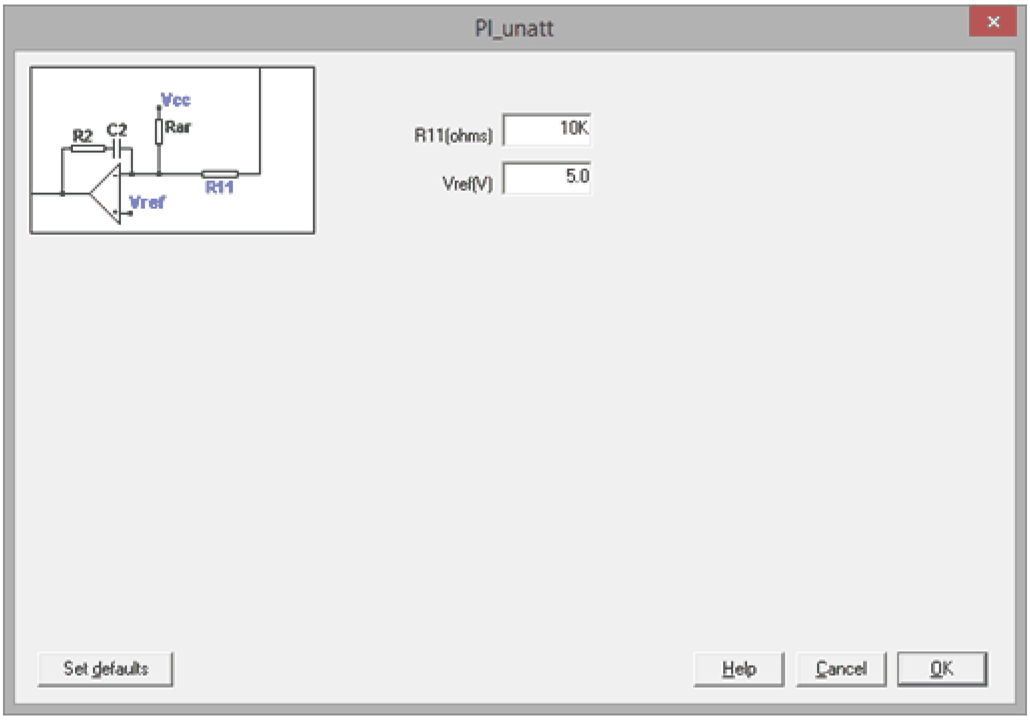
The voltage divider needed in order to adapt the sensed output voltage to the reference voltage is embedded within the regulator. It corresponds to R11 and Rar. This regulator configuration eliminates the attenuation due to the external voltage divider.



Input Data

R11(ohms)	Its default value is 10 $k\Omega$
Vref(V)	Reference voltage

Output Data

The compensator components values (**C2, R2**) and the resistor R_{ar} are calculated by the program and displayed in the corresponding text panel.

1.11.2 Digital compensators

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Digital compensators

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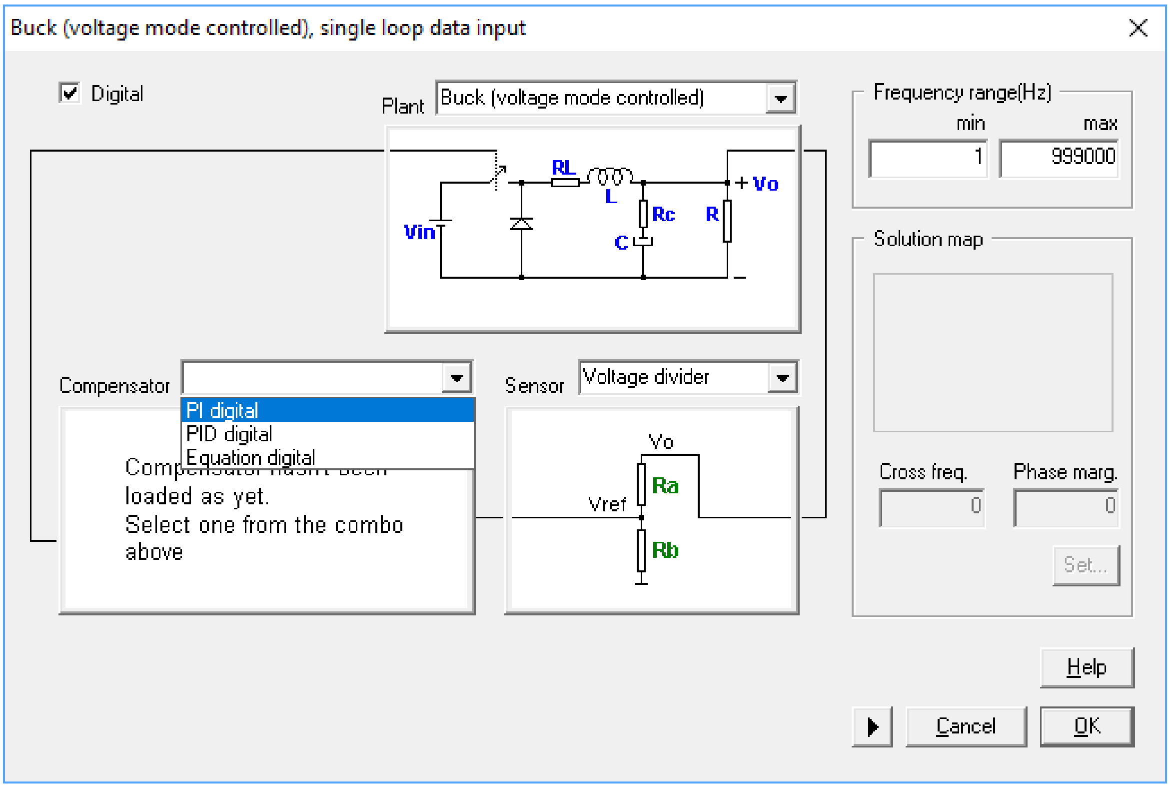
Digital compensators are obtained directly in z-domain, calculating the coefficients in order to be implemented by means of digital devices (as specific hardware in FPGA or ASIC, or as a program in a microprocessor, microcontroller or DSP), and can be exported to PSIM using z-domain blocks.

If the user is going to define a digital control it is necessary to click on the the Digital selection check box. This option should be selected since the beginning because it determines the different options that can be selected further on, in the sensor and in the compensator.



More information about Digital Control: Digital Control.

1.11.2.1 PI Digital

Navigation: SmartCtrl > Compensators > Digital compensators >

PI Digital

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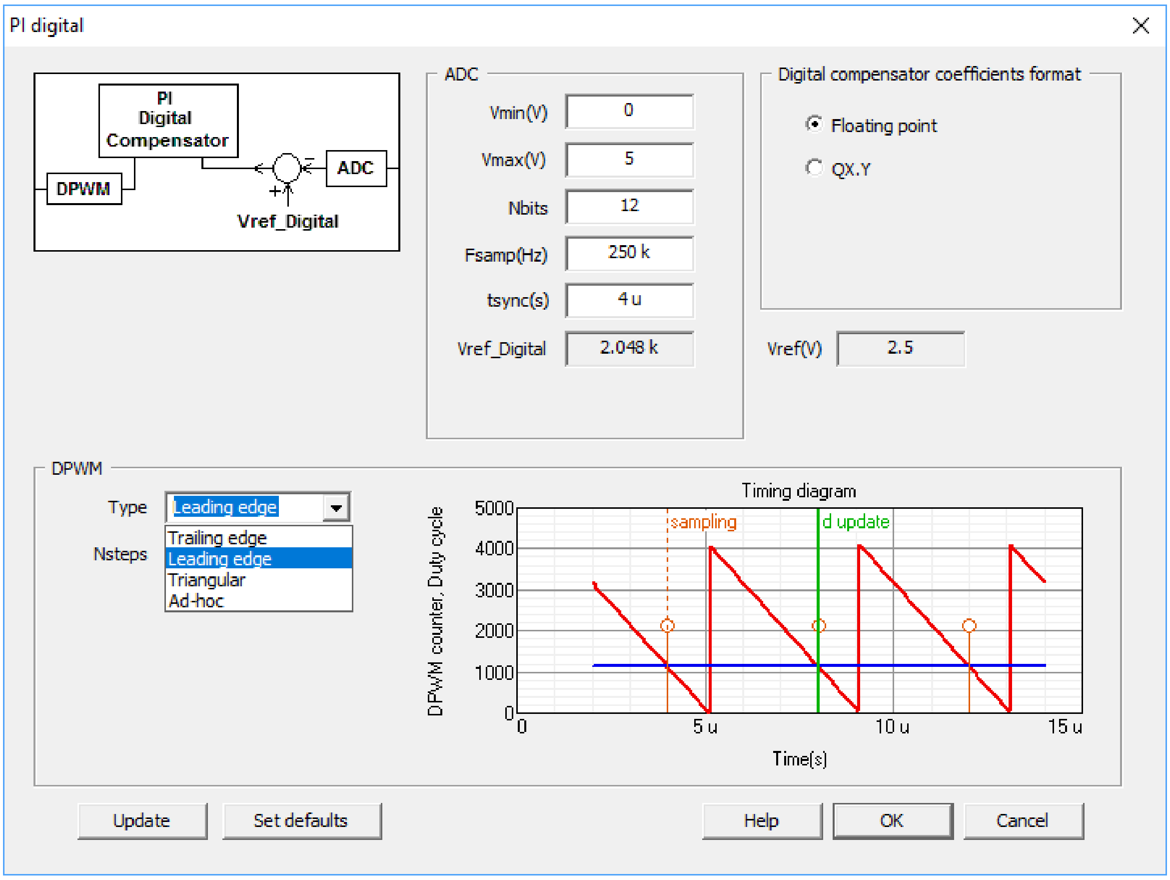
SmartCtrl takes into account some specifications regarding both the controller and the ADC, which are explained below.



ADC panel:

•**Vmin(V):** minimum voltage the ADC is able to read, used to calculate its gain.

•**Vmax(V):** maximum voltage the ADC is able to read, used to calculate its gain.

•**Nbits:** Number of bits of the ADC to represent the analog input value. This number affects the calculation of the reference, as stated below.

•**Fsamp(Hz):** Sampling frequency of the digital regulator. The sampling period Tsamp=1/fsamp is the time between two consecutive samples of the output signal of the regulator.

In many applications, the sampling frequency (fsamp) of the regulator is equal to the switching frequency (fsw) of the power converter. In SmartCtrl, the user can select different values for switching and sampling frequency, but **the sampling frequency must be a multiple or submultiple of the switching frequency**.

In current loops, the controlled magnitude in the converter has a significant ripple, therefore, it is recommended to use a Hall Effect sensor that includes a first order low pass filter that can act as an antialiasing filter.

•**Vref_Digital:** Value of the reference to be followed by the digital compensator, calculated as:

$$V_{ref_{Digital}} = (ValueToBeSensed \cdot SensorGain - V_{ADCmin}) \cdot \frac{2^{NbitsADC}}{V_{ADCmax} - V_{ADCmin}}$$

•**tsync(s):** it accounts for the time difference between the moment when a signal is sampled and when it is used to update the regulator output.

Unlike in an analog controller, where the sensor is continuously measuring and the control signal is updated at every moment, when a digital compensator is implemented, the instant when a signal is measured and the instant when a change is seen by the PWM signal are not the same.

Digital compensator coefficients format:

•**Floating point:** According to the international standard ISO/IEC/IEEE 60559:2011 (with content identical to IEEE 754-2008).

•**QX.Y:** Fixed point number is represented with the QX.Y notation, X + Y bits, with X bits to the left of the fixed point (integer part, sign bit included) and Y bits after the point (fractional part).

DPWM

For the modulator there are different options according to the waveform:

•Trailing Edge

•Leading Edge

•Triangular

•Ad-hoc, defining Gmod and tdelay(s).

More information about Digital Control: Digital Control.

1.11.2.2 PID Digital

Navigation: SmartCtrl > Compensators > Digital compensators >

PID Digital

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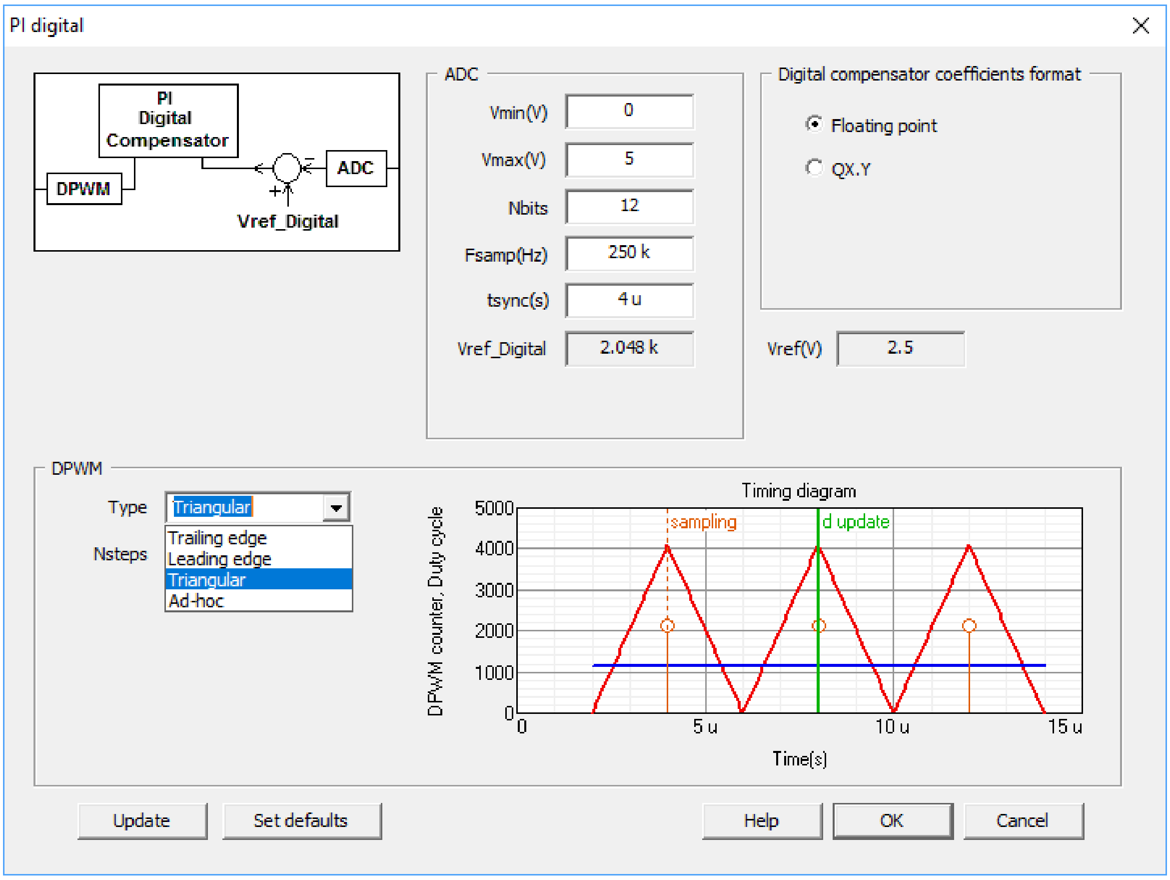
SmartCtrl takes into account some specifications regarding both the controller and the ADC, which are explained below.



ADC panel:

•**Vmin(V):** minimum voltage the ADC is able to read, used to calculate its gain.

•**Vmax(V):** maximum voltage the ADC is able to read, used to calculate its gain.

•**Nbits:** Number of bits of the ADC to represent the analog input value. This number affects the calculation of the reference, as stated below.

•**Fsamp(Hz):** Sampling frequency of the digital regulator. The sampling period Tsamp=1/fsamp is the time between two consecutive samples of the output signal of the regulator.

In many applications, the sampling frequency (fsamp) of the regulator is equal to the switching frequency (fsw) of the power converter. In SmartCtrl, the user can select different values for switching and sampling frequency, but **the sampling frequency must be a multiple or submultiple of the switching frequency**.

In current loops, the controlled magnitude in the converter has a significant ripple, therefore, it is recommended to use a Hall Effect sensor that includes a first order low pass filter that can act as an antialiasing filter.

•**Vref_Digital:** Value of the reference to be followed by the digital compensator, calculated as:

$$V_{ref_{Digital}} = (ValueToBeSensed \cdot SensorGain - V_{ADCmin}) \cdot \frac{2^{NbitsADC}}{V_{ADCmax} - V_{ADCmin}}$$

•**tsync(s):** it accounts for the time difference between the moment when a signal is sampled and when it is used to update the regulator output.

Unlike in an analog controller, where the sensor is continuously measuring and the control signal is updated at every moment, when a digital compensator is implemented, the instant when a signal is measured and the instant when a change is seen by the PWM signal are not the same.

Digital compensator coefficients format:

•**Floating point:** According to the international standard ISO/IEC/IEEE 60559:2011 (with content identical to IEEE 754-2008).

•**QX.Y:** Fixed point number is represented with the QX.Y notation, X + Y bits, with X bits to the left of the fixed point (integer part, sign bit included) and Y bits after the point (fractional part).

DPWM

For the modulator there are different options according to the waveform:

- Trailing Edge
- Leading Edge
- Triangular
- Ad-hoc, defining Gmod and tdelay(s).

More information about Digital Control: Digital Control.

1.11.3 User defined compensator

Navigation: SmartCtrl > Compensators >

User defined compensator

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When the user is designing a Generic Control System using the Equation Editor, for the compensator custom design details please go to Compensator (equation editor)

1.12 Graphic and text panels

Navigation: SmartCtrl >

Graphic and text panels

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The window is divided in six different panels.

The graphic panels are:

Bode plot Magnitude (dB)
Bode plot Phase (º)

[Nyquist diagram](#)
[Transient response plot](#)
[Steady State waveforms (temporal domain)](#)

There are also two text panels that are hidden till user press the corresponding bottom, these are:

Input data
Output data

1.12.1 Bode plots

Navigation: SmartCtrl > Graphic and text panels >

Bode plots

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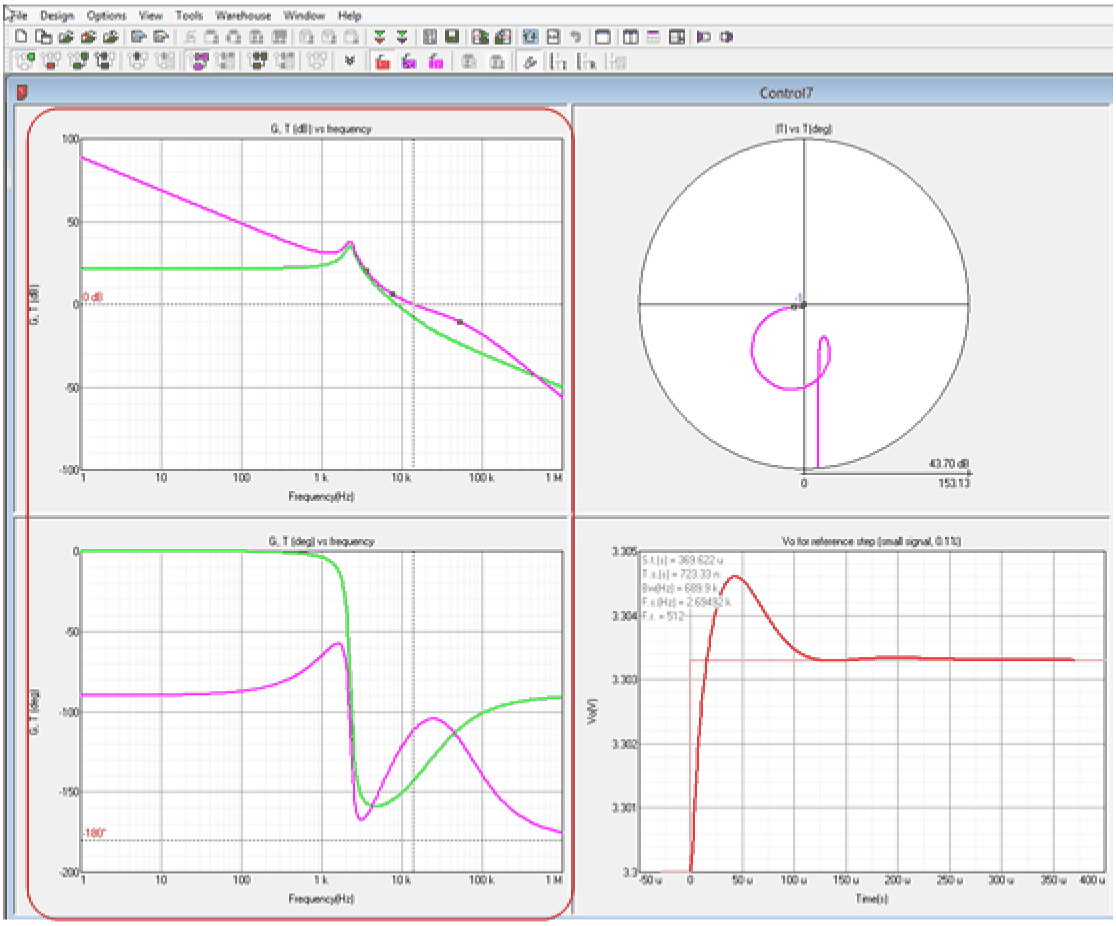
The Bode plot is used to characterize the frequency response of the system. It consists of two different graphs, the magnitude plot and the phase plot versus frequency. Frequency is plotted in a log axe.

Magnitude plot (dB)	Plots the magnitude of a given transfer function in decibels (dB) versus frequency. It is represented in the upper left panel of the SmartCtrl window.
Phase plot (º)	Plots the phase of a given transfer function in degrees versus frequency. It is represented in the bottom left panel of the SmartCtrl window.



In SmartCtrl there are seven different transfer functions that can be plotted in the Bode plot. To represent any of them, just click on the corresponding icon of the View Toolbar or select the corresponding transfer function within the View Menu.

Manual placement of poles and zeros

Additionally, when a type 3 or type 2 is used, poles and zeros of the compensator are represented

by means of three little squares.

Yellow	corresponds to fz
Red	corresponds to fp
Blue	corresponds to fi

The placement of the aforementioned zeros and poles can be varied by the designer just by clicking and dragging on each square. To enable this option **manual method tag** in the **design method box** must be selected.

Cross frequency

The cross frequency of the open loop is shown by means of a pair of dashed lines on the open loop transfer function of the system.

Click on right button

By right clicking on each plot a new window is opened with some additional options.

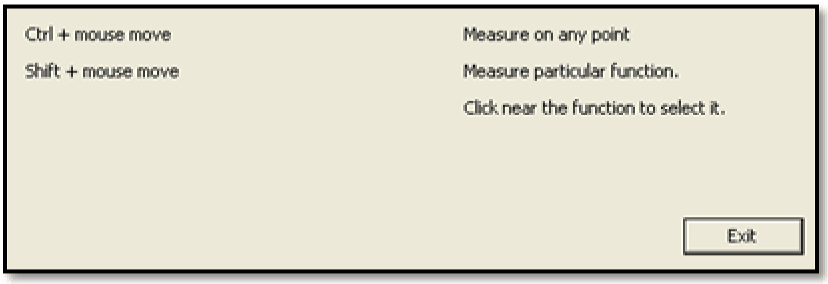
Copy	Copy the Bode Plot to clipboard
Export	This option allows exporting the data of the different frequency responses in several formats.
Help	Link to the on-line SmartCtrl help
Quick Help	Shows the keyboard shortcuts to measure directly on the plot

Measurement tools

Two different types of cursors are available:

Ctrl + mouse	Keep the Ctrl key pressed and move the mouse. Two crossed red lines are displayed and the two coordinates of the point on which the mouse is placed are given. You can measure at any point within the graph area.
Shift+mouse	Keep the Shift key pressed and place the mouse near one of the displayed module traces. The cursor will track itself to that trace, and the cursor will measure simultaneously the phase and module of the tracked trace. If you want to track the cursor to other trace, just left click on that trace. Additionally, if the selected trace is open loop transfer function, SmartCtrl will measure

simultaneously on both Bode plots (module and phase) and on the Nyquist diagram.



1.12.2 Nyquist diagram

Navigation: SmartCtrl > Graphic and text panels >

Nyquist diagram

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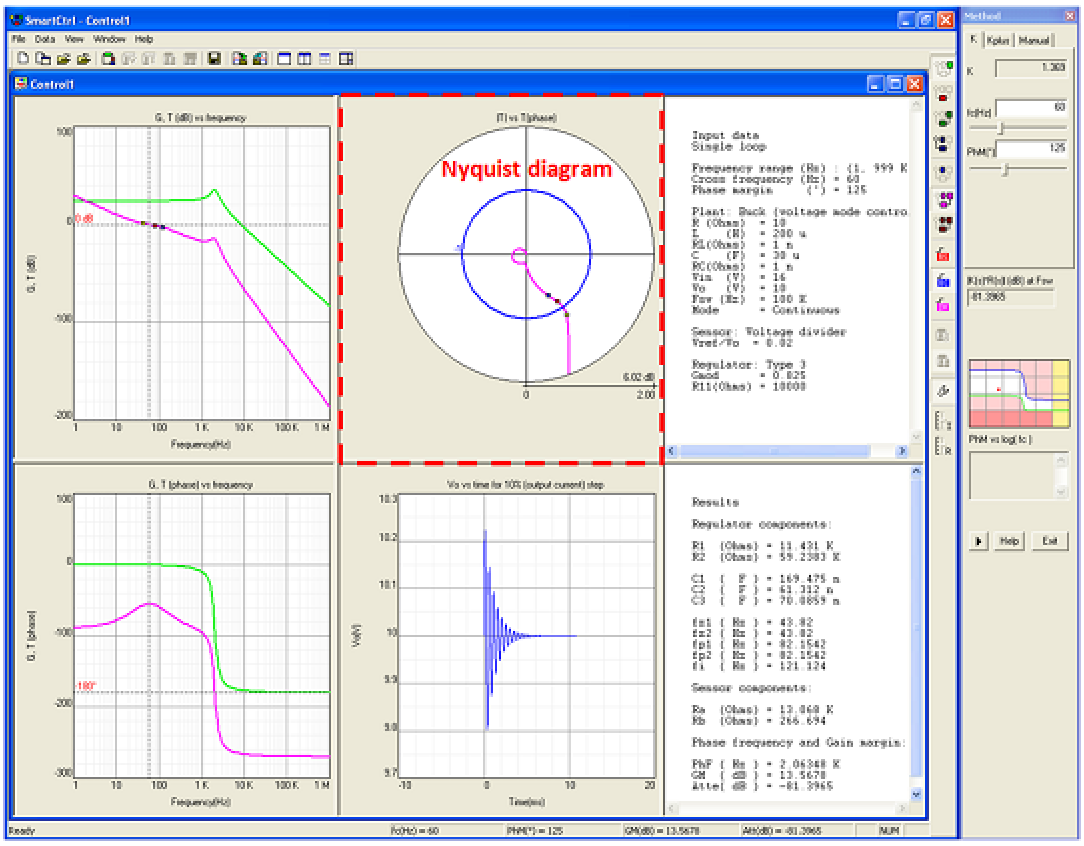
The Nyquist diagram, together with the Bode plot, is a graphical representation of the frequency response of a linear system.

For each ω, the resulting open loop transfer function is represented as Im(T) vs R(T). So, the gain at this ω is the distance from the represented point to the origin, and the phase is the corresponding angle.



In terms of stability, the polar Nyquist diagram provides a graphic and easy to evaluate criterion of the closed loop system stability based on the open loop system frequency response. This is, if the open loop transfer function is stable (no RHP poles), the closed loop system will be unstable for any encirclement of the point (-1, j0).

Poles and zeros

Poles and zeros of the compensator are represented by means of three little squares.

Yellow corresponds to fz

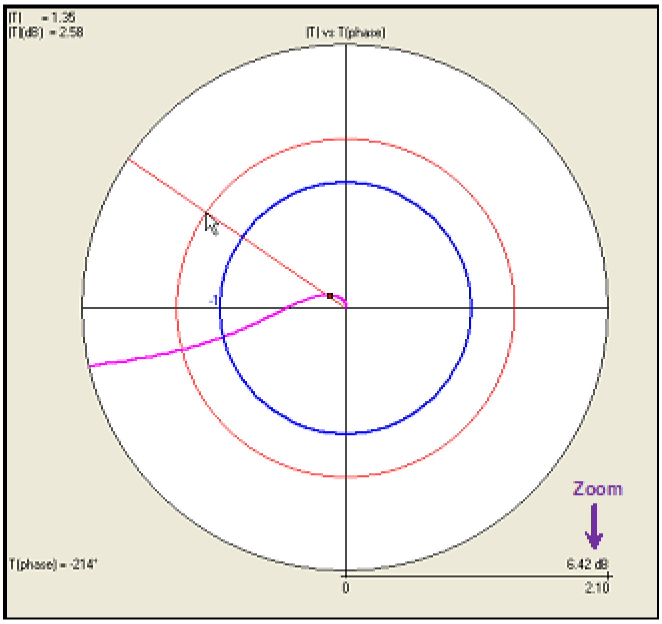
Red corresponds to fp

Blue corresponds to fi

However, unlike in the Bode plots, they cannot be placed manually.

Zoom

A zoom-in and zoom-out tool has been implemented by left-clicking and dragging the mouse within the white area of the polar plot. The relative scale is given by the radio of the outer circle both in dB and natural scale.



Copy to clipboard

The same way as in the Bode plots and the transient response plots, a copy to clipboard option is available through right click on the polar plot are that will allow the user to copy the current graph to the clipboard.

Click on right button

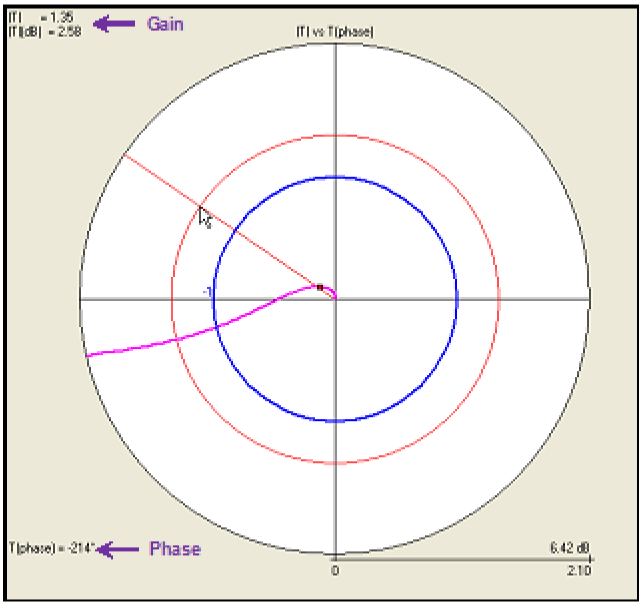
By right clicking on each plot a new window is opened with some additional options.

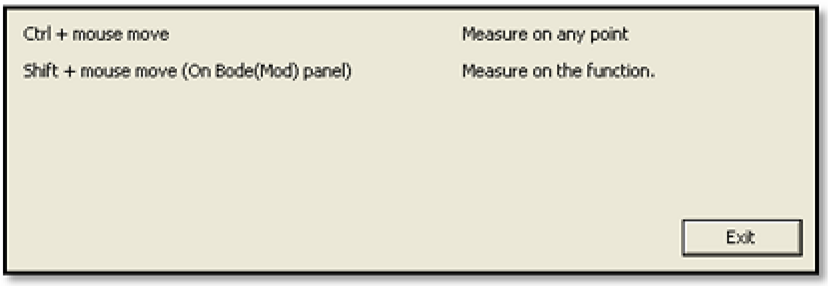
Copy	Copy the Bode Plot to clipboard
Help	Link to the on-line SmartCtrl help
Quick Help	Shows a short explanations about how to measure directly on the plot

Measurement tools

Two different types of cursors are available:

Ctrl + mouse	Keep the Ctrl key pressed and move the mouse. Two crossed red lines are displayed and the two coordinates of the point on which the mouse is placed are given. You can measure at any point within the graph area.
Shift+mouse	Keep the Shift key pressed and place the mouse near one of the displayed module traces. The cursor will track itself to that trace, and the cursor will measure simultaneously the phase and module of the tracked trace. If you want to track the cursor to other trace, just left click on that trace. Additionally, if the selected trace is open loop transfer function, SmartCtrl will measure simultaneously on both Bode plots (module and phase) and on the Nyquist diagram.





1.12.3 Transient response plot

Navigation: SmartCtrl > Graphic and text panels >

Transient response plot

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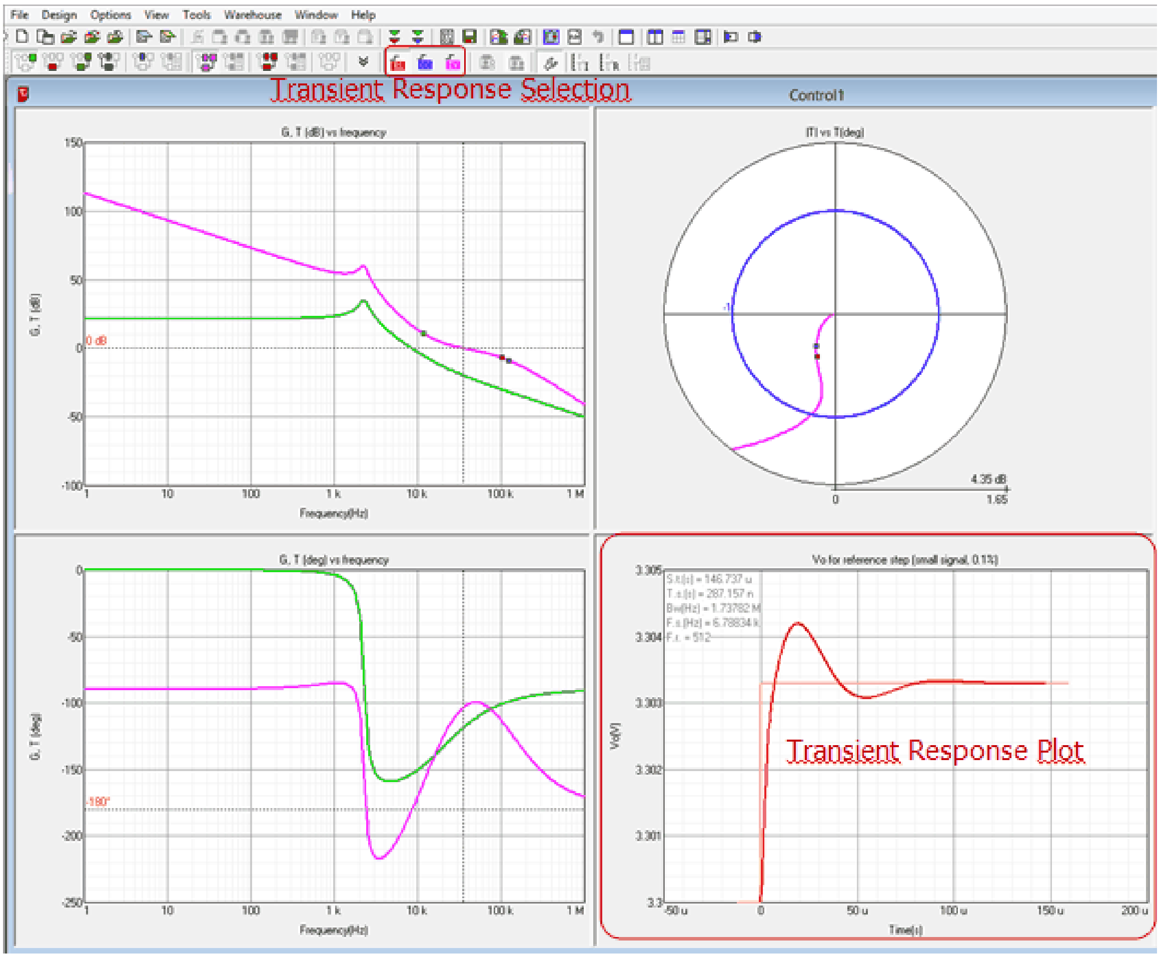
Transient response specifications, such as setting time and voltage peak transient values, are usually critical specifications when designing the control stage of a power converter. Therefore, providing a quick view to the transient response of the converter may greatly help the designer during the design process.

In SmartCtrl the three most significant transient responses have been developed. They can be plotted just by clicking on the corresponding icons of the **View Toolbar** or selecting the corresponding transient response within the **View Menu**.



By right clicking on the transient response plot, the following options are displayed.

Export

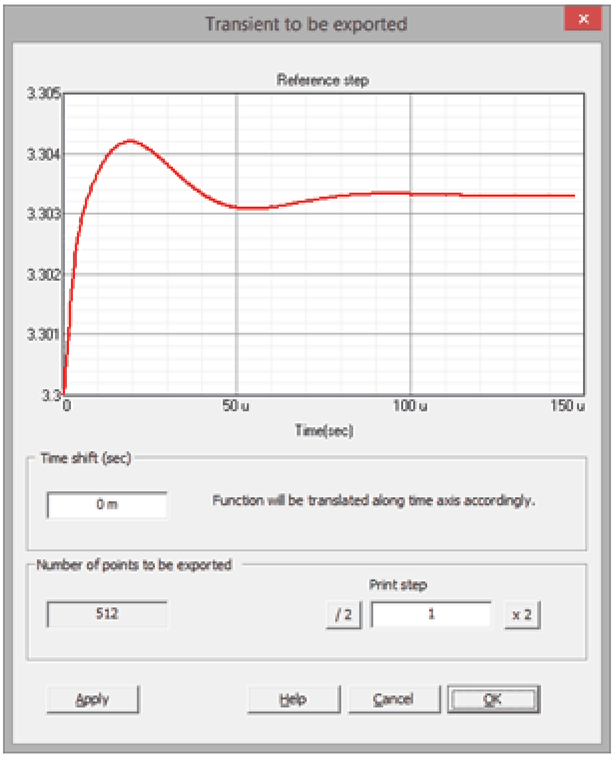
This option allows the user to export the current transient responses to a file which could be either .txt or .smv format. It is placed within the menu displayed through right click on the transient response panel.

Time shift:

This options allows the user to shift the time axis

Print step:

This option allows modifying the number of points to be exported. If the print step is multiplied by 2, only one point per two ones will be saved. This helps to reduce the size of the output file.



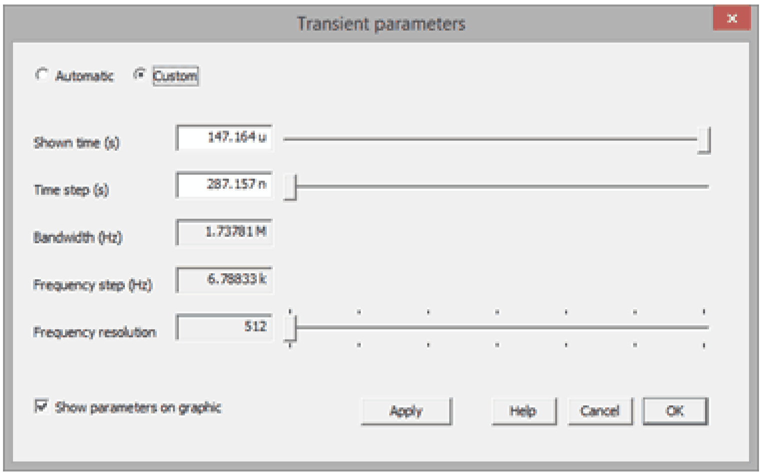
Copy

This allows the user to copy the current graphs in the clipboard

Modify transient parameters

This option allows the user to customize the transient response plot as well as the parameters of the computation algorithm

SmartCtrl makes an automatic selection of the parameters as the user modifies his design. By right clicking on the transient plot and selection the Custom option, a set of sliders are displayed so that the user is able to customize the settings listed bellow.



Time step: This option allows modifying the time interval between data points.

Frequency resolution: The transient response computation is based on sampling the frequency response of the power converter. The higher the resolution, the higher the number of sampled points, which means higher accuracy but also longer computational time. Therefore, the trade-off can be considered by the user.

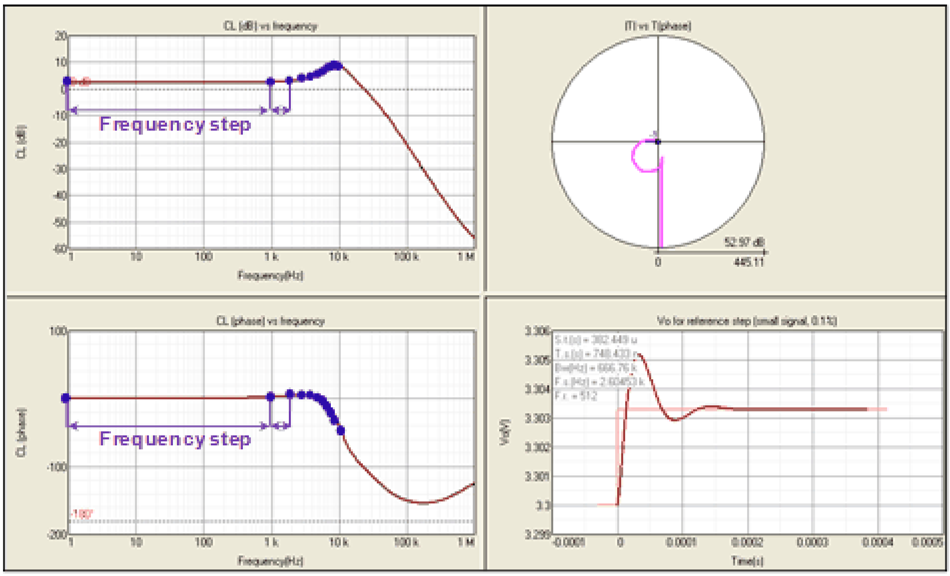
Shown time: This option allows the user to modify the time period displayed in the window. The maximum value is limited by the time step multiplied by the frequency resolution.

A zoom effect could be obtained by decreasing the shown time, decreasing also the time step parameter and finally increasing the frequency resolution if necessary.

In addition, the following information is displayed for informative purposes.

Frequency step: The frequency separation between two sampled frequency points. It is determinate by the frequency resolution and the bandwidth. An excessive high frequency step may lead to an incorrect transient plot.

Bandwidth: It determinates the maximum sampled frequency and is directly related to the time step selected by the user. An excessively low value may lead to an incorrect transient plot.



1.12.3.1 Steady-state waveforms

Navigation: SmartCtrl > Graphic and text panels > Transient response plot >

Steady-state waveform

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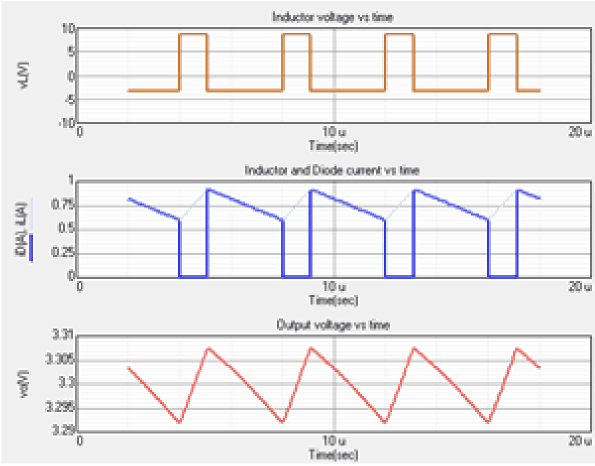
The "steady-state waveform" panel displays the most significant waveforms of the power plant and the modulator once the steady state is reached.

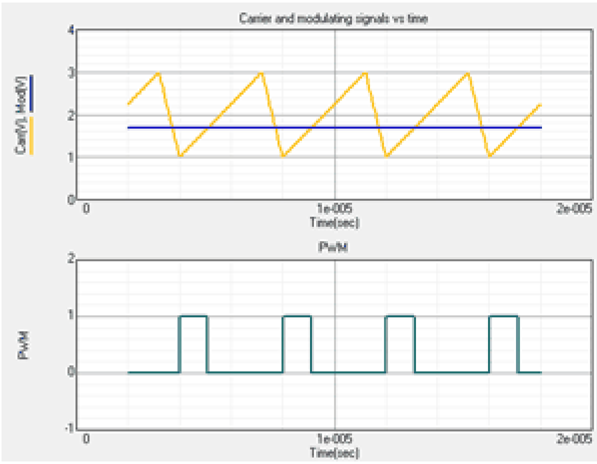
Power stage waveforms.



The available wave forms are:

Inductor voltage
Inductor and diode current
Output voltage

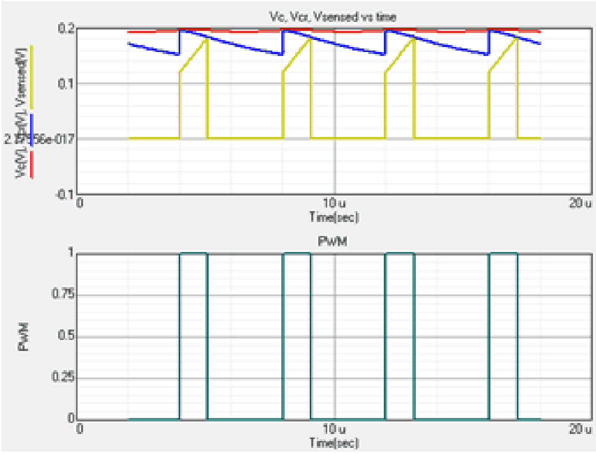
PWM Modulator waveforms.



The available wave forms are:

Carr[V] · Carrier signal
Mod[V] · Modulating signal
PWM [V] · Mosfet gate voltage.

Peak current mode control waveforms

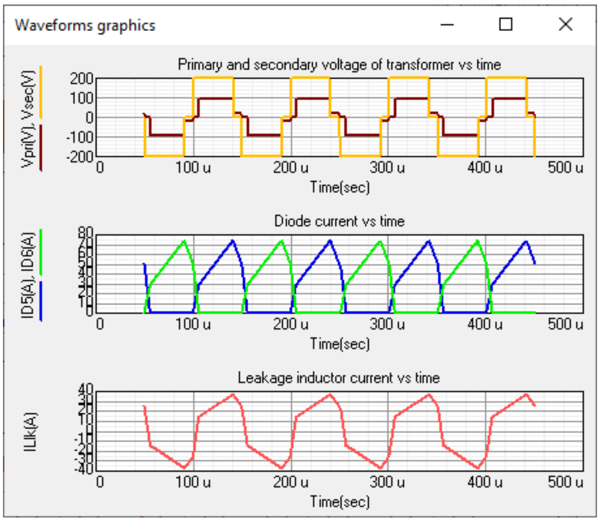


The available signals are:

Vc(t) · Modulating signal
Vcn(t) · Compensating ramp
Vsensed(t) · Sensed MOSFET current or inductor current

In the case of the forward converter Vsil(t) is also plotted to show the output filter inductor current.
PWM [V] · MOSFET gate voltage.

Phase Shifted Full Bridge additional waveforms



The available signals are:

Vpri(V) · Primary voltage
Vsec(V) · Secondary voltage
•ID5(A), ID(6) · Diode current
•ILlk(A) · Leakage inductor current

Phase Shifted Full Bridge Dual Active Bridge (DAB) additional waveforms

For the Dual Active Bridge please select the appropriate link (NEW in version 5.0):

[Phase Shifted Dual Active Bridge (VMC RL - V1 to V2)]
[Phase Shifted Dual Active Bridge (VMC ERL - V1 to V2)]
[Phase Shifted Dual Active Bridge (CS ERL - V1 to V2)]

Measurement tools

Two different types of cursors are available:

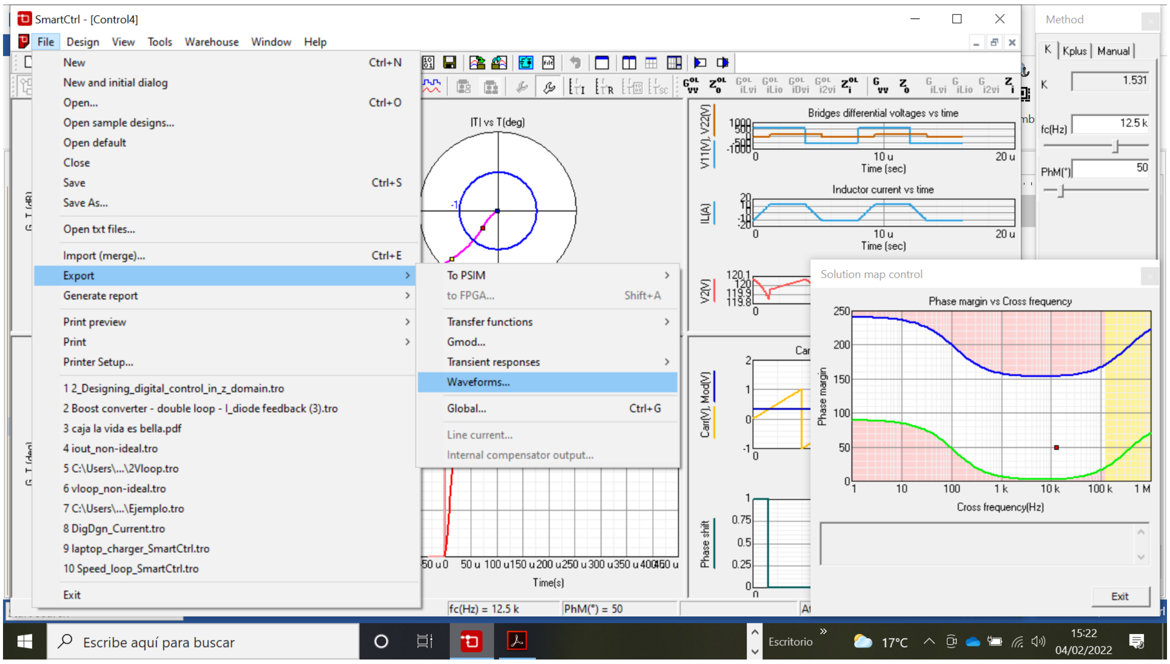
Ctrl + mouse	Keep the Ctrl key pressed and move the mouse. Two crossed red lines are displayed and the two coordinates of the point on which the mouse is placed are given. You can measure at any point within the graph area.
Shift+mouse	Keep the Shift key pressed and place the mouse near one of the displayed module traces. The cursor will track itself to that trace, and the cursor will measure the two coordinates. If you want to track the cursor to other trace, just left click on that trace.

Exporting tools

Right click	Through right click on the steady-state waveform panel, a pop-up menu becomes available. In it, the copy and export options are available.

- Copy: copies the graphic panel to the clipboard.
- Export: automatically redirects the user to the export option within the File Menu.

Use the **export** option in the main menu:



1.12.4 Text panels

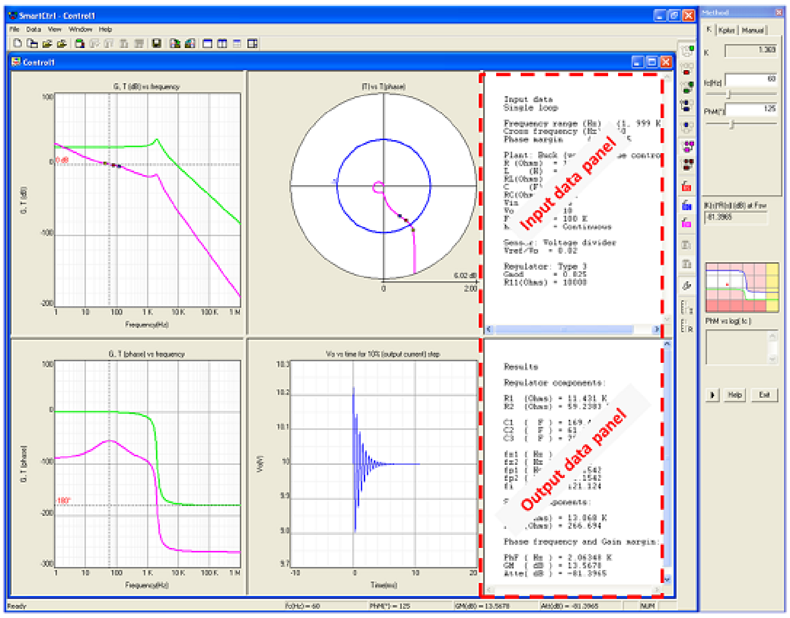
Navigation: SmartCtrl > Graphic and text panels >

Text panels Previous Top Next

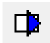
Two text panels are available to provide a complete list of the numerical values of all the elements that compose the whole circuit as well as some selection parameter such as type of compensator , type of sensor, etc.

Text panels are shown through the View Menu or by clicking on the corresponding icons in the main toolbar:

View Menu **Main toolbar**



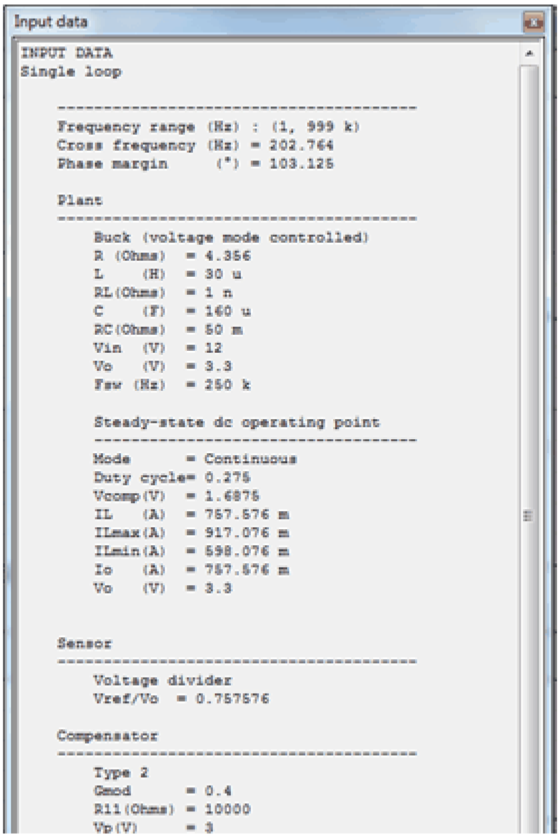
Icon  opens **input data panel**.

Icon  opens **output data panel**.

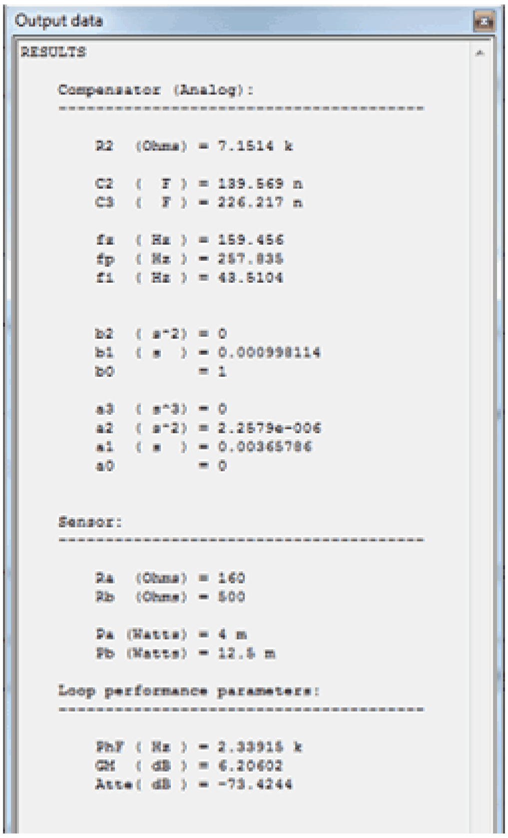
The Input Data Panel summarizes the input parameters of the converter such as the power stage parameters, the steady-state dc operating point, the compensator parameters, etc...

The Output Data Panel shows the numerical information about the design of the compensator. The compensator resistances and capacitances values as well as the frequencies of its poles and zeroes, are updated in real time. In addition, the most important loop characteristics are provided: that is, the phase margin, gain margin and attenuation at the switching frequency.

In the case of an average current mode control, which involves two nested control loops, the information regarding both the inner and the outer control loops is provided.



Input data panel.



Output data panel.

1.13 Solutions map

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Solutions map

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The appropriate selection of f_{cross} and Phase Margin is one of the key issues for loop optimization.

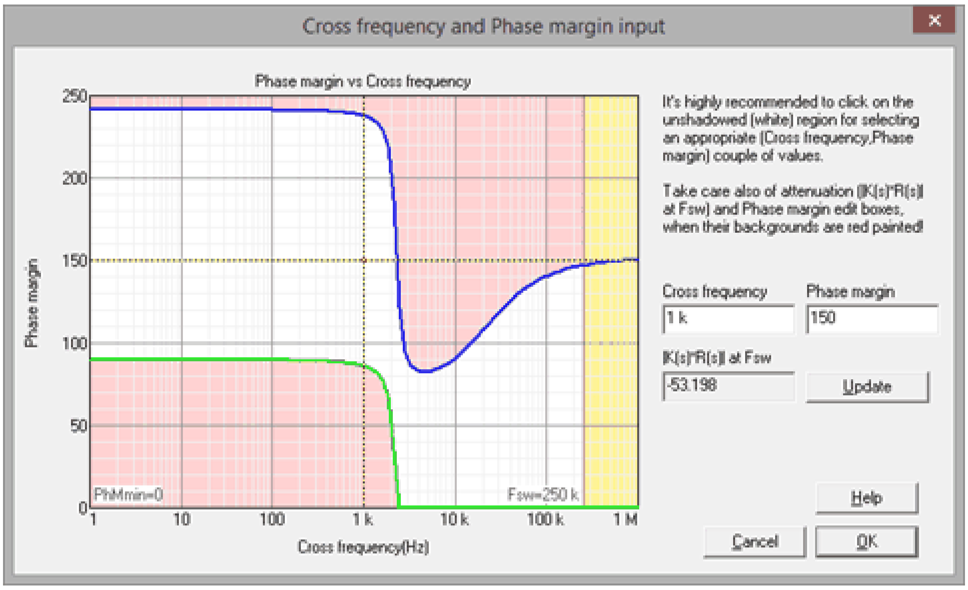
In order to ease the first attempt when designing a control loop, an **estimation of the stable solutions space** has been developed under the name of **solutions map**. Based on the selected plant, sensor and type of compensator, the solutions map provides a safe operating area of the different combinations of f_{cross} and PM that lead to stable systems. The parameters involved are represented as **PM vs frequency**.

Just by clicking within the white area, a set of (f_{cross} and PM) that lead to an stable solution is selected.

The input boxes (white background) are automatically updated

And so is the attenuation achieved at f_{sw} box. It is an output parameter (grey background) and represents the attenuation achieved by the combination of the sensor and the compensator at the switching frequency.

Additionally, when any of the three aforementioned values is uncommonly low or high, the boxes background are red-colored in order to draw the designer attention.



Boundaries

The boundaries, that determine the valid area (white area), **represent the maximum and minimum phase margin that can be achieved for any kind of compensator.**

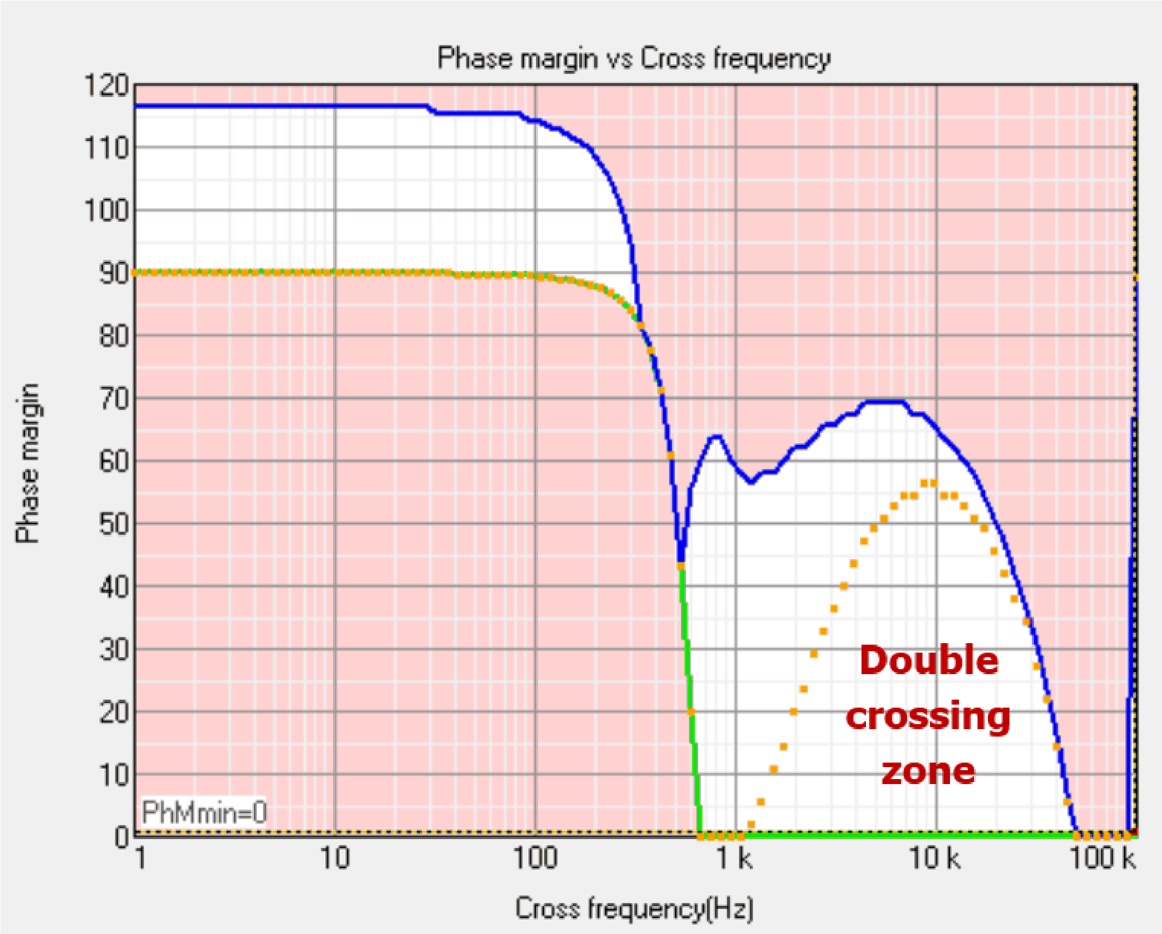
The simple integrator is a particular case of any regulator; therefore, it provides the lowest PM limit by adding 90 degrees to the phase of the open loop transfer function without regulator (plant, sensor and modulator) (green line).

The upper limit of the solution map is given by the maximum phase boost provided by each kind of compensator (blue line).

In terms of frequency, the solutions space is **limited by the switching frequency**, f_{sw}.

Double 180º crossing

Even while being a stable system, a double crossing by 180º can occur, which could lead to instabilities if, for any change in the operation point, the gain drops. Since those are still stable points, they are inside the white area, but an orange dotted line marks the frontier between the points where no double crossing occurs (above the orange line) and the ones when it does (below it), as seen in the next image.



When the first design point has been selected within the Solution Map, SmartCtrl shows its main screen. In the main screen the solutions Map will be shown as a floating window. The position of this window can be changed by the user by right clicking on the Solution Map window plus mouse move. Important Warning messages will be shown in the bottom part of the Solution Map window.

1.14 Equation Editor

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Equation editor

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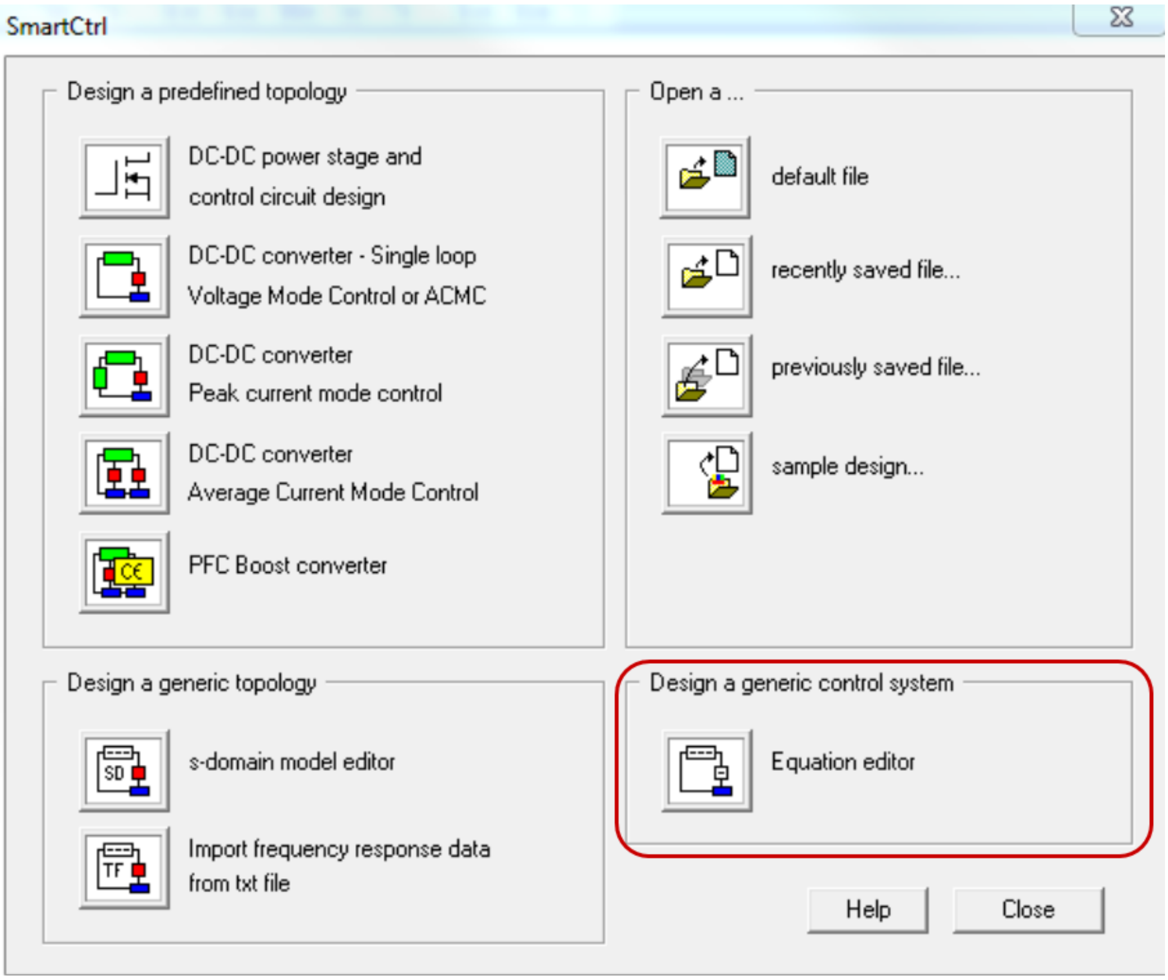
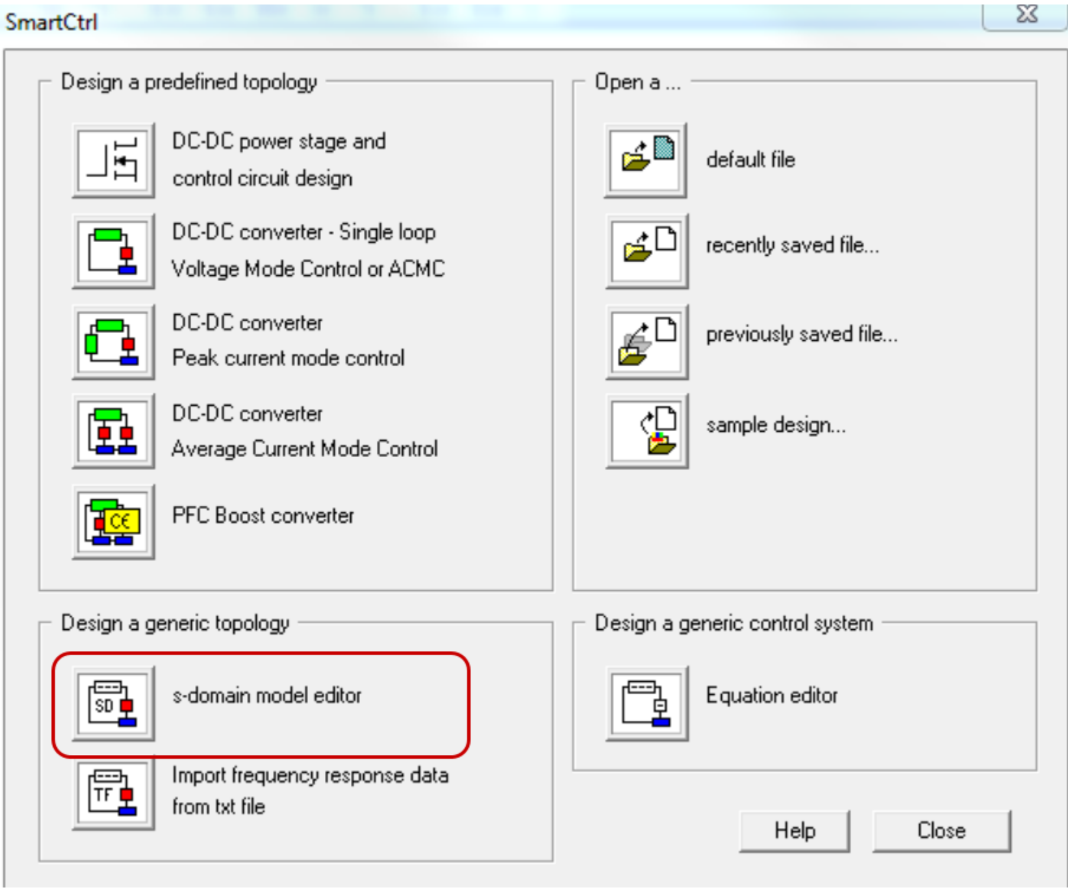
The Equation editor is a powerful tool that allows the user to define and control a system by means of its transfer function in S-domain or in Z-domain.

There are three ways of accessing it:

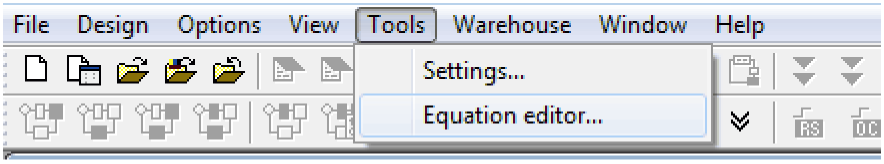
•Using the initial dialog menu, **Design a generic control system**: In this case the user has to define the transfer functions for the plant and sensor. For the compensator the user can select among different predefined topologies or defined a customized compensator transfer function.



•Using the initial dialog, **s-domain model editor**: The plant is set by its s-domain transfer function, the sensor will be selected form the predefined list and for the compensator, the user can select among different predefined topologies or defined a customized compensator transfer function.



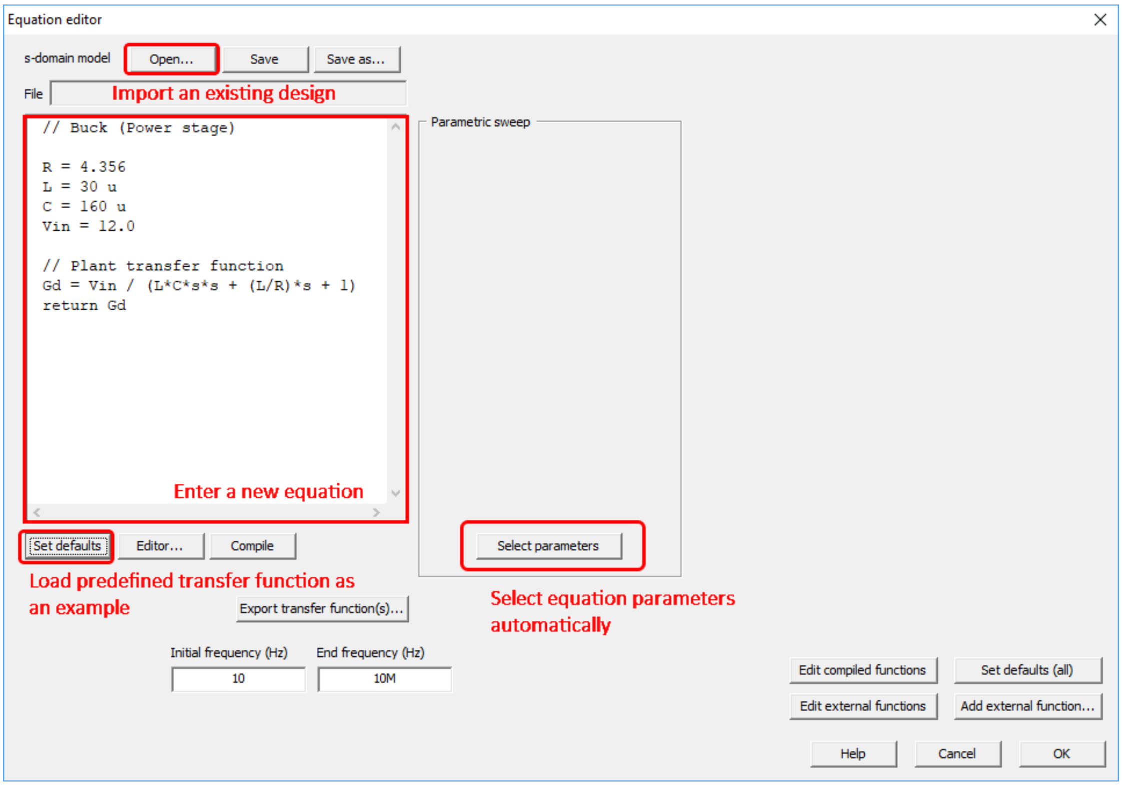
•Using the option **"Equation editor"** in the Tools menu: Just the plant is set and a txt file is generated, which can be used later on as input for the calculation of a regulator.



The design steps and options are similar for the three methods:

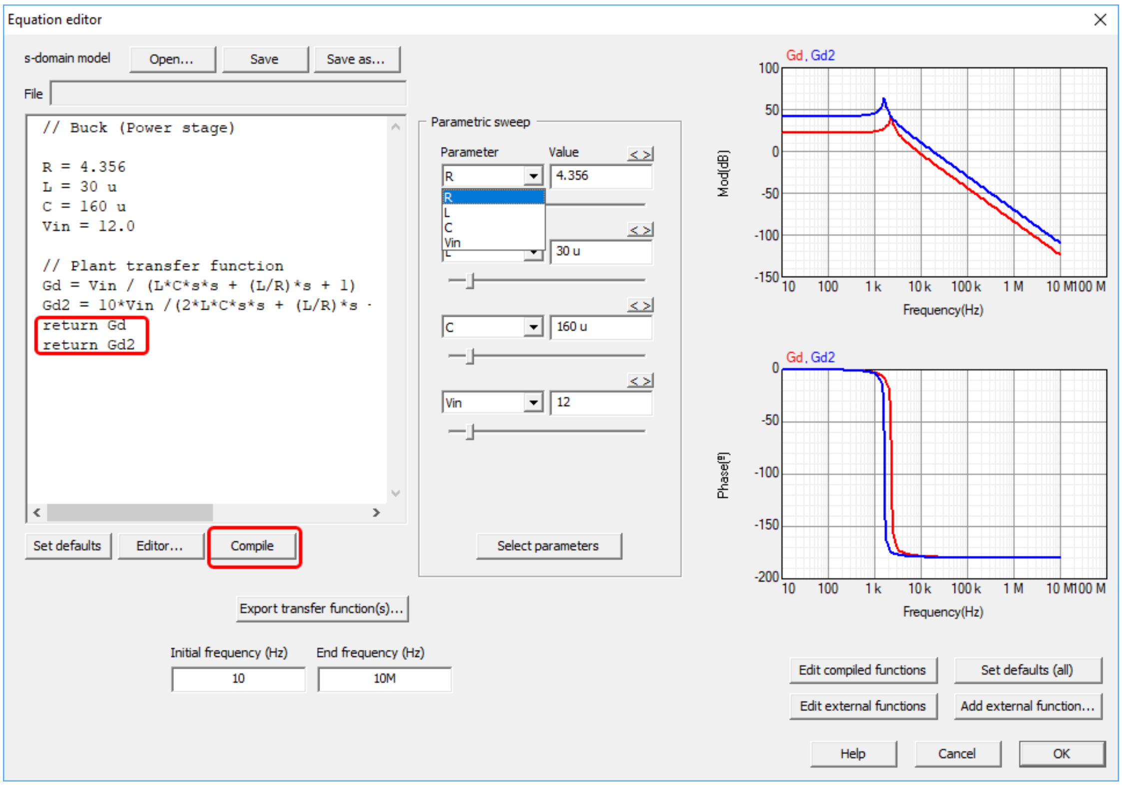
First, the user must define the transfer function, choosing between two different options:

•Import a previous design (click on open)
•Define a new transfer function entering it in the editor. Check the editor rules in the next chapter.
•*Additionally, there is a predefined transfer function that can be loaded by clicking on "set defaults".

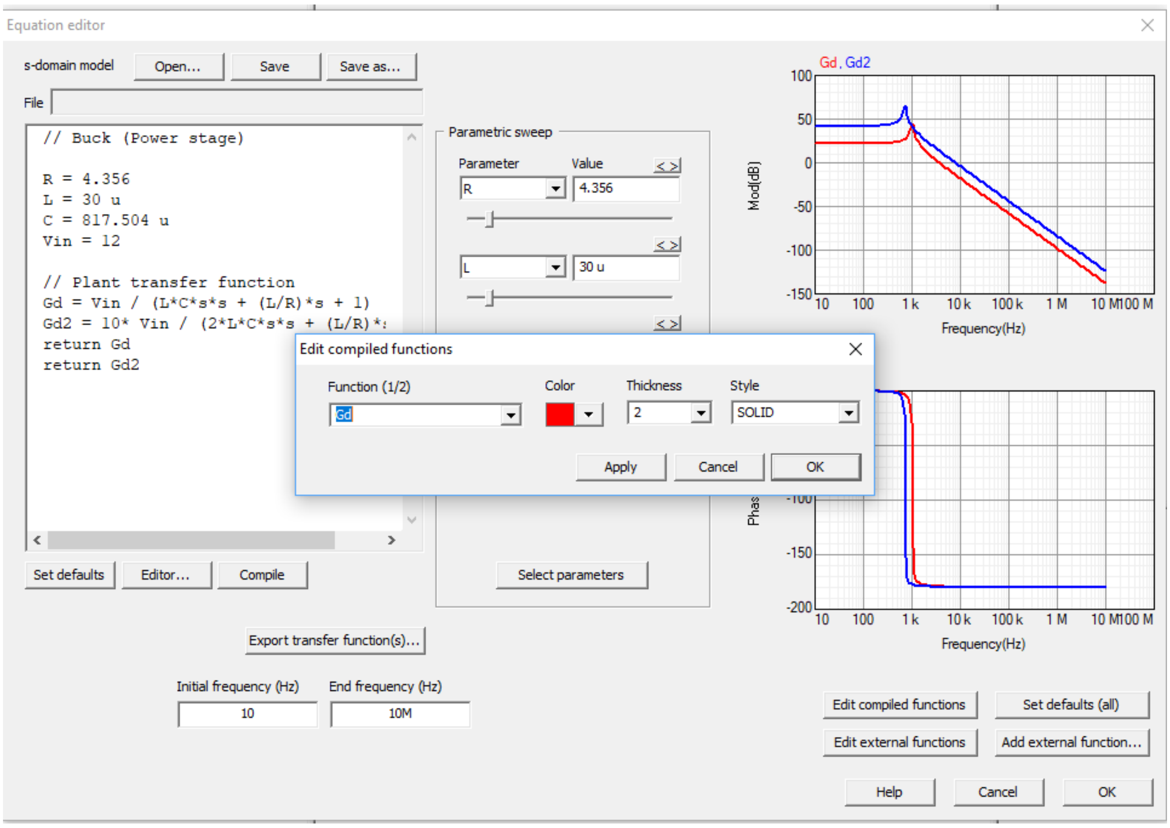


Once the equation has been introduced:

•Write **"return"** as the last sentence, followed by the name of the transfer function. Only when selecting the option Equation editor from the Tools menu, more than one transfer function can be returned at the same time, as shown in the figure below, allowing a fast comparison of results.
•Click on "Save" to save the mathematical equations in a text file with extension .tromod
•Click on "compile" to continue, the Bode plot of the returned transfer functions will appear on the right side of the window.
• If desired, the frequency response of the transfer function can be exported as a .txt file by clicking on "Export transfer function(s)". Afterwards, it can be recalled through the "Add external function" button and displayed in the Bode plot graphic panel. It can also be used as the system to be controlled in the main SmartCtrl window.

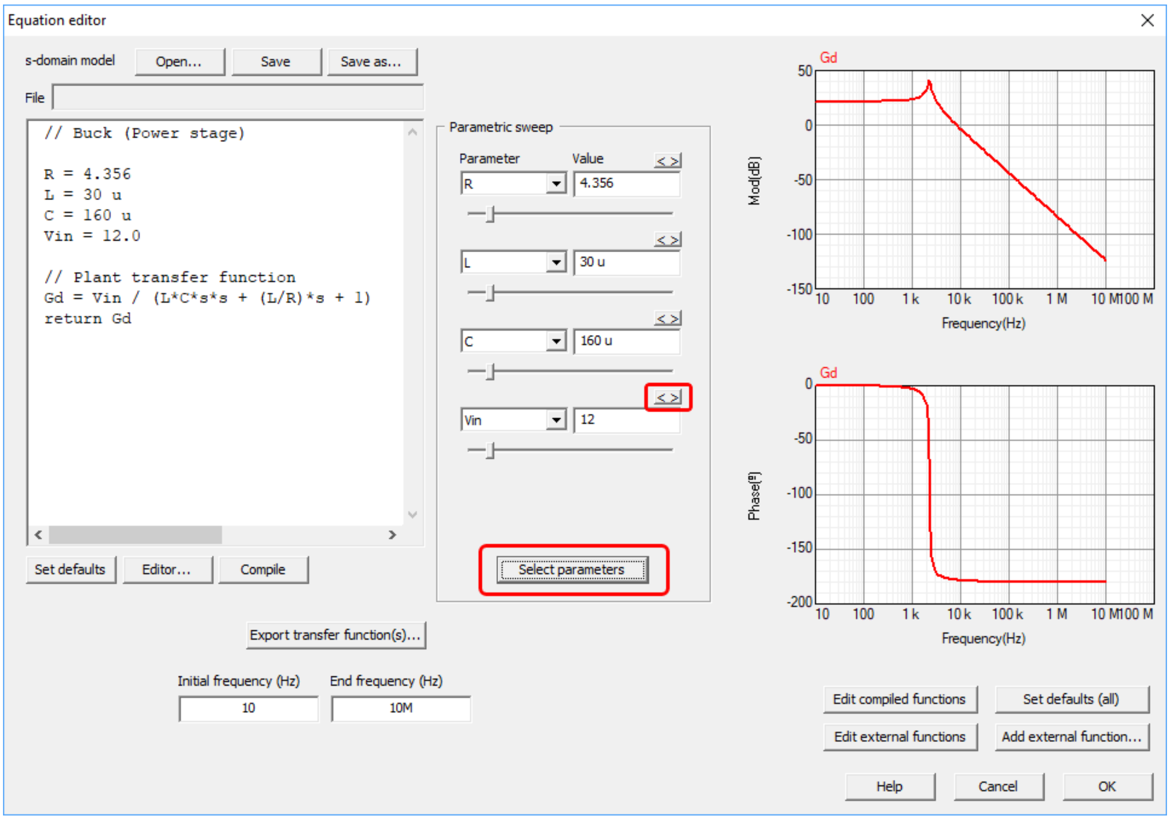


The Equation editor can display several transfer functions by adding return instructions. To change the properties of the curves displayed, click on Edit compiled functions button. Color, thickness and style can be selected for each curve.

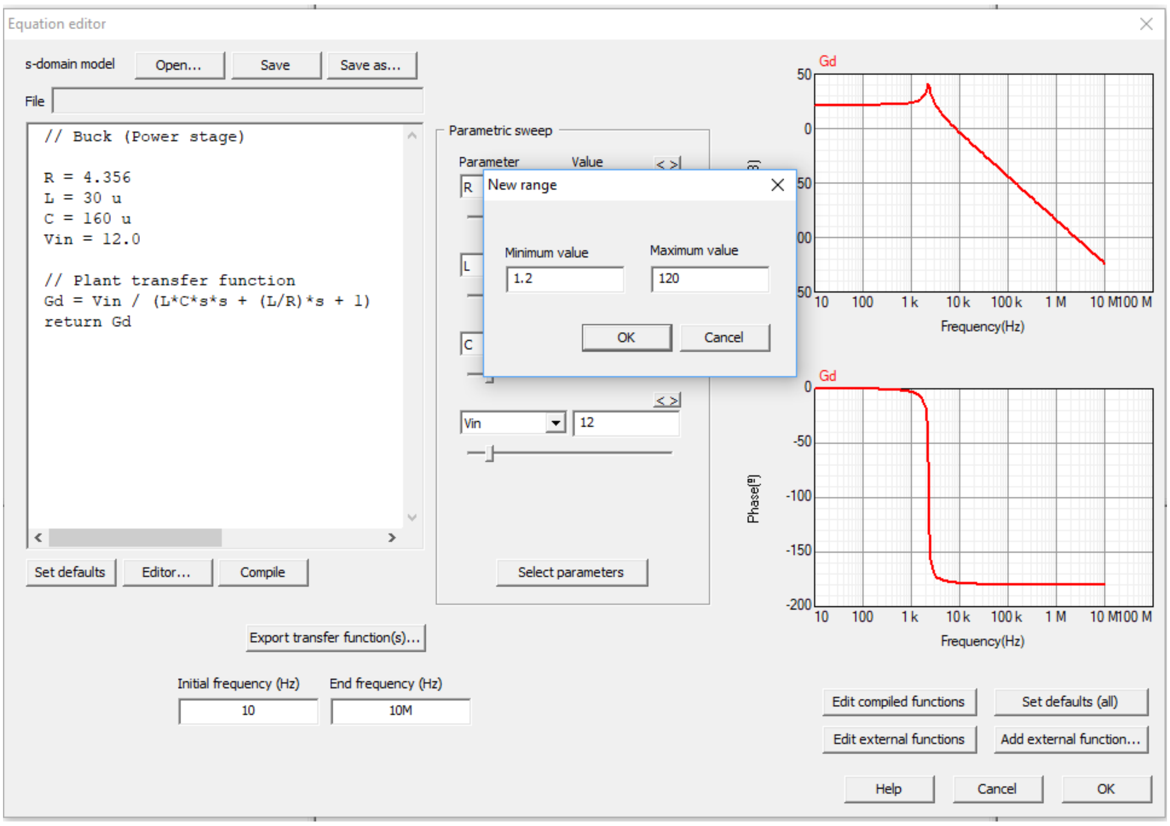


The Equation editor also allows the user to perform a parametric sweep of the defined variables.

To perform the sweep, click on Select Parameters button, as shown in the figure below.

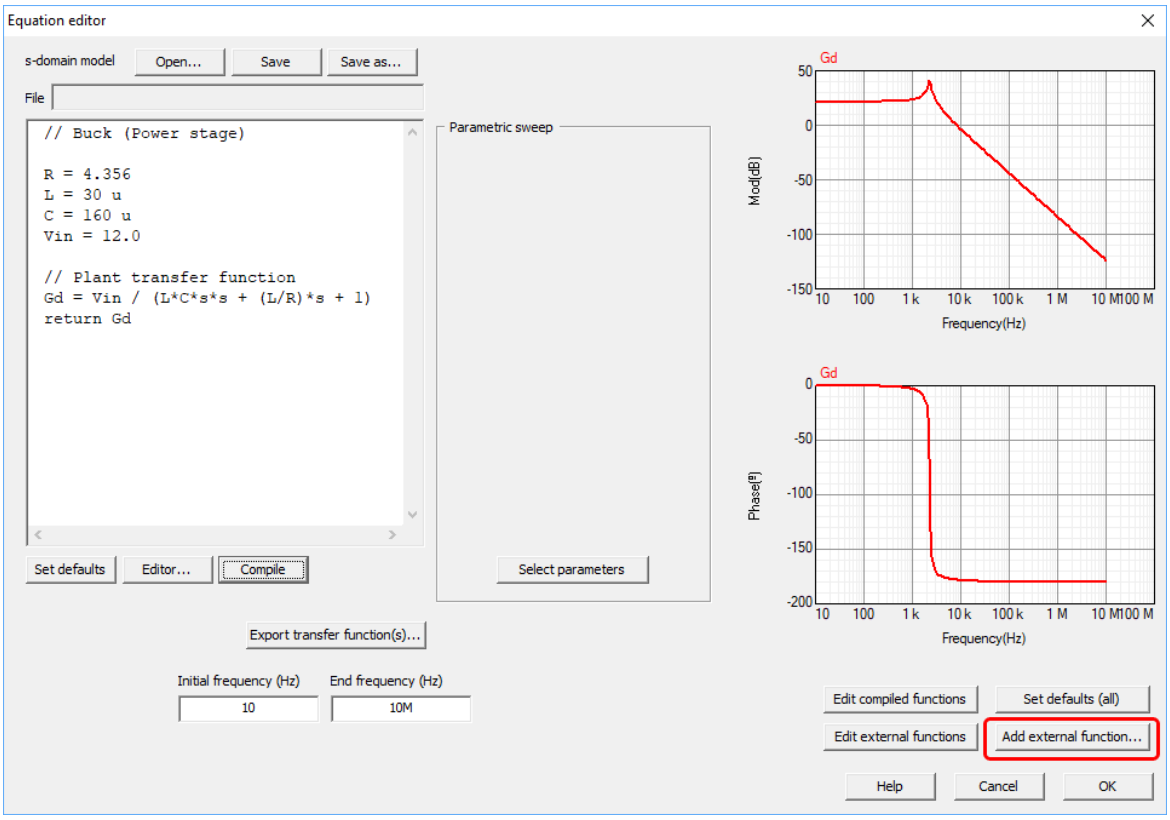


The transfer function parameters will automatically be displayed, use the slider to change the parameter value and the arrows button to adjust the parameter range, minimum and maximum values. The changes are automatically displayed in the Bode plot window.



If the whole system, plant and regulator, has been made this way, the sweep can also be done later on, by clicking on Modify source code variables. Refer to Parametric sweep.

To ease comparison with other transfer functions, their Bode diagram can be imported by clicking on Add external function and browsing for a .txt file with three columns separated by tabs, being frequency, magnitude and phase.



1.14.1 Editor box

Navigation: SmartCtrl > Equation Editor >

Editor box

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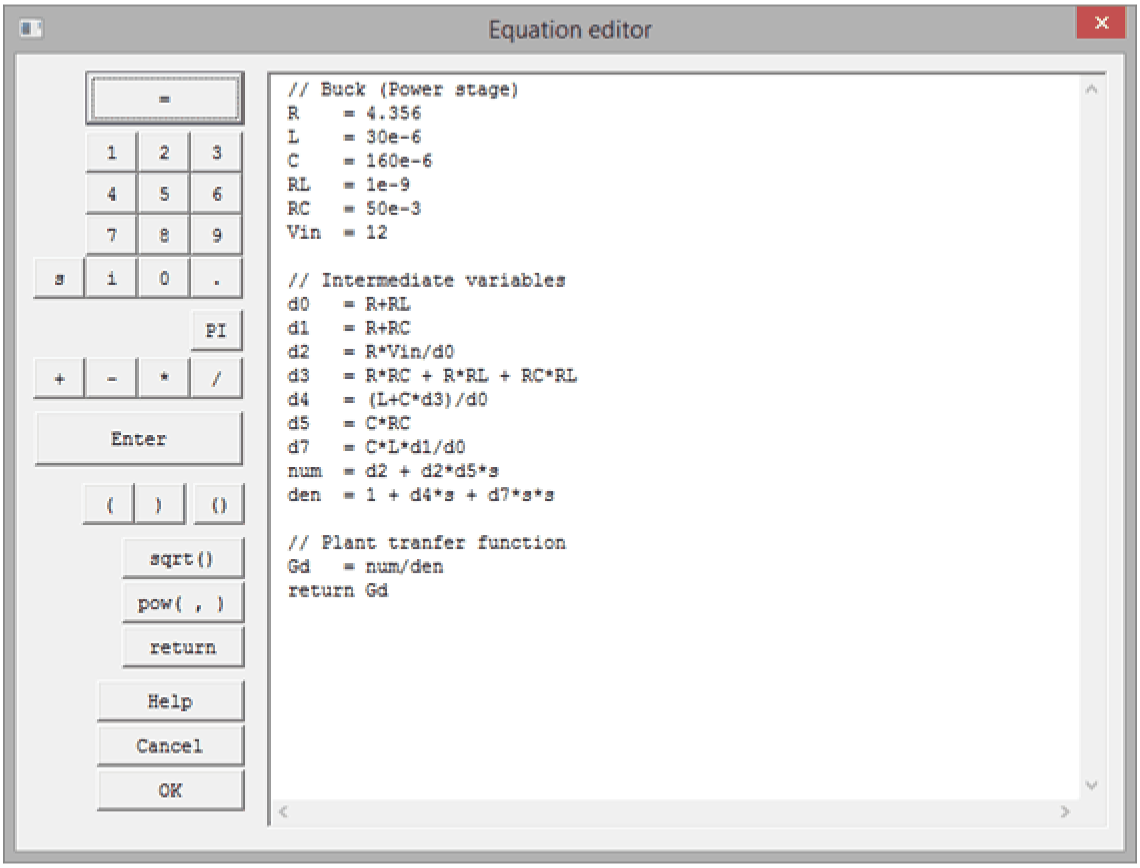
The equation editor allows the user to define a transfer function as an algebraic expression. The basic rules that must be taken into account when using this editor are listed below:

1. There are two types of instructions: assignment and return.
2. Only one instruction per line is permitted (whether it is assignment or return).
3. Blank lines are allowed.
4. Rules for naming variables in assignment instruction:
    a. The names must begin with an alphabetic character.
    b. The name can be formed of alphabetic or numeric characters, or underscore.
    c. The names sqrt, pow, return and PI are reserved names that cannot be used as variable names.
5. Rules related to mathematical expressions:
    a. Valid operator for algebraic expressions are +, -, *, /.

b. Expressions can use grouping parentheses.
c. The available built-in functions are:
   sqrt(a) · calculates the square root of a
   pow(a, b) · calculates 'a' raised to 'b'.
d. Algebraic expressions can include the built-in functions.



1.15 Import and Export

1.15.1 Export

1.15.1.1 Export transfer function

Navigation: SmartCtrl > Import and Export > Export >

Export transfer functions

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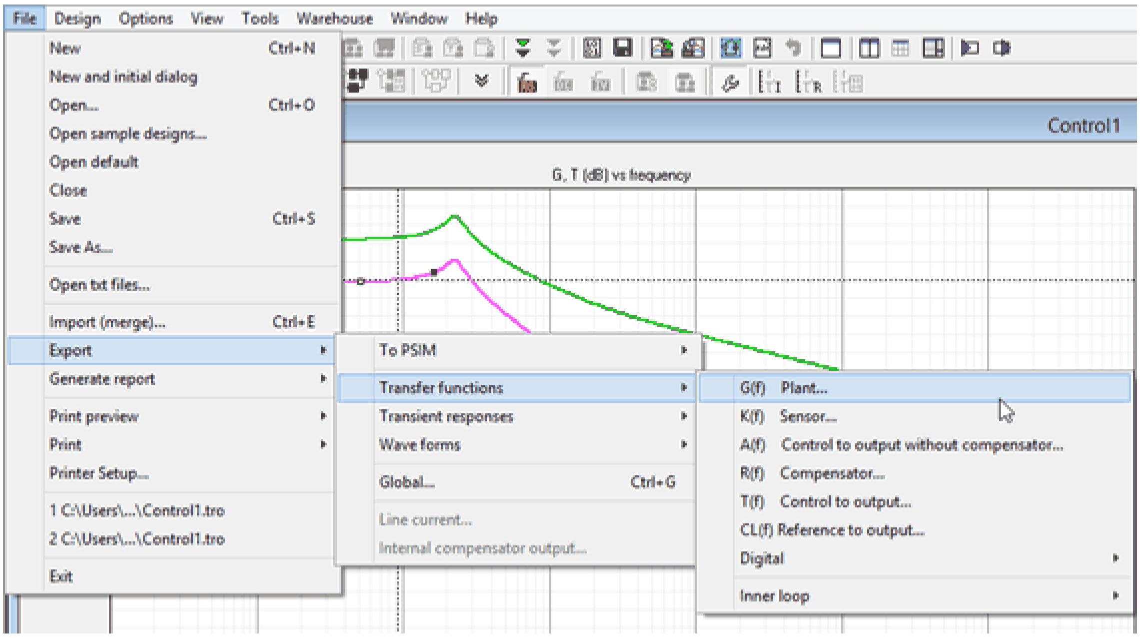
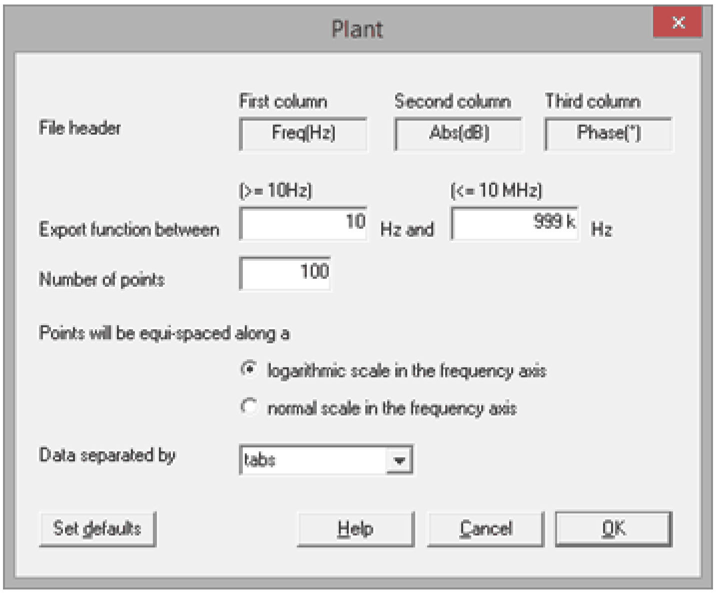
SmartCtrl provides three different exporting options which are available under the export item of the File Menu. The first of the exporting options is export transfer functions which is also available through left click on the icon  placed in the main toolbar.

Any of the transfer functions available can be exported to a .txt file. To do that, the designer must select the function to export within the available list and set the options of the file in the corresponding dialogue box.



The addressed file is formed by three columns containing the frequency vector, the magnitude in dB and the phase in degrees respectively.

The file options and characteristics are contained in the "Exporting transfer function dialogue box" and they are described below:



File Header	It contains the name of the three columns of the file.
Export function between	The designer is able to set the frequency range of the exported transfer function
Number of points	Number of points to be saved in the file

Points will be equi-spaced along a:
Logarithmic scale in the frequency axis
Decimal scale in the frequency axis

Data separated by:
tabs
spaces
commas

1.15.1.2 Export to PSIM

Navigation: SmartCtrl > Import and Export > Export >

Export to PSIM

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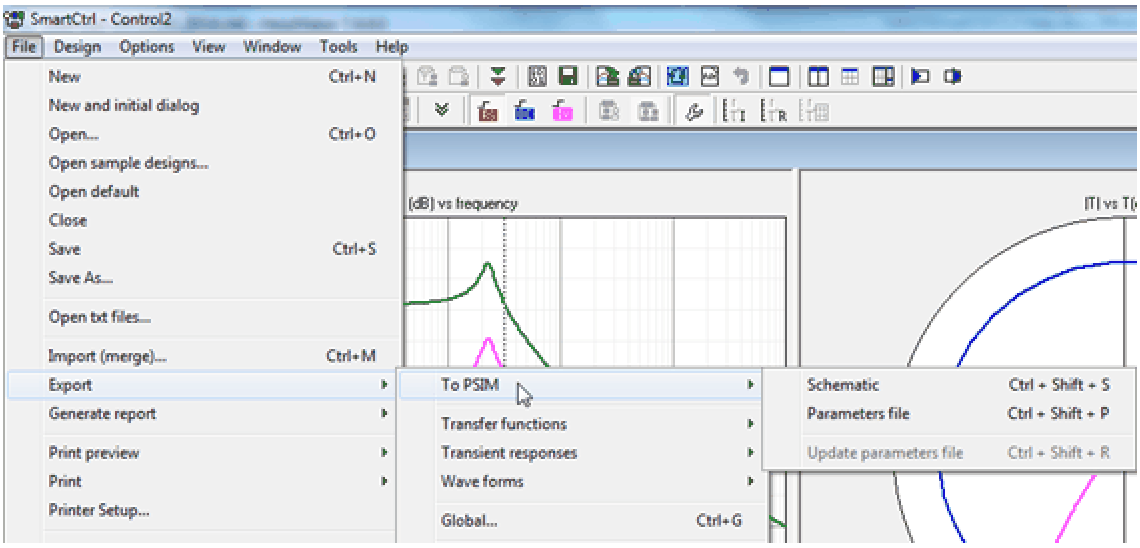
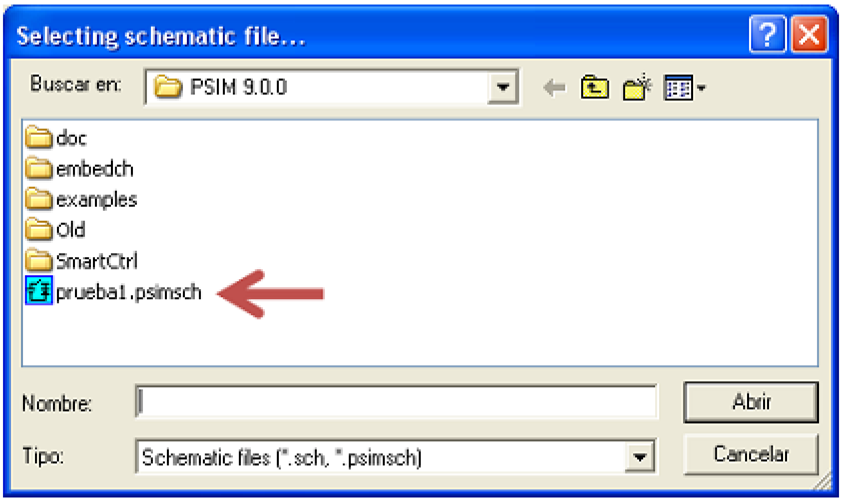
SmartCtrl provides a link with PSIM software. Once the regulator has been designed, the power stage and the compensator can be exported to PSIM, providing an automatic generation of the schematic and/or an exportation of the parameters of the design performed in SmartCtrl. This schematic can be used to validate the design using PSIM.

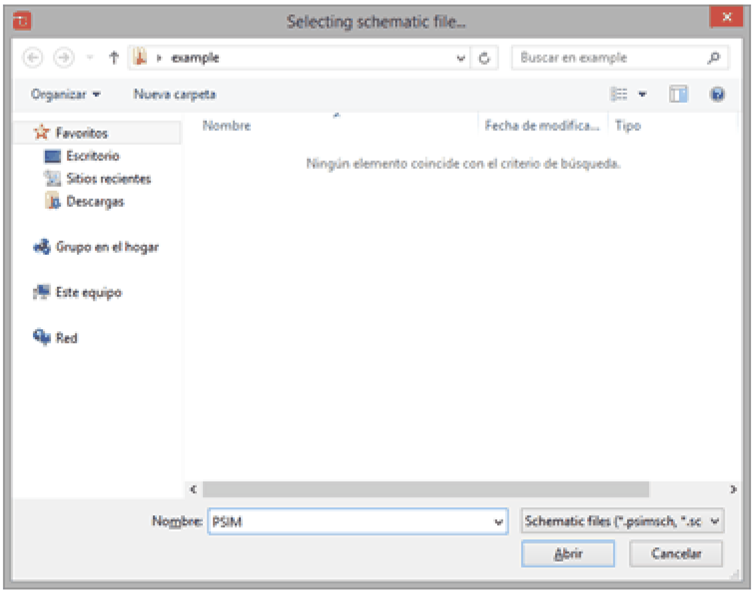
In the File Menu, it is available the export option To PSIM. The user can select between exporting the schematic, only the parameters file or just update a previously exported parameters file.



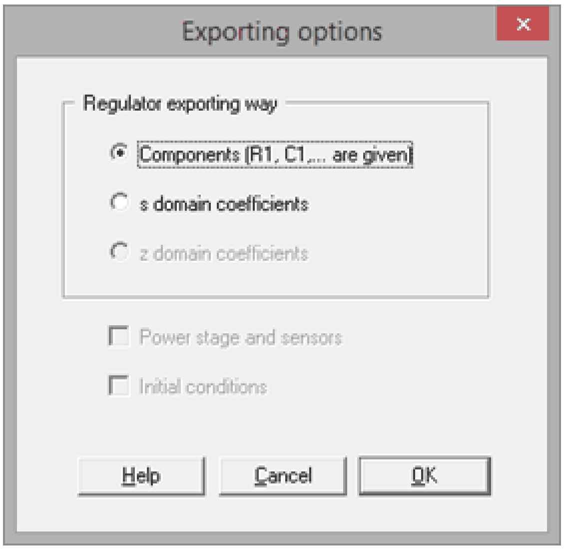
Export to PSIM (schematic)



In the first step the user will be asked to select the path and the name of the PSIM file in which the schematic will be inserted. If the file has not already been created, a new PSIM file will be created with the name provided by the user.

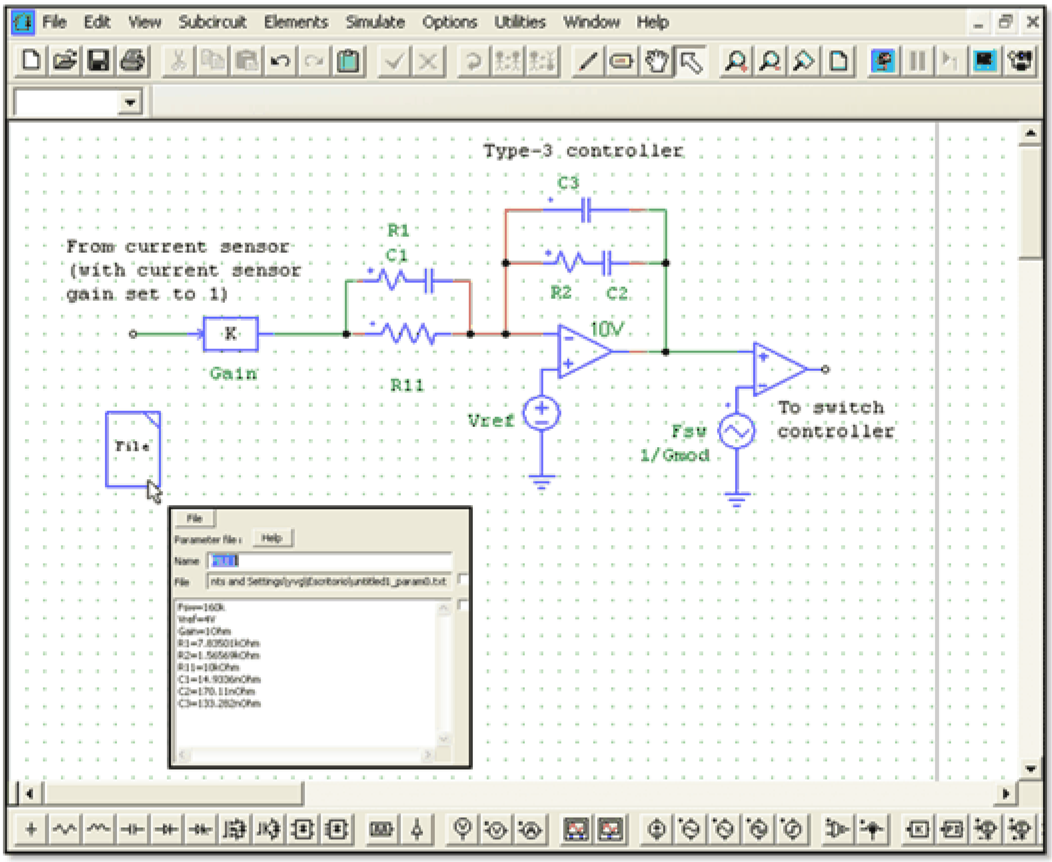


In the next step, the user will be asked to choose between different options:

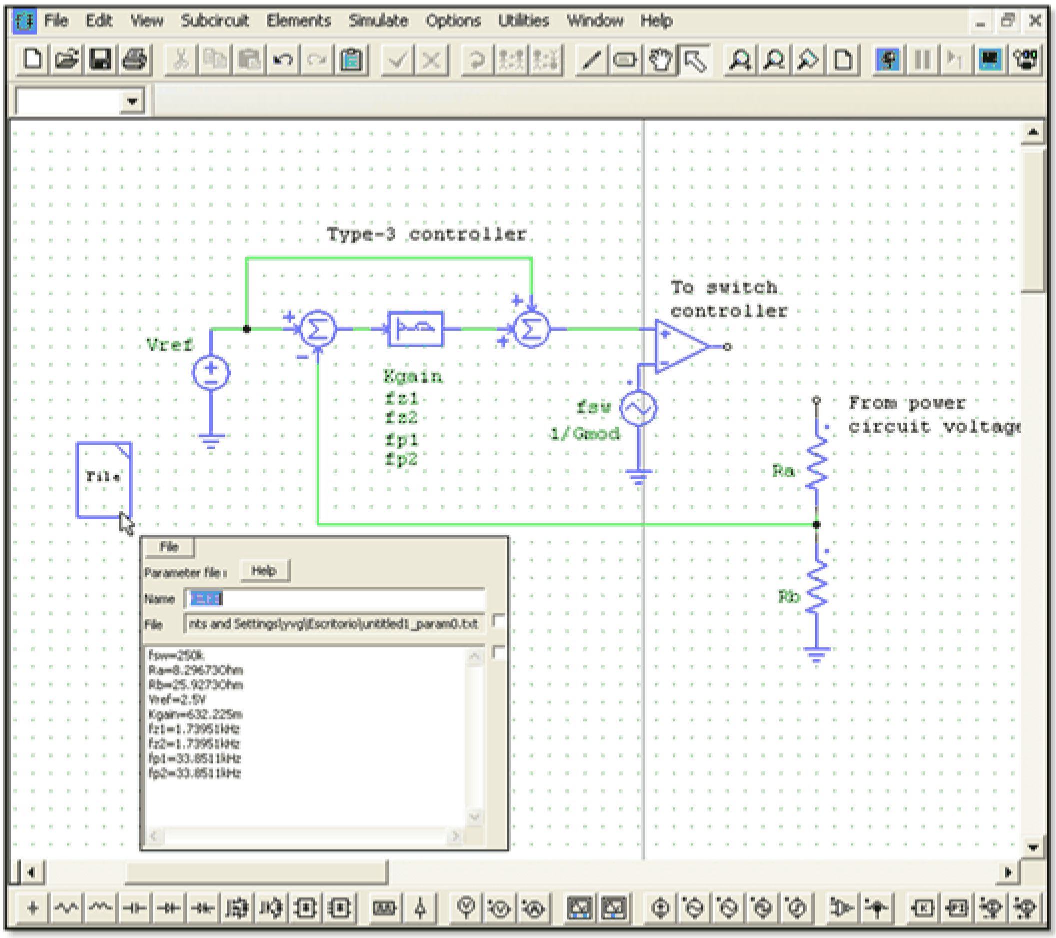


Compensator exporting way

Components (R1, C1, ... are given): the schematic and parameters of the compensator will be exported with an analog implementation (Operational amplifier and passive components) like in the following example.



s-domain coefficients: the schematic and parameters of the compensator will be exported in the form of PSIM control blocks, like in the following example.



z-domain coefficients: the schematic and parameters of the compensator will be exported in the form of a z-domain transfer function. Therefore it is necessary to configure the "Digital Settings" before selecting the z-domain format for exportation to PSIM. Besides the z-domain transfer function that represents the digital compensator, additional blocks are added:

Time-delay block: it represents the accumulated delay of the control loop minus the time delay corresponding to the modulator, i.e., the ADC delay and the calculations delay.

Limiter before the comparator of the modulator which ensures that the duty cycle is at least lower than 97%.

Note 1: when the selected sensor is "Embedded V.div." the schematic is not exported to PSIM, because this sensor is especially oriented to the analog implementation with components.

Note 2: Currently, in the case of the peak current mode control, the only available option to export the compensator is the "components" one, the s-domain and z- domain are not available yet.

Power stage and sensors

The schematic and parameters of the power stage and the sensors will be exported.

Initial conditions

The initial voltage across the output capacitor and the initial current through the inductor will be exported. This way the initial transient of the simulation can be reduced.

· Export to PSIM (parameters file) 

Only the text file with the necessary parameters will be exported to a PSIM schematic previously generated. Similarly to the previous option, SmartCtrl will ask the designer to select the path of the PSIM schematic to which the parameters file must be exported. Then the designer will have to select the exporting options (compensator exporting way, power stage and sensors and initial conditions).

· Update parameters file 

Once one of the previously described options has been configured, only the updating of the existing parameter file is needed. When the designer clicks, the previously inserted parameter file will be updated automatically.

1.15.1.3 Export transient responses

Navigation: SmartCtrl > Import and Export > Export >

Export transient responses

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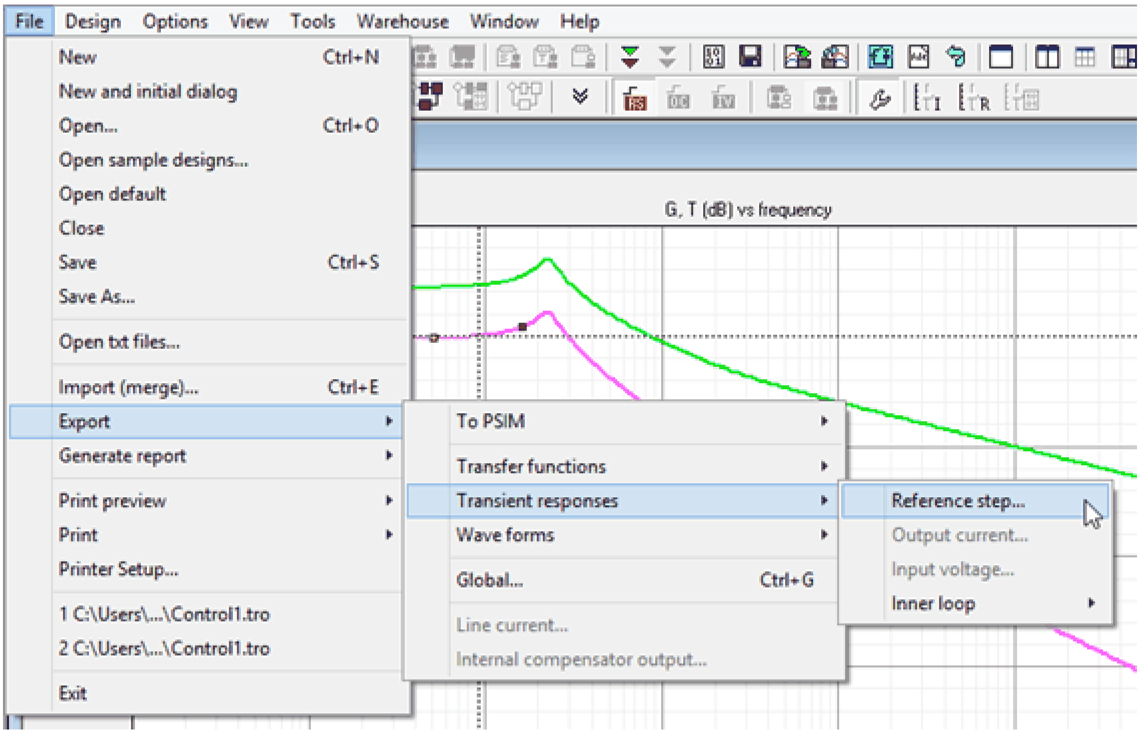
SmartCtrl provides three different exporting options which are available under the export item of the **File Menu**. The third of the exporting options is "export transient functions" which export any of the available transient responses to a file.

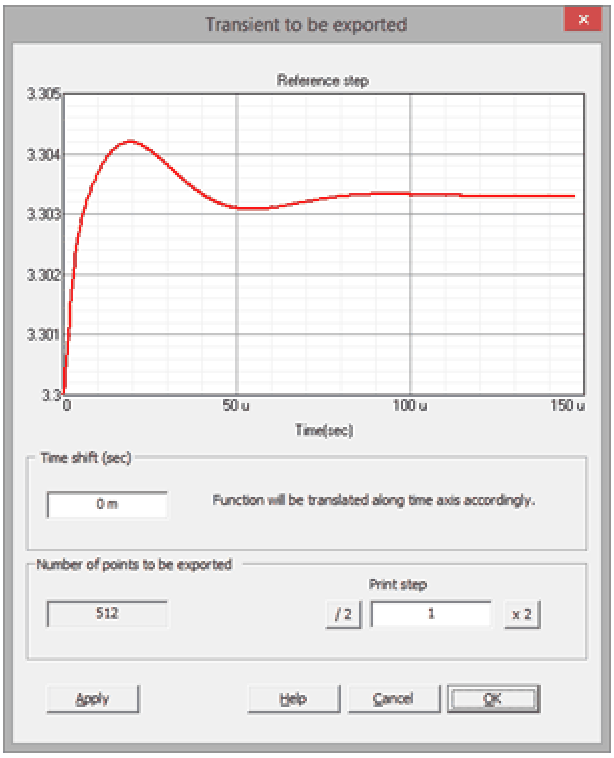


This option is also available through right click on the transient response graphic panel. The corresponding dialogue box is displayed below. It shows the transient response to be exported as well as the following parameters:

Time shift The user is able to set a customized time shift (in seconds) if necessary, and the transient response will be translated accordingly along the time axis.

N. of points to be exported SmartCtrl shows the total number of points of the graph.

Print step Its default value is 1 and it means that every data point will be exported to the file. If it is 4, only one out of 4 points will be saved. This helps to reduce the size of the resultant file. The two buttons placed at both sides of the pint step box allow to increase (x2) or decrease (/2) the print step easily.



Click Apply to update the parameters and OK to continue. At this point, the program will ask you the name and location of the file.

1.15.1.4 Export global

Navigation: SmartCtrl > Import and Export > Export >

Export global

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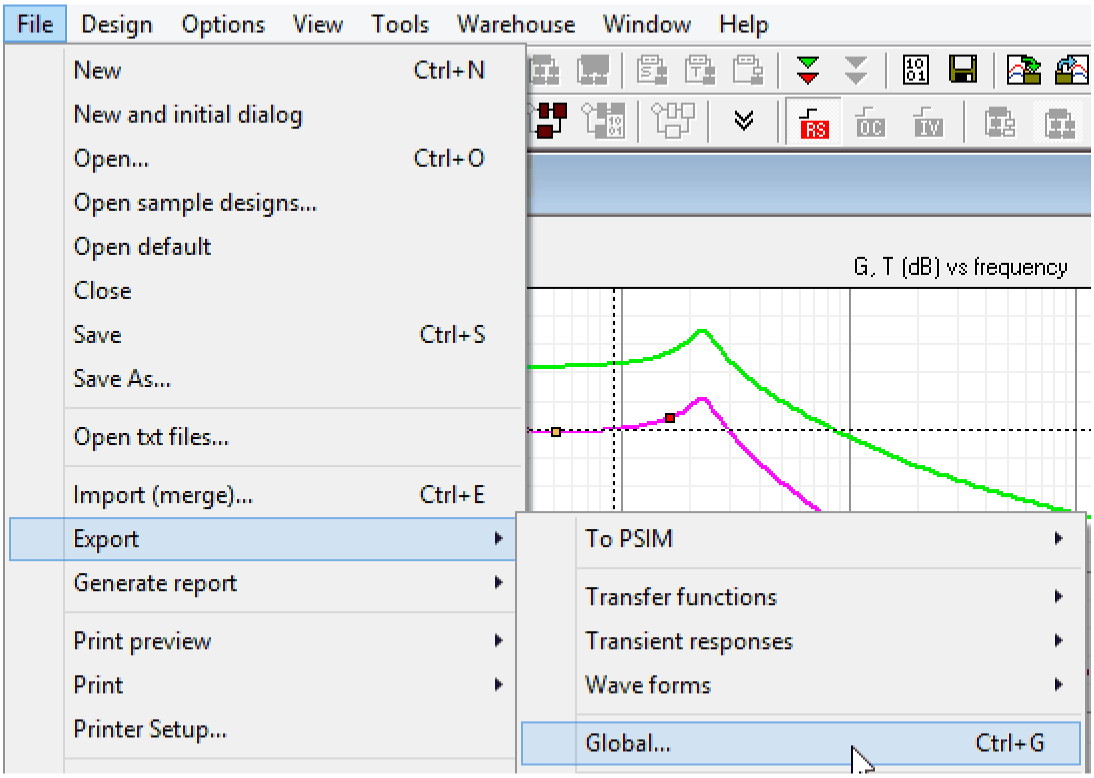
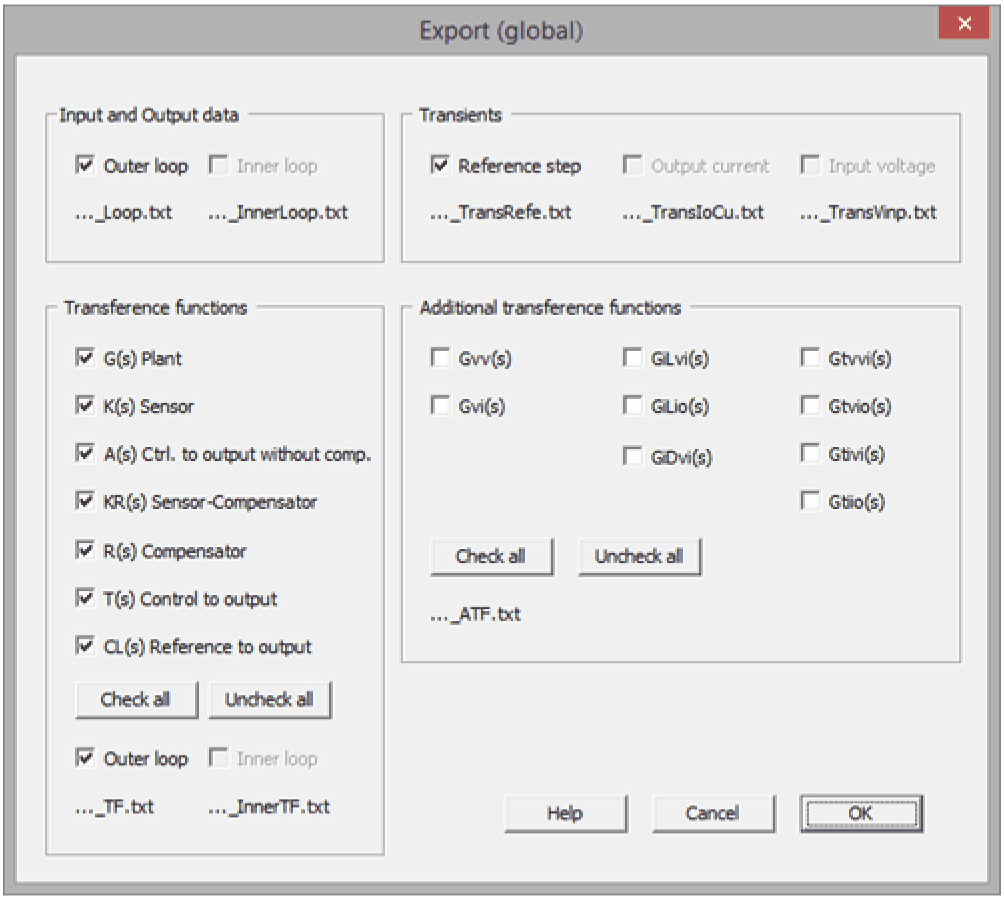
From the File menu it is possible to select Export Global.



This option allows the user to export to text files different information regarding the design. Depending on the selected information, the text files will have different names, shown below the corresponding check boxes.



It is possible to export the following information:

Input and output data of the design.

Transients: time (s) and magnitude (V or A) of a transient step.

Transference functions: frequency (Hz), magnitude (dB) and phase (deg) of the basic transfer functions.

Additional transfer functions: frequency (Hz), magnitude and phase (deg) of additional transfer functions, like audiosusceptibility, impedances, etc.

The designer is asked to configure the file format for the transference functions, like in Export transfer functions.

Finally, the user is asked for the path to save the file/s.

1.15.1.5 Export waveforms

Navigation: SmartCtrl > Import and Export > Export >

Export waveforms

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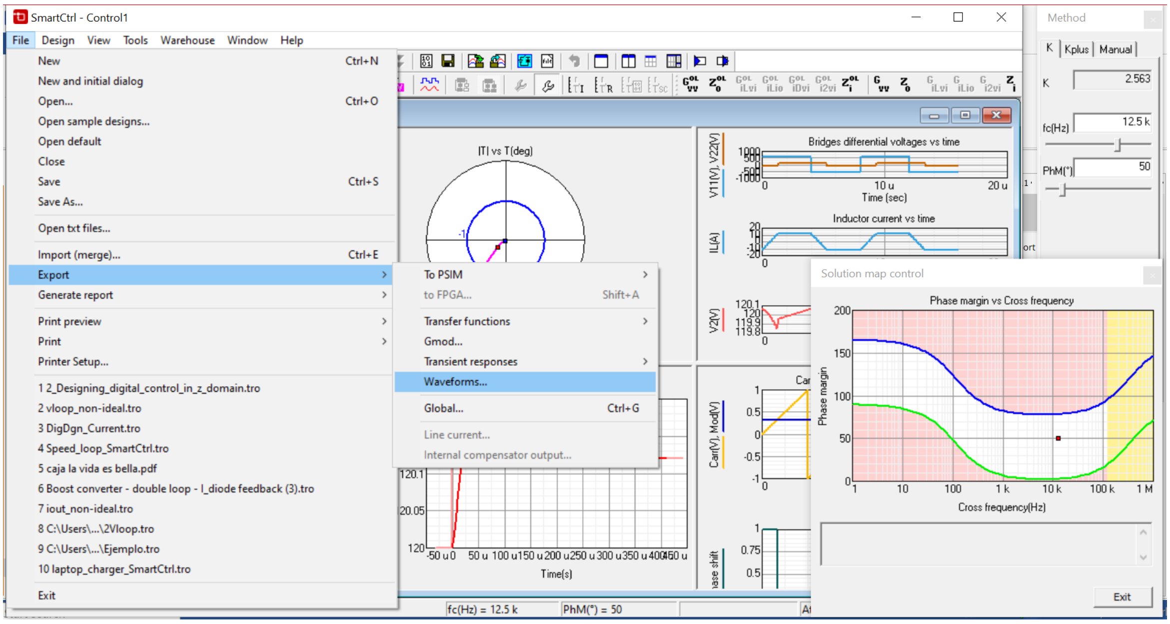
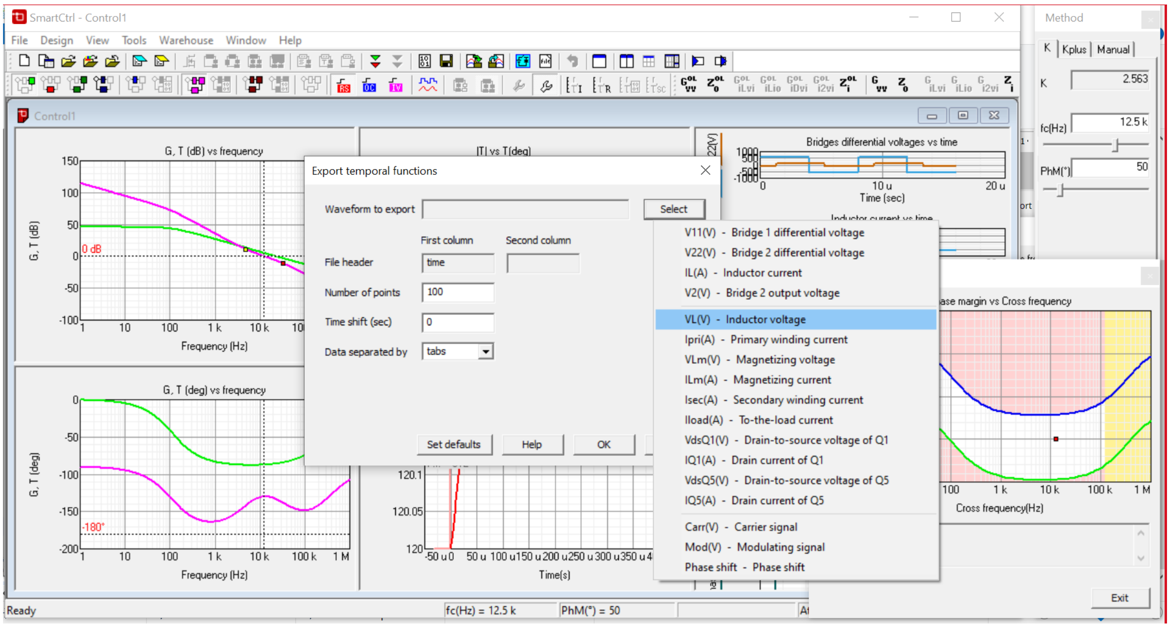
SmartCtrl provides three different exporting options which are available under the export item of the **File Menu**. The third of the exporting options is export waveforms.

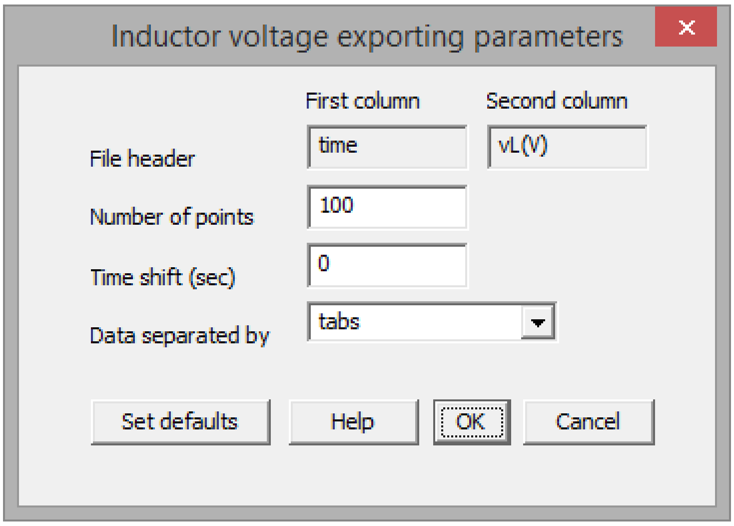


Any of the waveforms available can be exported to a .txt file. To do that, the designer must select the signal to be exported within the available list and set the options of the file in the corresponding dialogue box.



The addressed file is formed by two columns containing the time in seconds and the current/voltage instantaneous value, respectively.

The file options and characteristics are described below:



File Header	It contains the name of the two columns of the file.
Number of points	Number of points to be saved in the file
Time shift (sec)	The user is able to set a customized time shift (in seconds) if necessary, and the transient response will be translated accordingly along the time axis.

Data separated by: tabs
spaces
commas

1.15.1.6 Export to FPGA

Navigation: SmartCtrl > Import and Export > Export >

Export to FPGA

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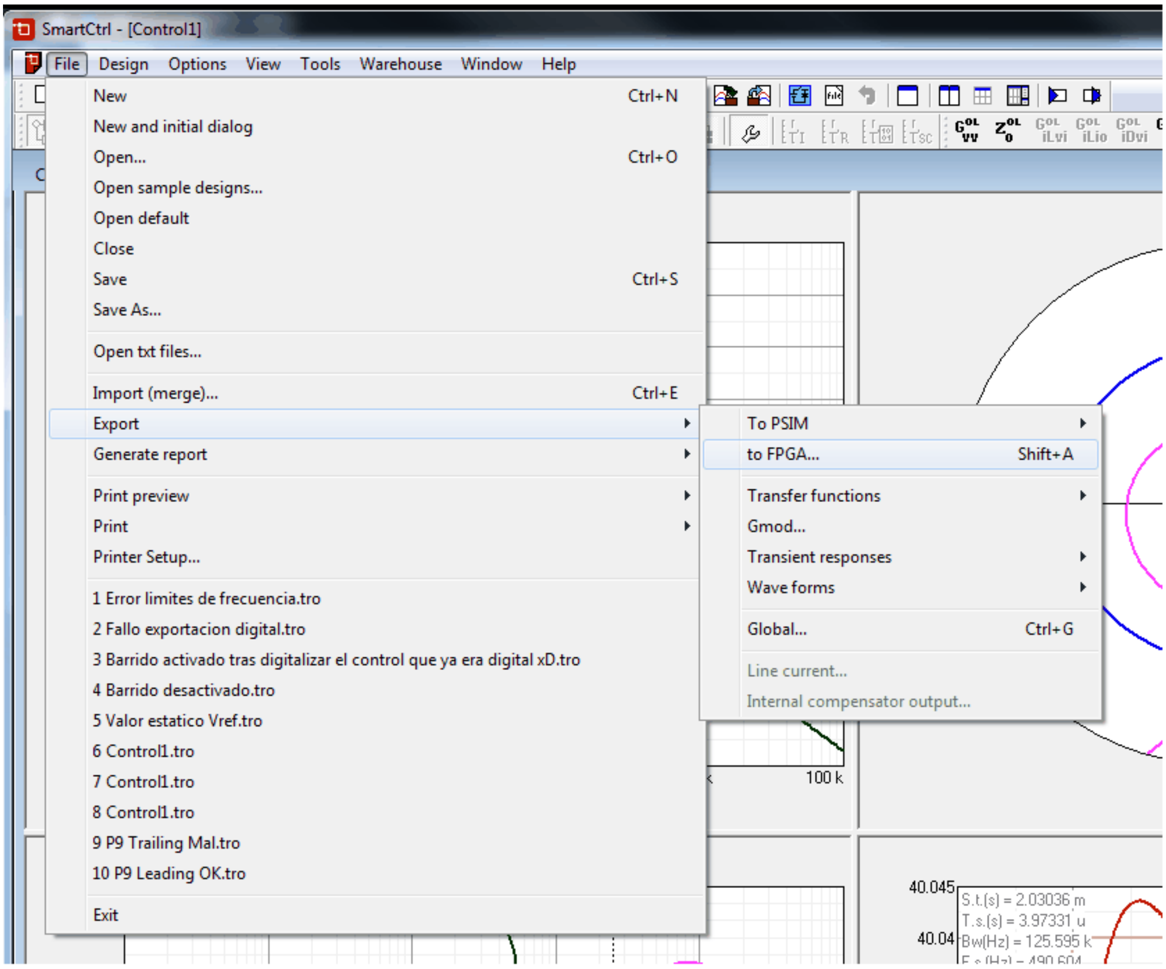
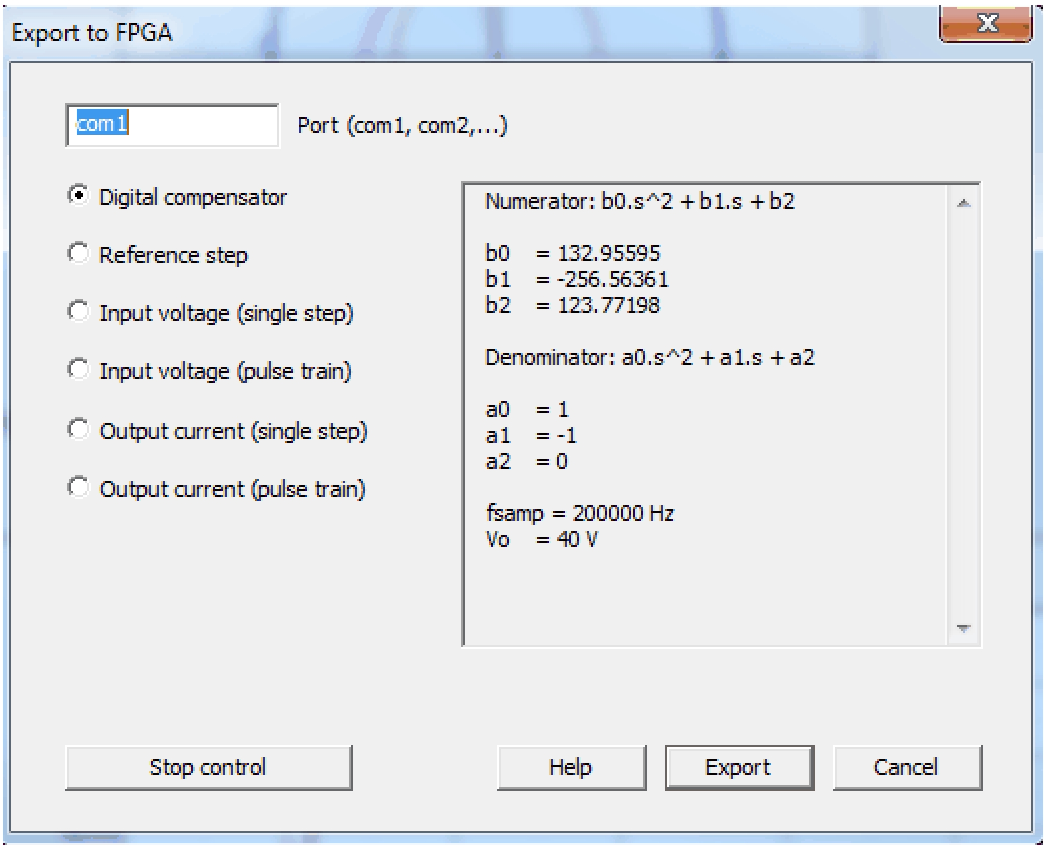
When a digital compensator has been designed, it can be directly exported to an FPGA by clicking on File Export -to FPGA (Shift+a).



When clicking on it, a new window will appear:



The options on this window are (the window will change explaining every selected option):

•Port: PC port at which the FPGA is connected.

•Digital compensator: just the compensator is exported to the FPGA.

•Reference step: a step is done in the reference value, defined as a percentage.

•Input voltage (single step): a step is done in the input voltage, from 100% to 78%, defined by its time duration.

•Input voltage (pulse train): several steps are done in the input voltage, from 100% to 78%, set by the frequency of these pulses (1/period), the duty cycle and the number of pulses.

•Output current (single step): a step is done in the output current, from I max to I min, set by its duration.

•Output current (pulse train): several steps are done in the output current, set by the frequency of these pulses (1/period), the duty cycle and the number of pulses.

Once the option is selected, it can be exported to the board by means of the export button, and it can be stopped with the Stop Control icon.

1.15.2 Import (Merge)

Navigation: SmartCtrl > Import and Export >

Import (Merge)

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Import (Merge) data of another file with the data of the existing file for display. The curves of these two files will be combined. The Merge function is available within the File Menu and through click on . It **is oriented to the comparison of frequency response curves (Bode plots)**.

The file to be merged with the current one can be either a .tro file, a .txt file or a .fra. This is, the comparison of the current file results can be compared with the results previously saved by the SmartCtrl Program, with any transfer function saved in a .txt format or with a PSIM frequency AC analysis, respectively.

Neither the .tro file or the .fra file need to be formatted in order to be used by the merge function. However, if a .txt file is going to be used the following considerations must be taken into account:

The file must be organized in three columns (from left to right)

First column corresponds to the frequency values

Second column correspond to the module in dB

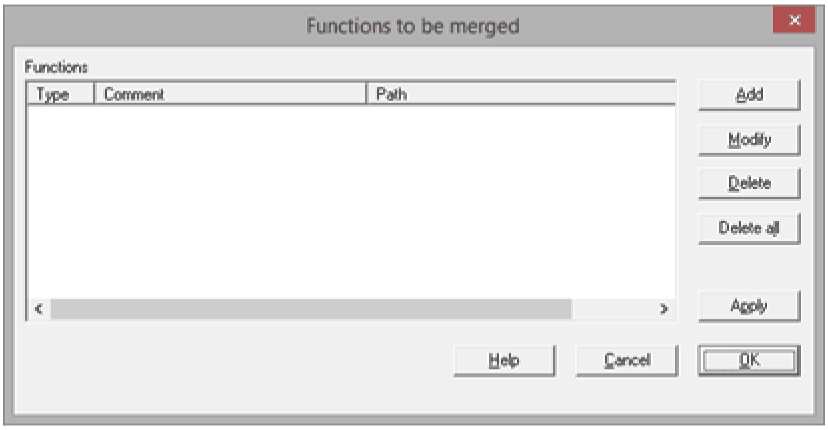
Third column correspond to the phase in degrees

The first line of the file corresponds to the columns headings

The next steps will guide you to add, modify or delete transfer functions to/from the comparison, either from a .tro file or a .txt file.

1. Merge

You can select the Merge function both from the File Menu or through left click on  from the main toolbar.



2. Available actions

You can choose among the following available actions:

Add	Adds a new transfer function to the comparison
Modify	Modify the settings of a previously added transfer function (change color, file of origin...)
Delete	Deletes the selected function
Delete all	Delete all the functions
Apply	Apply the current settings
OK	Apply the current settings and close the merge window
Cancel	Close the Merge window but don't apply any change
Help	Display the help window

1.15.2.1 Add Function

Navigation: SmartCtrl > Import and Export > Import (Merge) >

Add Function

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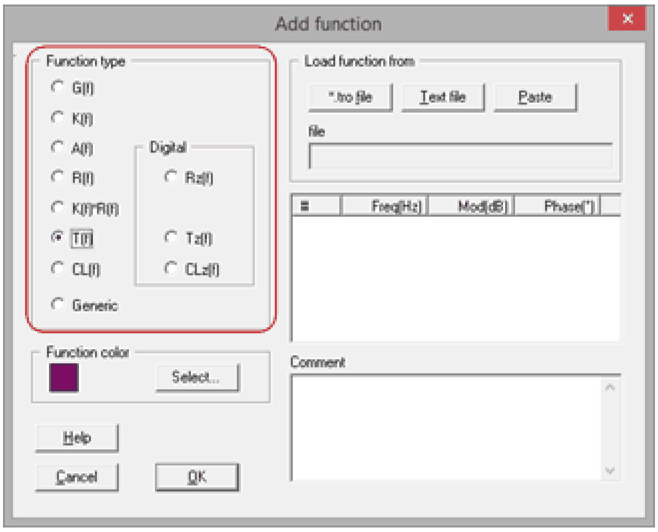
The Add function to merge allows the user to add a new transfer function to the comparison

1. Select the Function Type



Where:

G(s) Plant Transfer Function

K(s) Sensor Transfer Function

A(s)=G(s)*K(s)

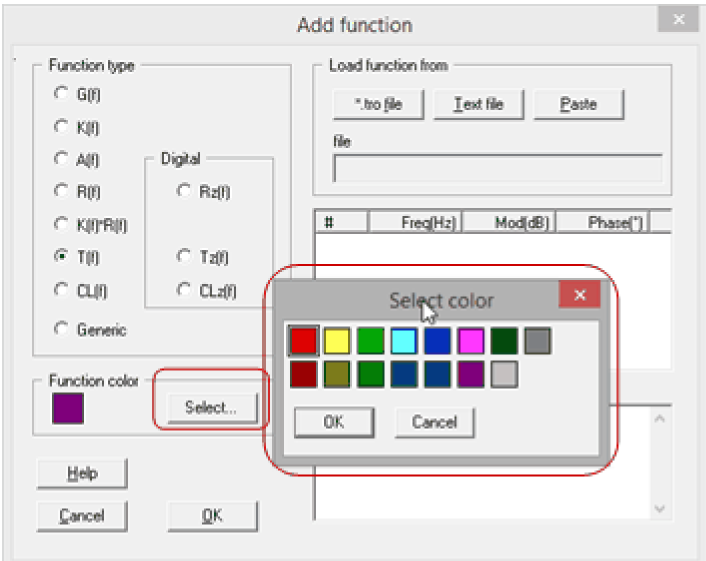
R(s) Regulator Transfer Function

K(s)*R(s)

T(s)=A(s)*R(s) Open loop transfer function

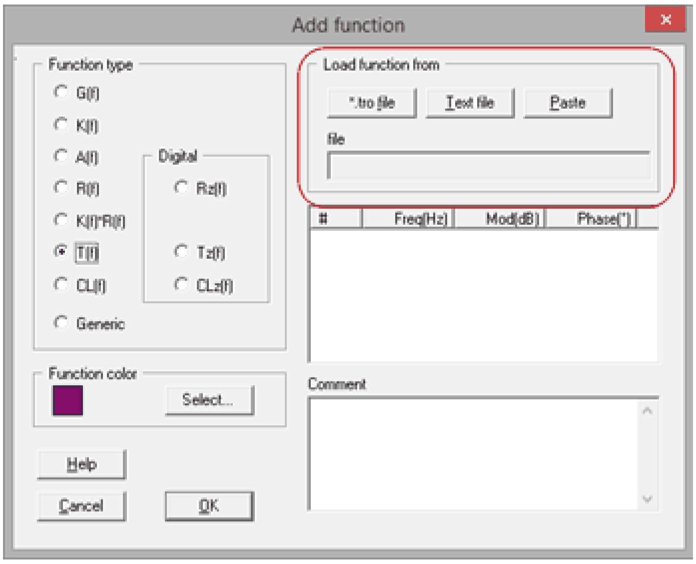
CL(s) Closed loop transfer function

2. Select the color



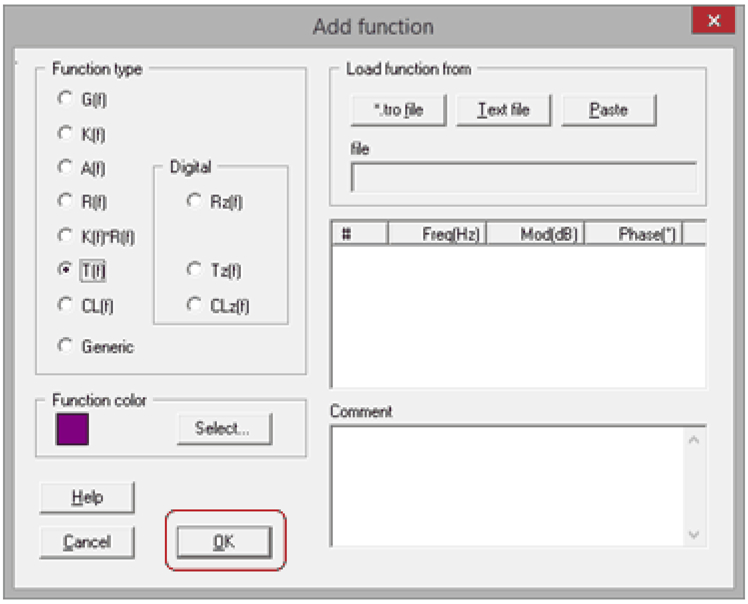
3. Load function from .tro or .txt file

Load function from either a .tro file or a text file (.txt)



4. OK

And the transfer function will be added to the module and phase panels of the Bode Plots



1.15.2.2 Modify Function

Navigation: SmartCtrl > Import and Export > Import (Merge) >

Modify Function

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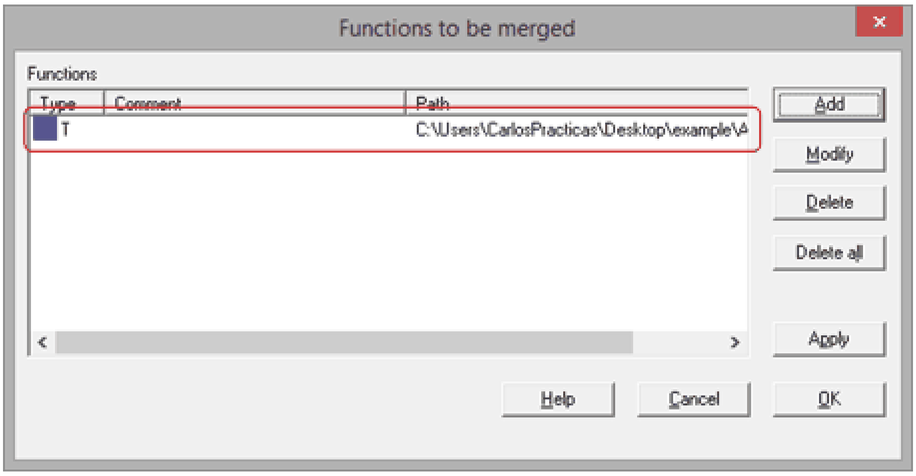
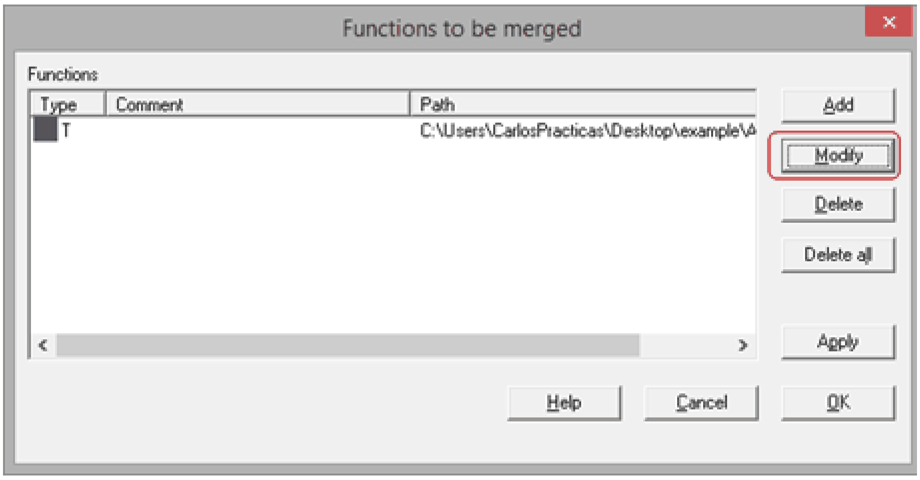
The Modify function allows the user to Modify the settings of a previously merged transfer function (change color, file of origin...)

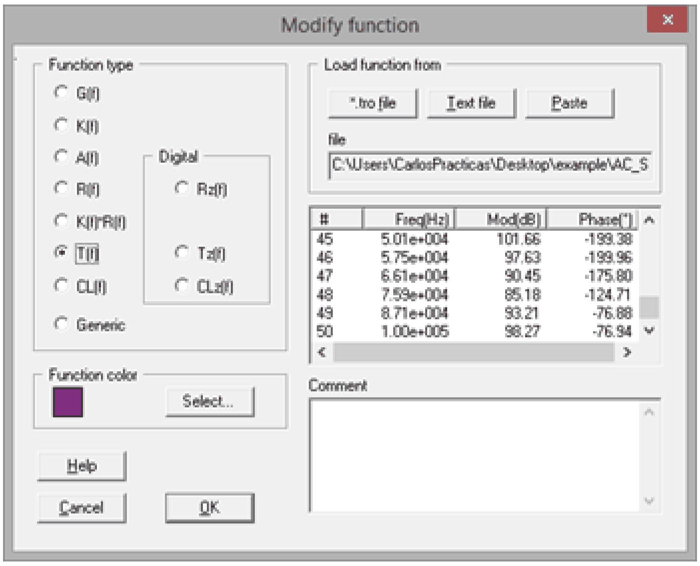
1. Select the Function to be modified



2. Click on the Modify button



3. Modify settings



The user is able to modify the following parameters:

- Load a new file
- Change the trace color

However, if the user modifies the function type, a new file must be loaded

1.16 Design Methods

Navigation: SmartCtrl >

Design Methods

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The design method box is enabled or disabled by clicking on the  icon of the **View Toolbar**.

The design method box includes the following utilities:

Design method tags

Each tag correspond to one of the three different design methods available for the regulator calculation, this is:

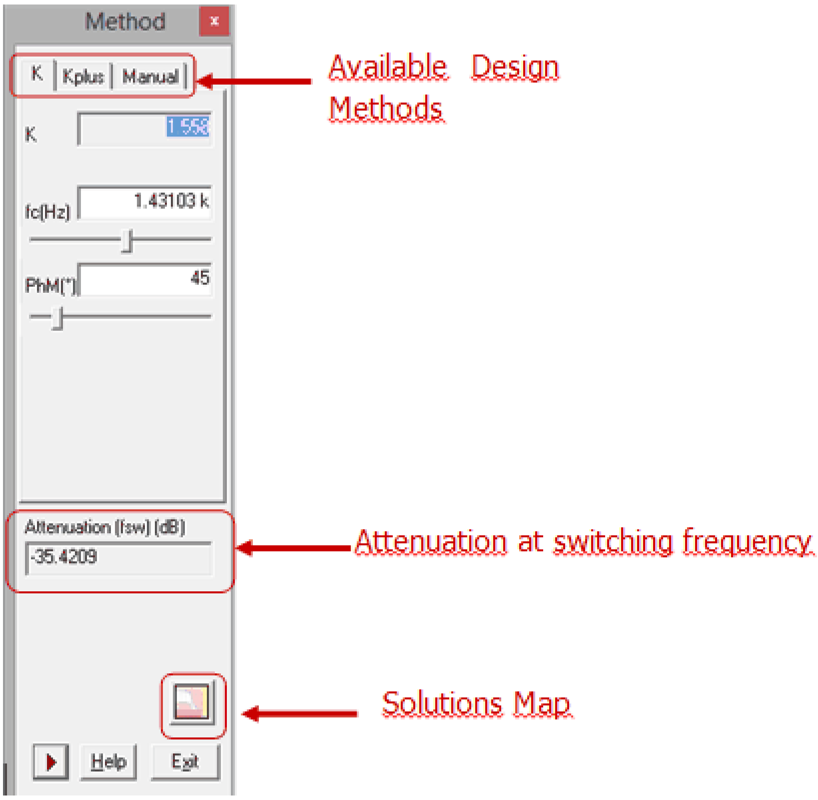
- **K-method**
- **K plus method**
- **Manual**

Attenuation at switching frequency

This output box displays the attenuation achieved by the open loop transfer function at the switching frequency.

Solutions map

Based on the selected plant, sensor and type of regulator, the solutions map provides an estimation if the stable solutions space that lead to stable solutions. The two parameters involved are represented as PM vs frequency.



Two change the considered cross frequency and the phase margin, the designer can either change their values in the white-coloured boxes, use the sliders or just click on a different point within the solutions map.

1.16.1 K-factor method

Navigation: SmartCtrl > Design Methods >

K-factor method

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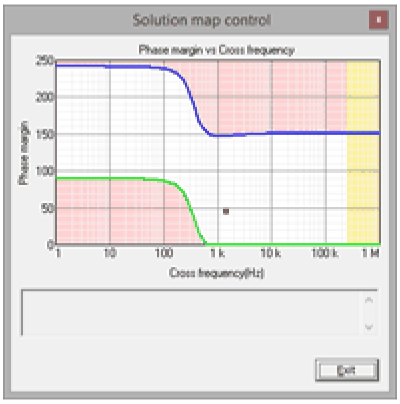
The **K factor** allow the designer to **choose a particular open loop cross-over frequency and phase margin**, and then determine the necessary component values to achieve these results. In SmartCtrl, the regulator component values are displayed within the **results text panel**.

The two input parameters of the K factor (f_c, PM) can be easily changed in the K method tag of the design method box.

They can be also modified by clicking on the **solutions map** and the K method will recalculate the regulator to fit the new values. Remember that the stable solutions area is the white one.



In SmartCtrl it is possible to use the K method for both, the Type 2 and Type 3 regulators.

K factor for Type 3 regulator

A Type 3 regulator is formed by two zeroes, two poles and a low frequency pole. When a Type 3 regulator is chosen, the K factor method assumes that a double pole and a double zero must be placed to design the compensator.

The double zero is placed at $\frac{f}{\sqrt{K}}$ frequency

The double pole is placed at $f\sqrt{K}$ frequency

Where K is defined as the ratio of the double pole frequency to the double zero frequency and the frequency f is the geometric mean between the frequency of the double zero and the frequency of the double pole.

So, the maximum open loop phase boost is achieved at frequency f, and it is assumed that the regulator is designed so that the open loop cross-over occurs at frequency f also.

K factor for Type 2 regulator

A Type 2 regulator is formed by a single zero, a single pole and a low frequency pole. When a Type 2 regulator is selected the pole and the zero are placed as follows:

The zero is placed at $\frac{f}{K}$

The pole is placed at $f \cdot K$

Where the K factor is defined as the square root of the ratio of the pole frequency to the zero frequency and *f* is the geometric mean of the zero frequency and the pole frequency.

The maximum phase boost from the zero-pole pair occurs at frequency *f*, and it is assumed that the regulator is designed so that the open loop cross-over occurs at frequency *f* also.

1.16.2 Kplus method

Navigation: SmartCtrl > Design Methods >

Kplus method

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The **Kplus method** is based on the **K-factor** and the **inputs** are the same:

- The desired cross-over frequency (f_c)
- The target phase margin (PM)

However, unlike K-factor method, cross-over frequency is no longer the geometric mean of the zeroes and the poles frequencies.

The Kplus method provides an additional design freedom degree with respect to the conventional Kfactor method, since the Kplus method places the double zero frequency f_z a factor α below f_{cross} ($f_z = \frac{f_c}{\alpha}$) and the poles a factor β above f_{cross} ($f_z = f_c \cdot \beta$).

Where α is set from f_{cross} and phase margin. This parameter allows the designer to select the exact frequency in which the zeroes will be placed. After that, β is automatically calculated.

The additional degree of freedom obtained with Kplus can be used as follows:

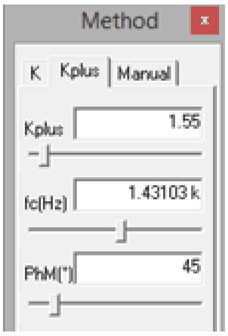
· *If α is set to be lower than K* (from the K-factor method), higher gain at low frequencies but less attenuation at switching frequency (f_{sw}) are obtained.

· On the contrary, *if α is set higher than K* (from the K-factor method), the control loop has less gain at low frequency but more attenuation at f_{sw}. It should be remarked that the phase margin is the same in all cases.

· When *α is equal to K,* both methods are equivalent.

Therefore, the Kplus method can be used to improve the overall performance of the control loop in those cases where a slightly larger high frequency ripple could be admitted at the input of the PWM modulator.

In the same way as the K method, when the Kplus tag is selected, the user can easily change the input parameters, phase margin and cross-over frequency And also an additional parameter, Kplus, which corresponds to the aforementioned α factor.



They can also be modified by clicking on the **solutions map** and the Kplus method will recalculate the regulator to fit the new values. Remember that the stable solutions area is the white one.

1.16.3 Manual

Navigation: SmartCtrl > Design Methods >

Manual

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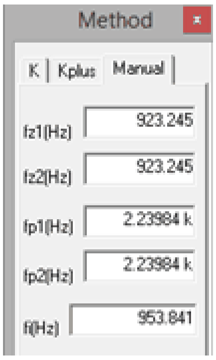
This method allows **placing poles and zeroes independently from each other**. It is used when the designer would like to refine the results obtained from the K and Kplus methods or when these automatic methods do not provide a valid solution.

The manual method is provided for both the type 3 and type 2 regulators. Their poles and zeroes frequencies can be varied by directly dragging and dropping them in the **Bode plots**.

Or typing the frequencies of poles and zeroes in corresponding input boxes of the design methods box.



In the case of a **Type 3 regulator**, the designer can adjust the frequency values of:

The two zeroes,

The two poles

And the low frequency pole

In the case of a **Type 2 regulator**, the available frequencies are:

The zero

The pole

And the low frequency pole

1.16.4 PI tuning

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PI tuning

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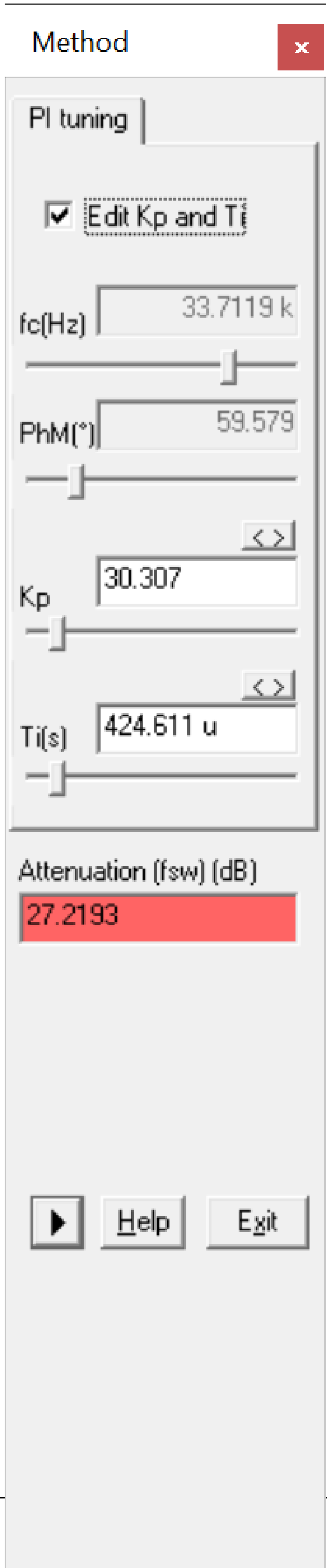
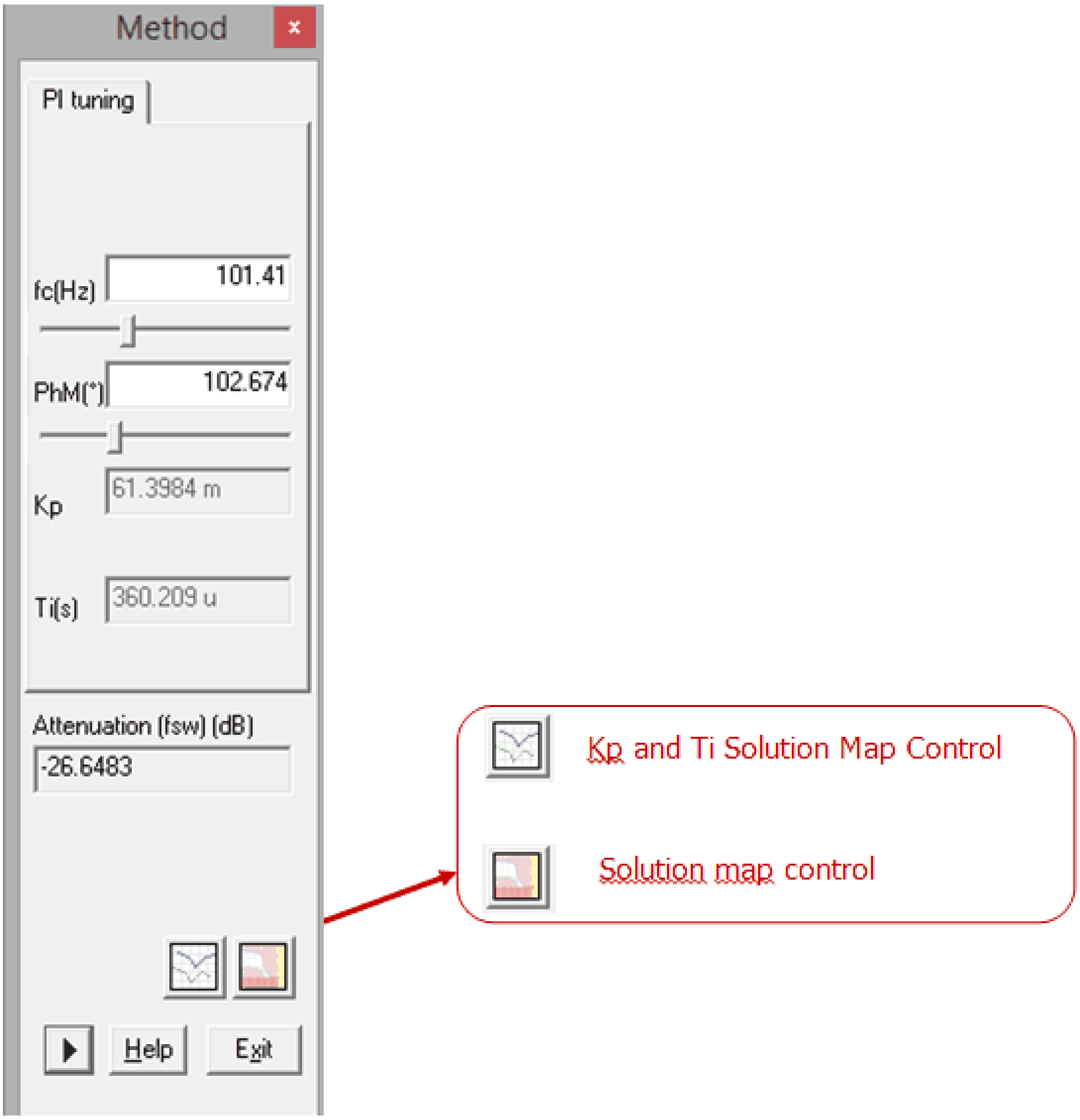
With the PI tuning method the input parameters that can be modified are:

Phase margin & Cross-over frequency

Selecting the option "Edit Kp and Ti" directly adjust the PI compensator parameters (NEW in version 5.0).


Method
PI tuning
Edit Kp and Ti
fc(Hz)
33.7119 k
PhM(°)
59.579
Kp
30.307
Ti(s)
424.611 u
Attenuation (fsw) (dB)
27.2193
Help
Exit

When selecting the Phase margin & cross-over frequency SmartCtrl calculates the both the proportional (Kp) and integral (Kint) gains and shows them in the corresponding output boxes.



The same as in the other automatic calculation methods, the phase margin and cross-over frequency can be set directly by clicking in the solutions map.

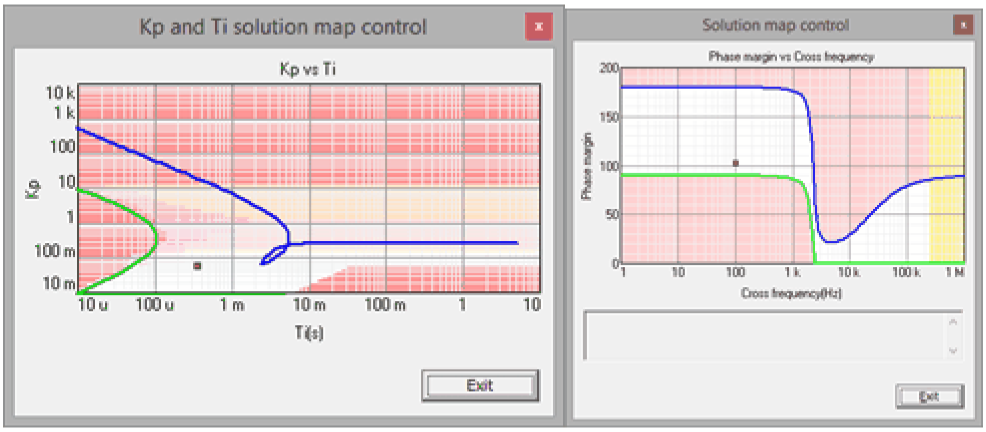
Additionally, there is a **Kp and Ti Solution Map** that allows the tuning of the PI regulator by

directly tuning its parameters Kp and Ti.

A Proportional Integral controller (PI) is defined by the following transfer function:

$$G(s)=Kp\cdot\frac{1+Ti\cdot s}{Ti\cdot s}\quad where\begin{cases}Kp\text{:is the Gain of the PI controller.}\\ Ti\text{:is the time constant of the PI controller, in seconds.}\end{cases}$$

The constant time Ti is located on the x-axis of the graphic and the gain Kp is placed on the y-axis. Any change will involve an instantaneous update of the rest of the windows of the **graphic panel**, as well as in the **solution map**.



Every point in the recommended area of the **Solution Map** box has an equivalent point in the **Kp and Ti Solution Map** control box, which is also expected to be stable. However, several points of the **Kp and Ti Solution Map** control box might correspond to an unique point in the **Solution Map**.

Since there many possible combinations of Kp and Ti that lead to a compensator with the same dynamic performance, some areas of the **Kp and Ti Solution Map** control box have been colored in order to avoid a complex definition of the relationship between points of the **Kp and Ti Solution Map** control box and **Solution Map** box.

The recommended design space corresponds to the white area in between the green and the blue lines. These lines represent the limits of the set of Kp and Ti variables that correspond to feasible PI regulators. The rest of colored regions represent a weighted average of gain margin, phase margin and attenuation. Red region has to be avoided. Yellow and pink area in between the green and the blue lines correspond to feasible compensator which attenuation at switching frequency is higher than 0 dB.

1.16.5 Single Pole tuning

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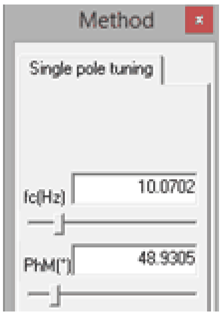
Single Pole tuning Previous Top Next

The **I tuning** method is the equivalent of the manual method but for integral regulators.

The simple integrator is formed by a single pole, which frequency must be selected by the designer. Given this frequency, the associated phase margin is automatically calculated by the program.



The solutions map of an integrator is a single line that represents the addition of 90º to the open loop without regulator transfer function. So, the designer can also determine the cross-over frequency by clicking in the **solutions map**, the same way as in the other design methods.

1.16.6 Method box

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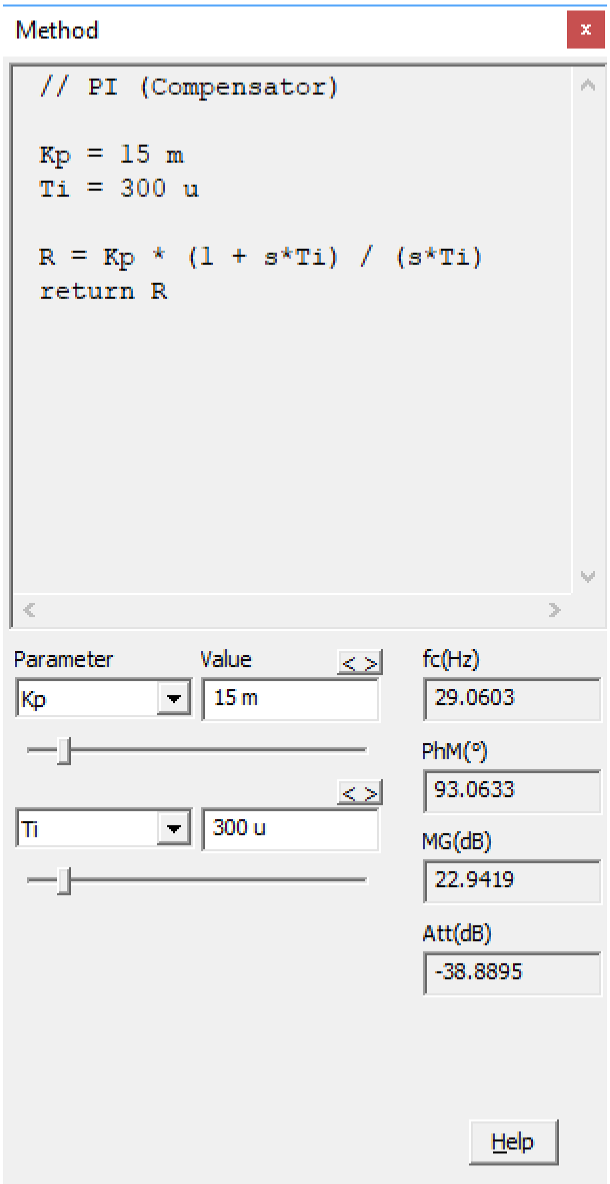
Method box Previous Top Next

In any mode when the user selects a customized compensator using the Equation Editor, the solutions map is not available.
The alternative to check the system response and stability using the graphic panels is the method box that will allow to modify the compensator parameter value with the sliders.



1.17 Parametric Sweep

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Parametric Sweep Previous Top Next

The parametric sweep can be accessed either through the **Design Menu** or the **View Toolbar** icons. The SmartCtrl program distinguish among two different parametric sweeps:

Input Parameters Parametric Sweep

It allows the variation of all the input parameters of the system. These are:

- General Data
- Plant
- Sensor
- Regulator

Compensator Components Parametric Sweep

It allows the variation of the component values of the compensator. This is, the resistances an capacitances values that conform the regulator.

1.17.1 Input parameters parametric Sweep

Navigation: SmartCtrl > Parametric Sweep >

Input Parameters Parametric Sweep

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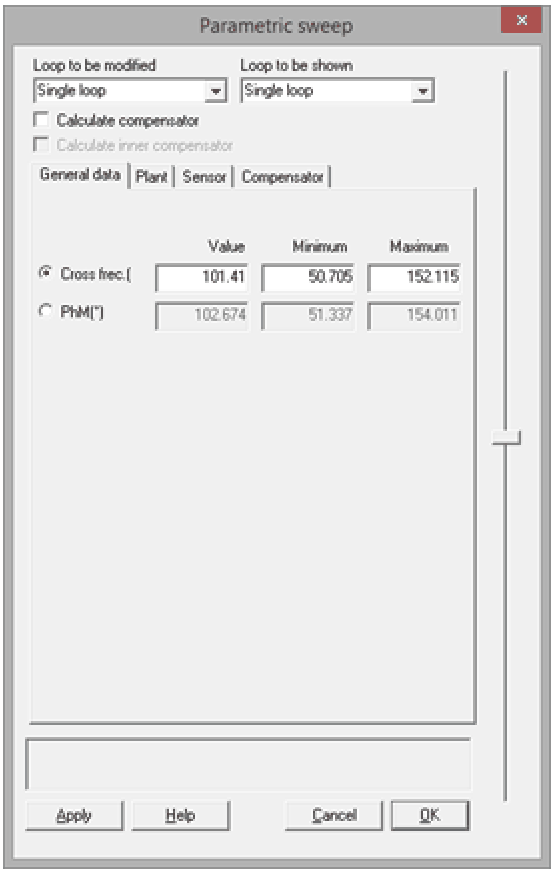
To access the **input parameters parametric sweep** the user can either click must click on the button , placed within the **View toolbar or** through the **Design Menu > Parametric Sweep > Input parameters**.

The functions available within the input parameters parametric sweep are the following:

Loop to be	Select which loop would you like to modify. This option is only available in the case of a double loop design, where the designer can select amongst the inner loop or the outer loop
Tick box	When this box is selected, the regulator is recalculated for each new set of parameters along the parametric sweep. If it is not selected, the regulator is fixed to the last one calculated

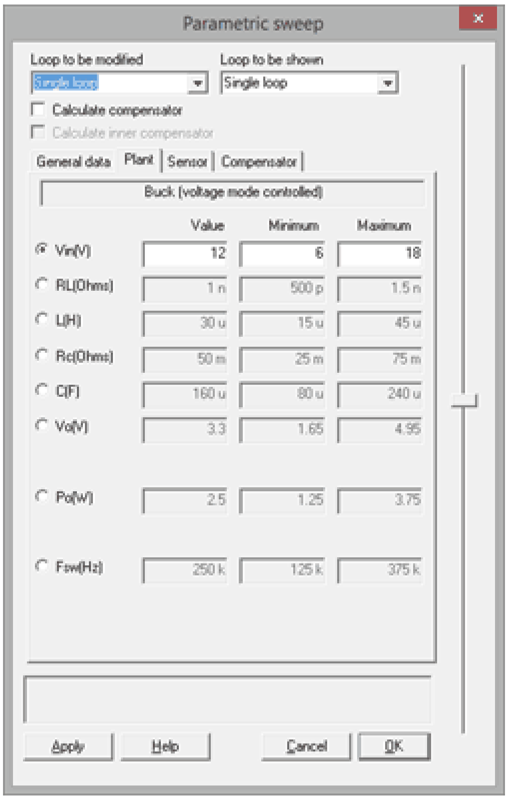
Loop to be Select which loop results would you like to display. This option is only available in the case of a double loop design, where the designer can select amongst the inner loop or the outer loop.

Tag "General Data" The parameters to be varied are related to the open loop parameters. The designer is asked to provide a range of variation. The available parameters are:



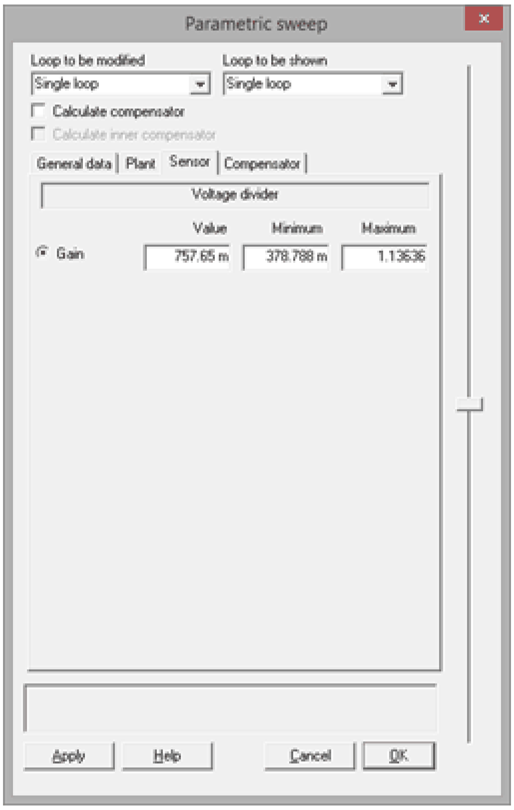
Tag "Plant"

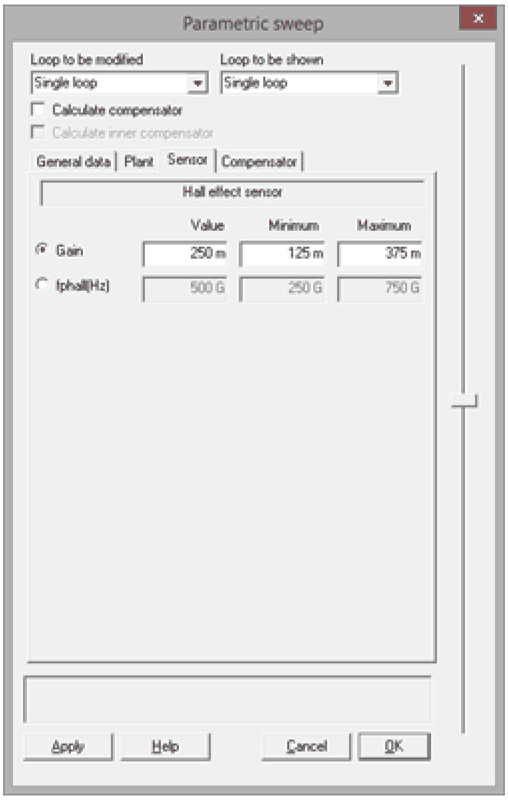
The parameters available for variation are related to the plant input parameters. The user must introduce a minimum and a maximum value for the variable selected, in order to provide its range of variation. Only one parameter can be varied at a time



Tag "Sensor"

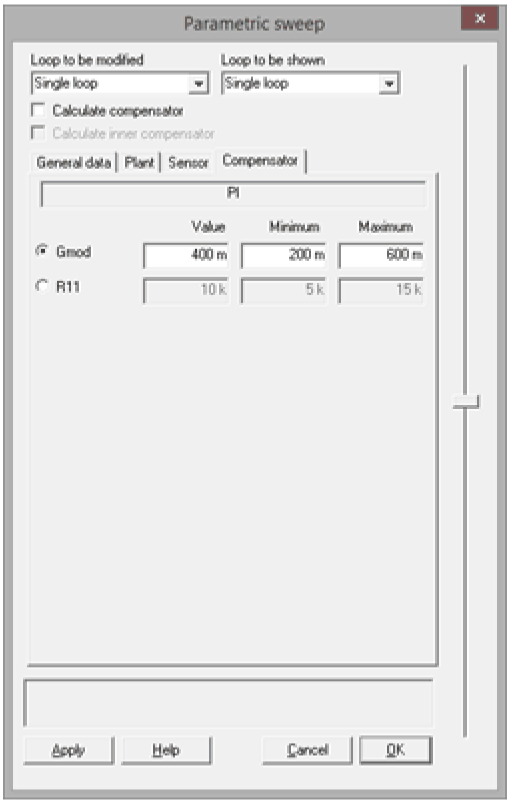
The parameters of the sensor selected for the current design will be available for variation. For instance, in the case of the **voltage divider** the parameter to be varied in the voltage divider is its voltage gain (V_{ref}/V_o). And in the case of the **Hall effect sensor**of there are two available parameters: its gain at 0Hz and the pole frequency.





Tag "Compensator"

The parameters available correspond to the modulator gain and the Resistance R11.



1.17.2 Compensator Components Parametric Sweep

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Compensator Components Parametric Sweep

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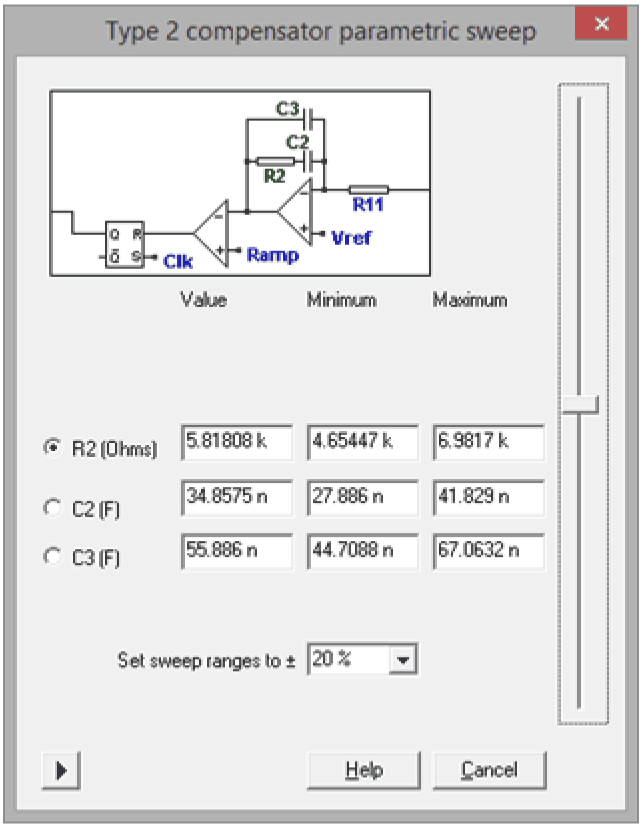
To access the **compensator components parametric sweep** the user can either click on the button, placed within the **view toolbar** or through the **Design Menu > Parametric Sweep > Compensator components**.

The compensator components parametric sweep is oriented to the variation of the resistances an capacitances values that conform the compensator. For instance, in the figure below a parametric sweep window for a type 2 is shown.



1.17.3 Source code parametric sweep

Navigation: SmartCtrl > Parametric Sweep >

Source code Parameters sweep

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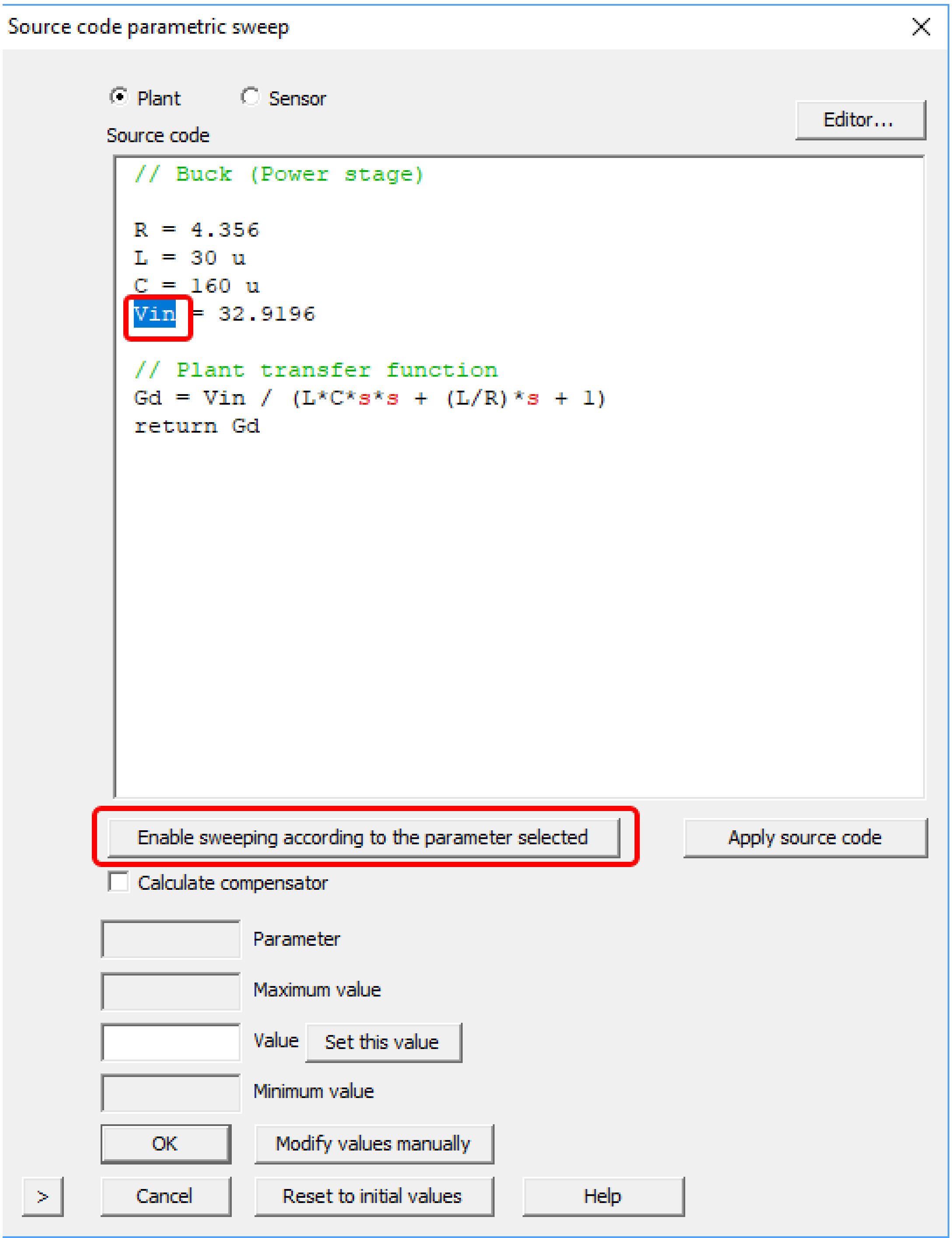
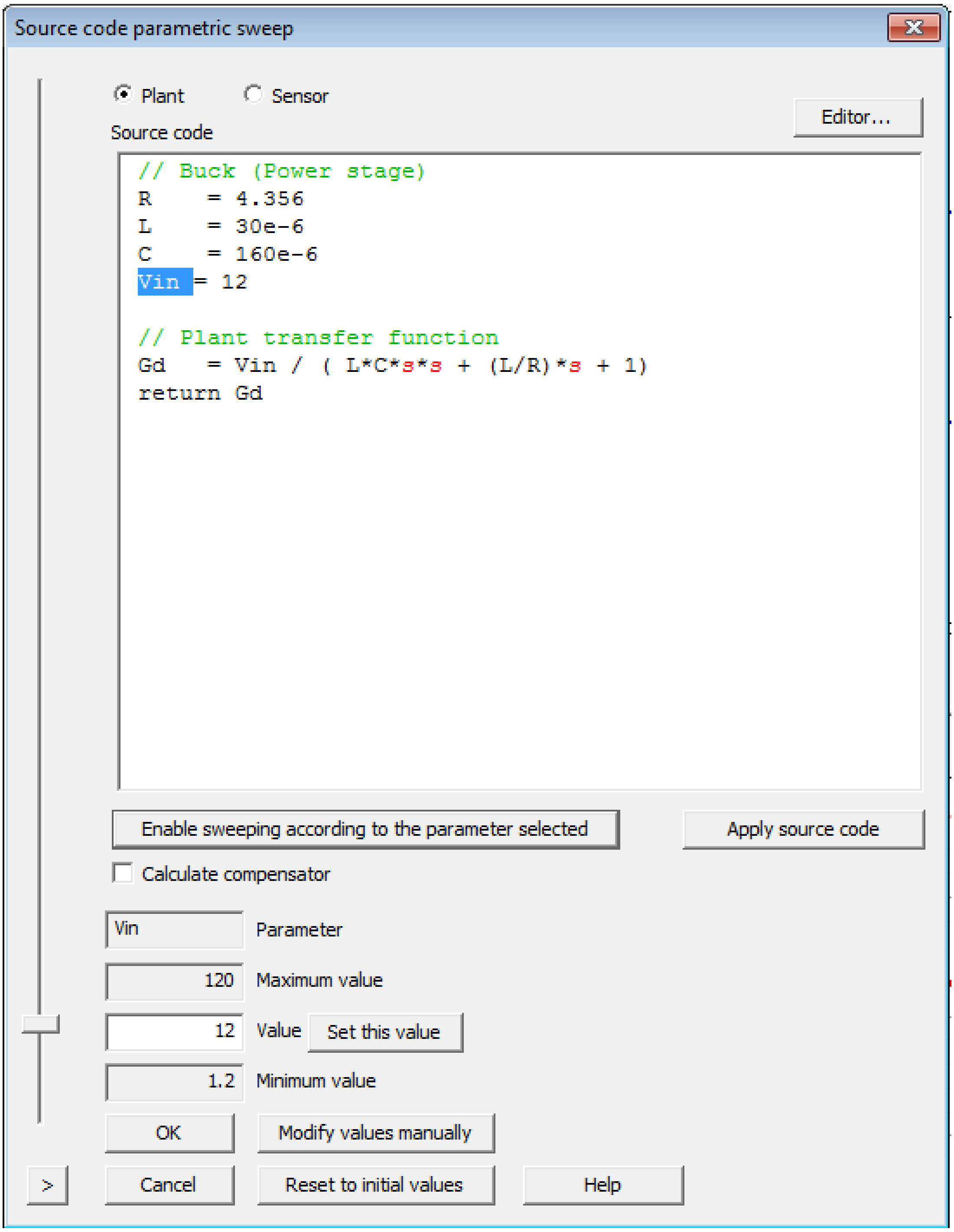
To access the source code parametric sweep the user can either click on the button , placed within the view toolbar or through the Data Menu > Parametric Sweep >Source code variables. This option is only available when the design of the topology has been done with equation editor.

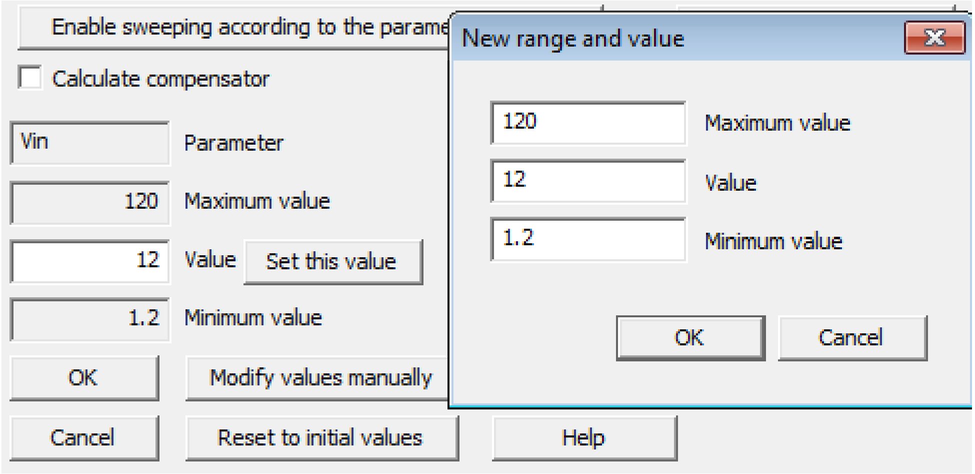
To enable the sweep, first select the variable in the source code and then click on button marked in next picture ("Enable sweeping according to the parameter selected"):



Then with the left scroll, the user can change the value of the variable between the maximum and minimum selected. The changes produced by these variations are shown automatically in the design window.



Maximum and minimum margins can be changed as shown in next picture:



Once a value is selected, the source code can be modified by clicking on *Apply Source Code.*

1.18 Digital Control

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Digital Control

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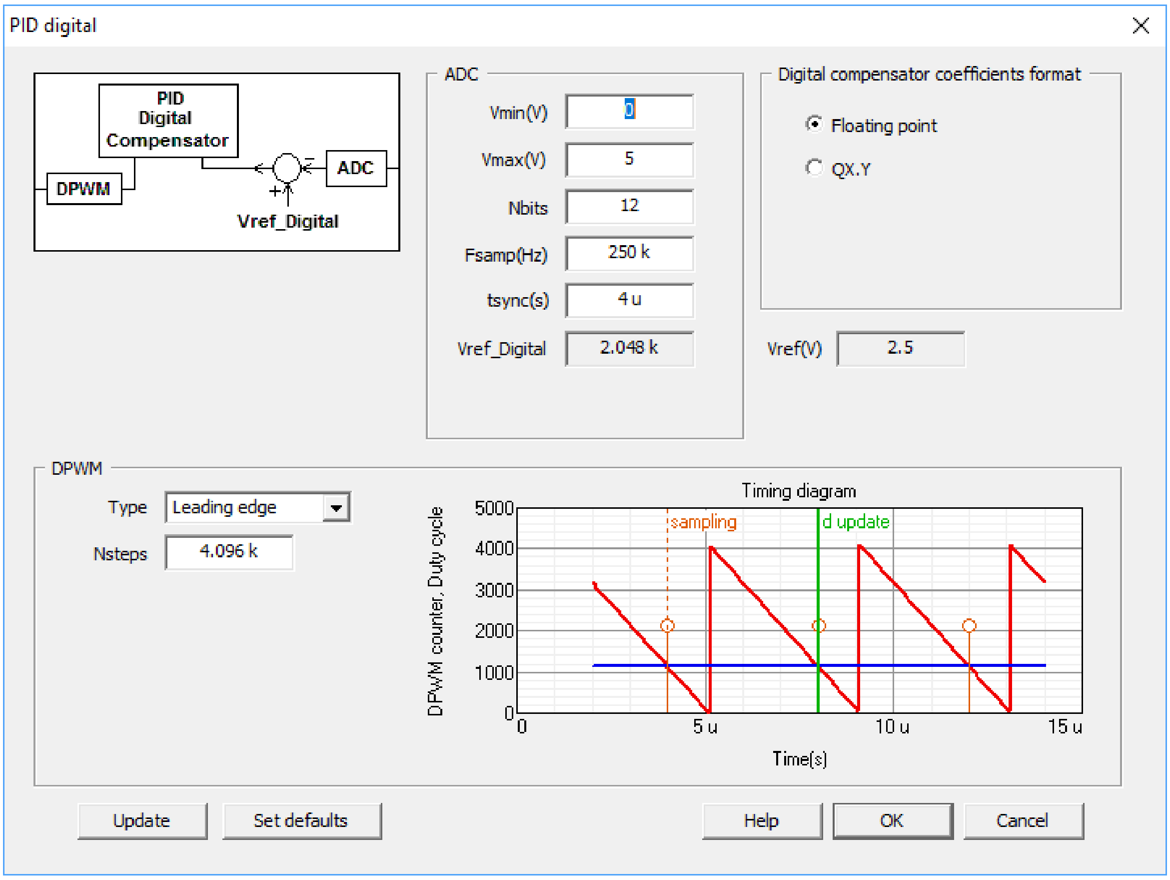
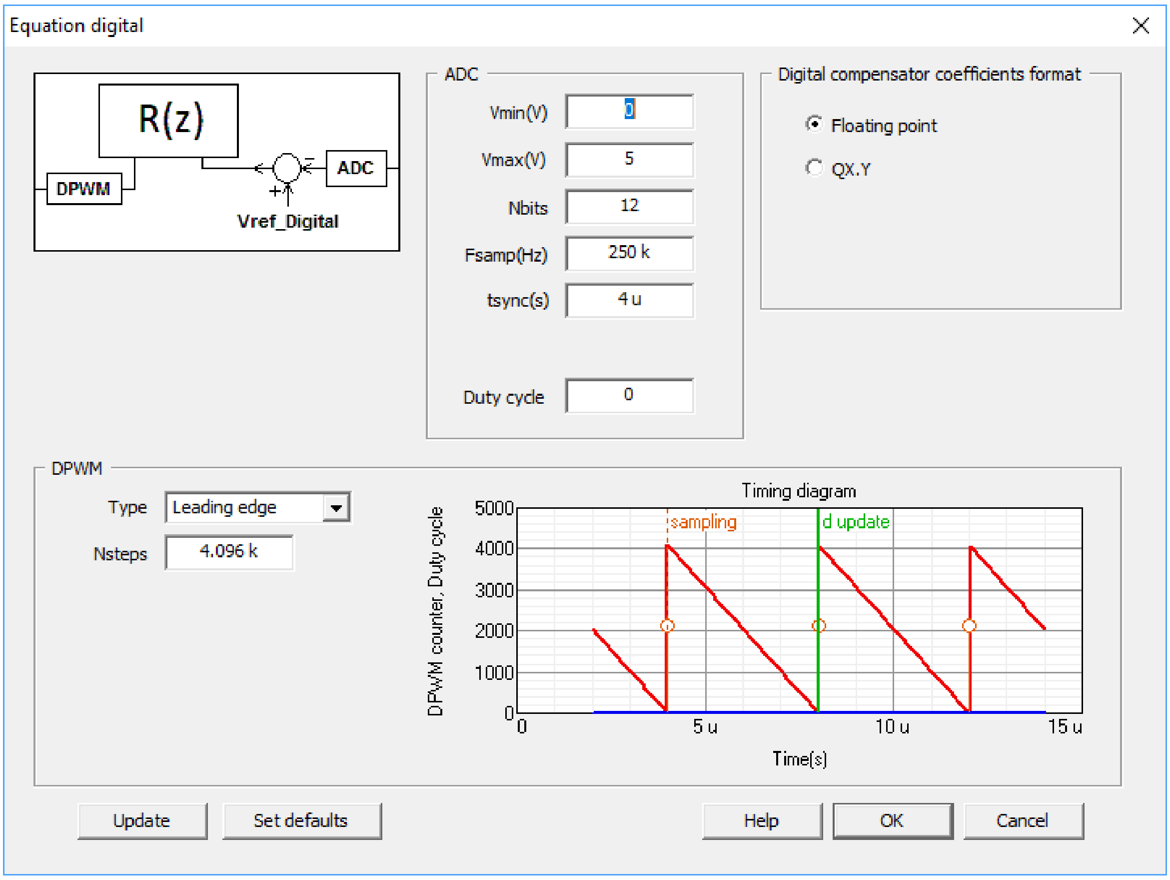
The digital control module of SmartCtrl allows the calculation of the coefficients of digital compensators in order to be implemented by means of digital devices (as specific hardware in FPGA or ASIC, or as a program in a microprocessor, microcontroller or DSP).

Digital compensators are obtained directly in z-domain, and can be exported to PSIM using z-domain blocks. SmartCtrl takes into account some specifications regarding both the controller and the ADC, which are explained below.



"**ADC and DPWM**" option when defining a customer compensator using the Equation Editor:



ADC panel:

•**Vmin(V):** minimum voltage the ADC is able to read, used to calculate its gain.

•**Vmax(V):** maximum voltage the ADC is able to read, used to calculate its gain.

•**Nbits:** Number of bits of the ADC to represent the analog input value. This number affects the calculation of the reference, as stated below.

•**Fsamp(Hz):** Sampling frequency of the digital regulator. The sampling period Tsamp=1/fsamp is the time between two consecutive samples of the output signal of the regulator.

In many applications, the sampling frequency (fsamp) of the regulator is equal to the switching frequency (fsw) of the power converter. In SmartCtrl, the user can select different values for switching and sampling frequency, but **the sampling frequency must be a multiple or submultiple of the switching frequency**.

In current loops, the controlled magnitude in the converter has a significant ripple, therefore, it is recommended to use a Hall Effect sensor that includes a first order low pass filter that can act as an antialiasing filter.

•**Vref_Digital:** Value of the reference to be followed by the digital compensator, calculated as:

$$V_{ref_{Digital}} = (ValueToBeSensed \cdot SensorGain - V_{ADCmin}) \cdot \frac{2^{NbitsADC}}{V_{ADCmax} - V_{ADCmin}}$$

•**tsync(s):** it accounts for the time difference between the moment when a signal is sampled and when it is used to update the regulator output.

Unlike in an analog controller, where the sensor is continuously measuring and the control signal is updated at every moment, when a digital compensator is implemented, the instant when a signal is measured and the instant when a change is seen by the PWM signal are not the same.

Digital compensator coefficients format:

•**Floating point:** According to the international standard ISO/IEC/IEEE 60559:2011 (with content identical to IEEE 754-2008).

•**QX.Y:** Fixed point number is represented with the QX.Y notation, X + Y bits, with X bits to the left of the fixed point (integer part, sign bit included) and Y bits after the point (fractional part).

DPWM

For the modulator note there are different options according to the waveform:

•Trailing Edge

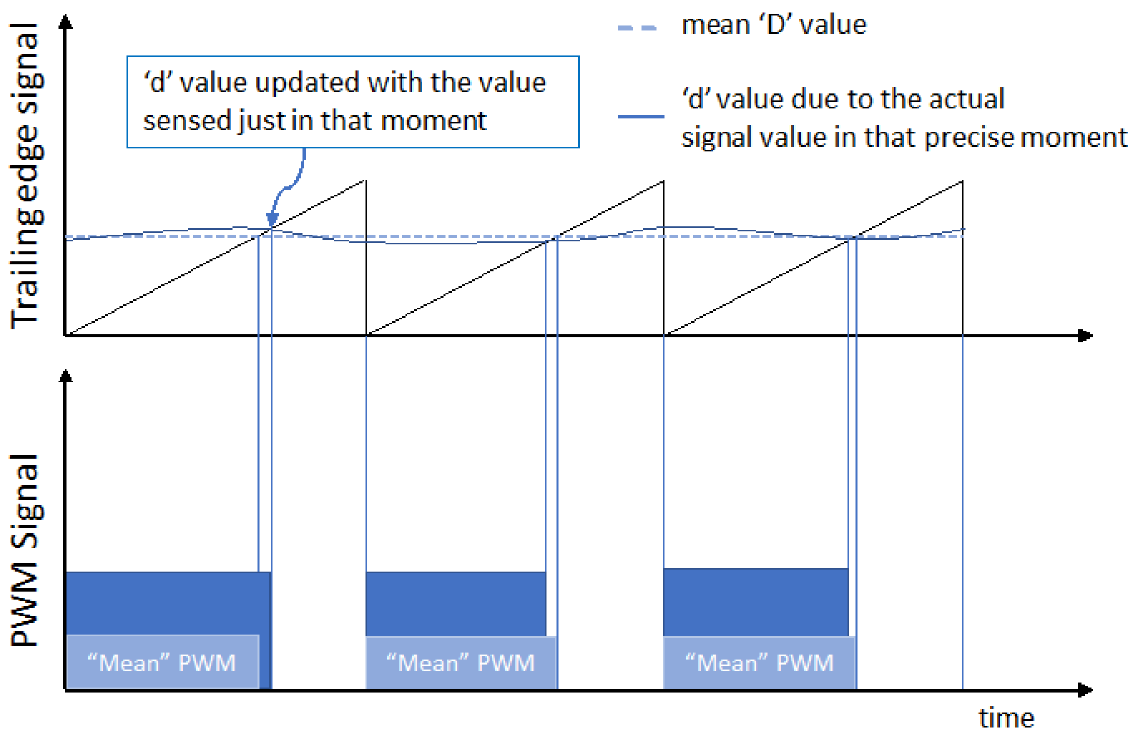
•Leading Edge

•Triangular

•Ad-hoc, defining Gmod and tdelay(s).

Analog controller:

As reference, an analog controller time stamp is presented:



Digital controller:

When implementing a digital controller, some additional parameters are taken into account:

ot_{delay}: it is the time difference between the moment when the ramp begins and the moment when a measurement is done (0 if they are the same).

o$t_{digital}$: it is the time needed by the digital system to measure an analog signal, convert it to a digital value, and make the necessary regulator calculations.

ot_{sync}: it is the time difference between the moment when a signal is measured and the moment when that measurement affects the output. This last parameter is the one to be introduced in SmartCtrl. Here some examples are presented, in order to clarify the selection of the right tsync parameter, that must be set by the user.

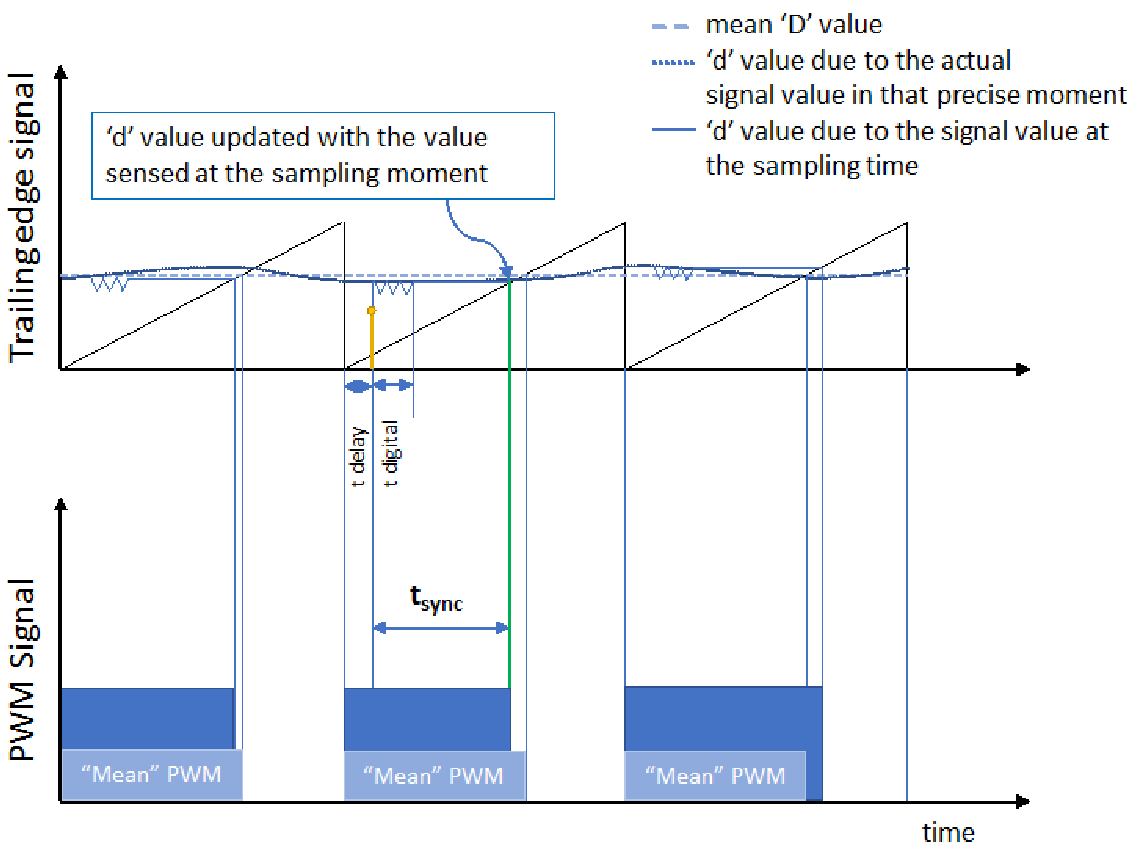
Here, some examples are presented, to ease the understanding of the different times defined.

Digital controller (fsampling ≤ fswitching)

Digital controller (Trailing edge) with $t_{digital} < t_{on} - t_{delay}$

If t_delay equals 0, the parameter t_sync equals ton, the generic expression would be:

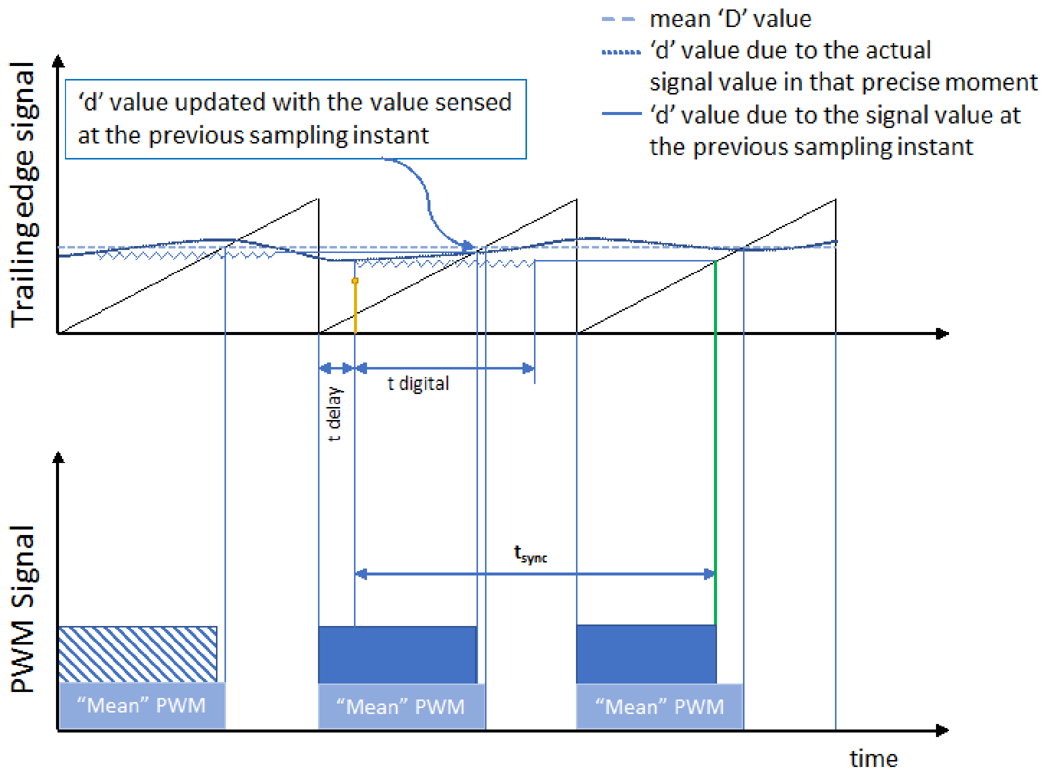
$$t_{sync} = t_{on} - t_{delay} = d \cdot \frac{1}{f_{sw}} - t_{delay}$$



Digital controller (Trailing edge) with $t_{digital} > t_{on} - t_{delay}$

This can happen if the digital circuits are not fast enough to make every calculation in the time between the measurement and the crossing with the sawtooth. In this case, the information taken does not affect the output until the next period, so t_sync takes an extra switching period:

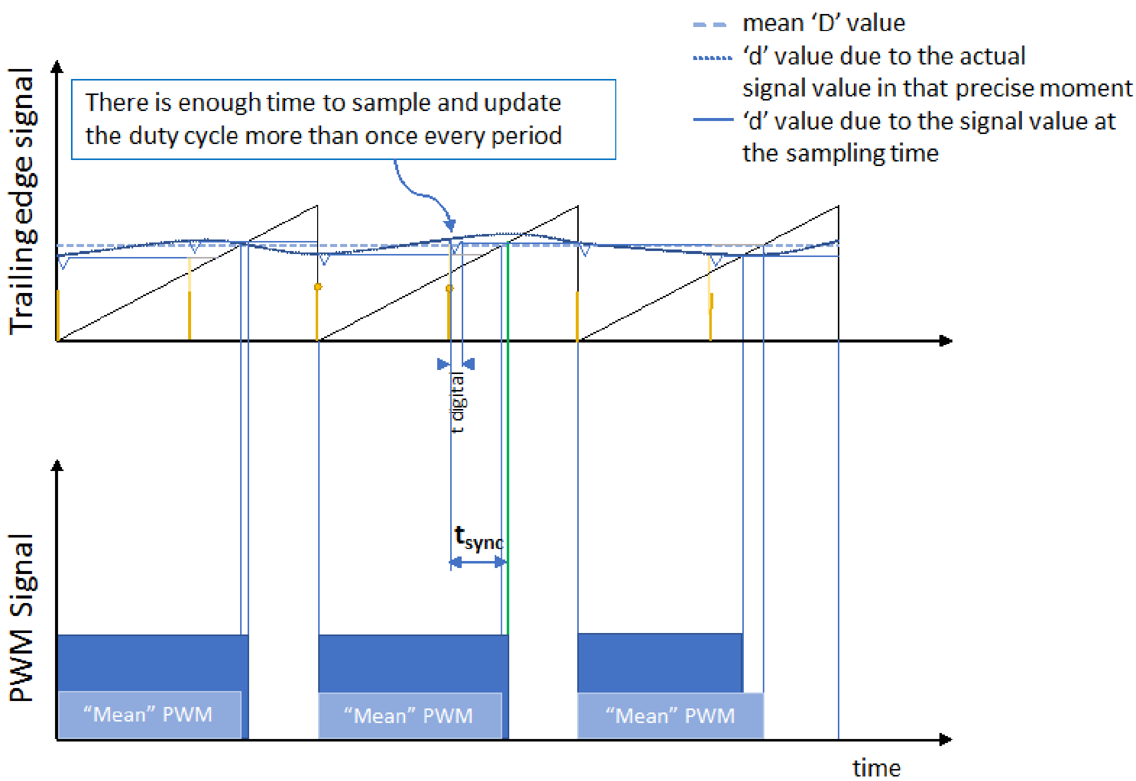
$$t_{sync} = t_{on} - t_{delay} + T = (1+d)\cdot\frac{1}{f_{sw}} - t_{delay}$$



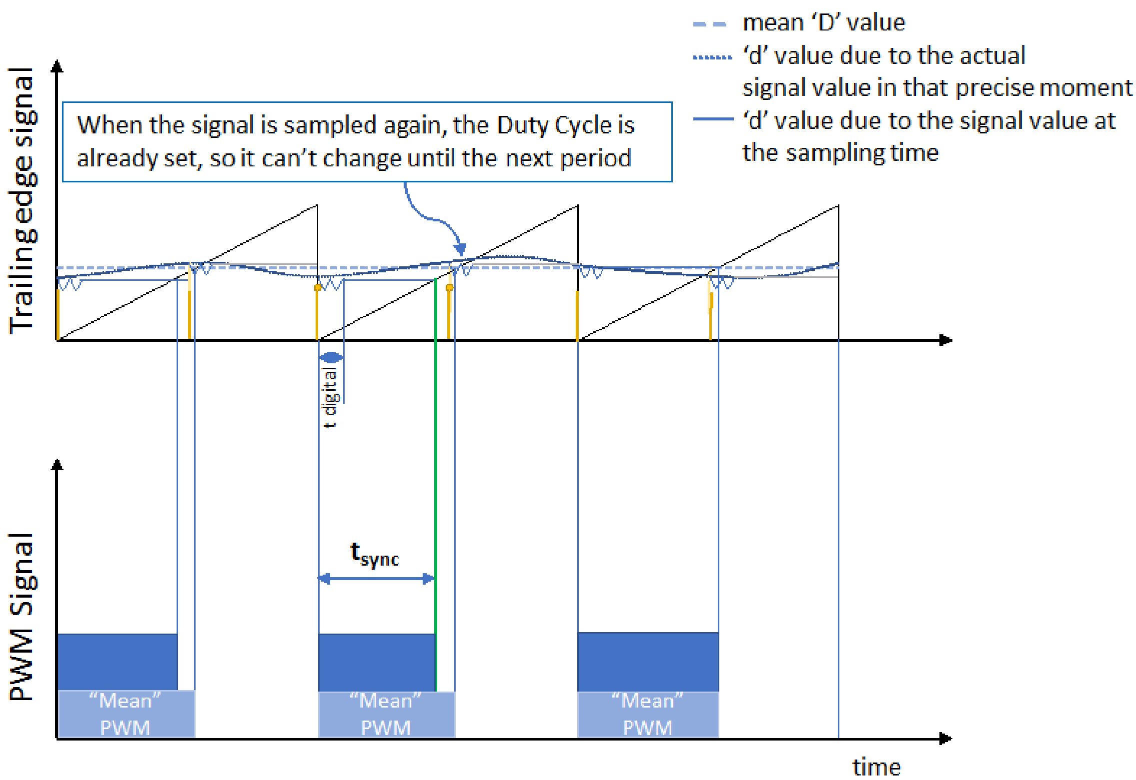
Digital controller (fsampling > fswitching)

When sampling at a frequency higher than the switching one (always a multiple), there are 2 possible scenarios:

•Every measurement has enough time to make a change in the output:



•Only some measurements are able to affect the output signal every switching period.

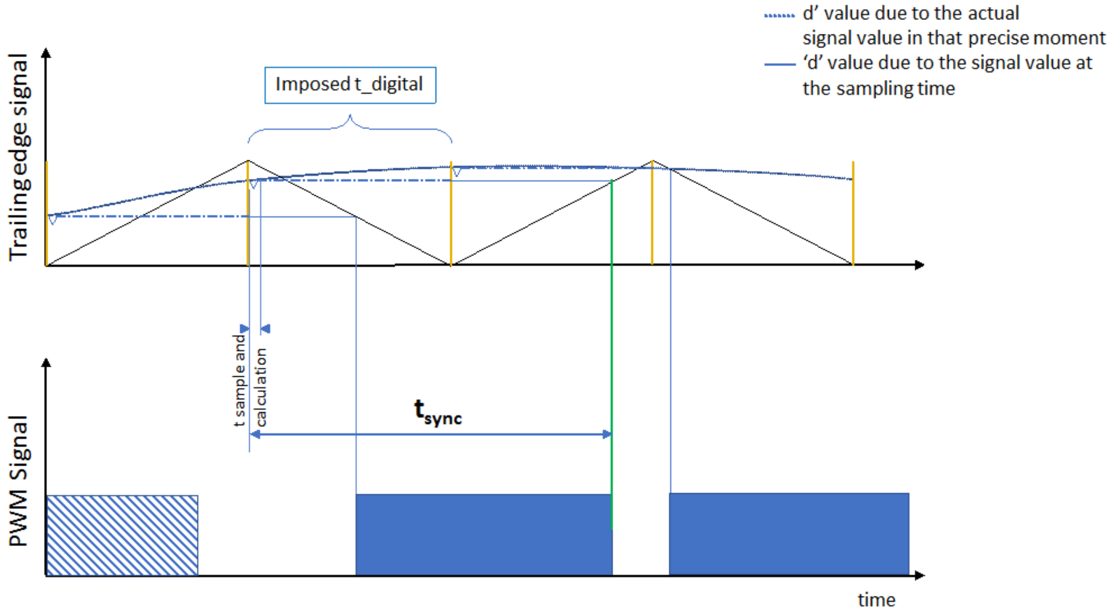


t_sync is always limited by t_digital as the lowest value, and by 1/fsw as the highest (assuming $t_{digital} < Tsw$):

$$t_{digital} < t_{sync} < \frac{1}{f_{sw}}$$

Digital controller (fsampling > fswitching) with set tdigital

Many times. A set t_digital is selected in order to have a better control over its effects. An example is presented here, usually employed to control inverters:



In this example, a minimum t_digital of one sampling period (1/2 switching period) is imposed, so tsync will always remain between T_sampling and T_switching, depending on the Duty cycle (higher T_sync the higher Duty cycle) in that precise moment:

$$T_{sampling} < t_{sync} < T_{switching}$$

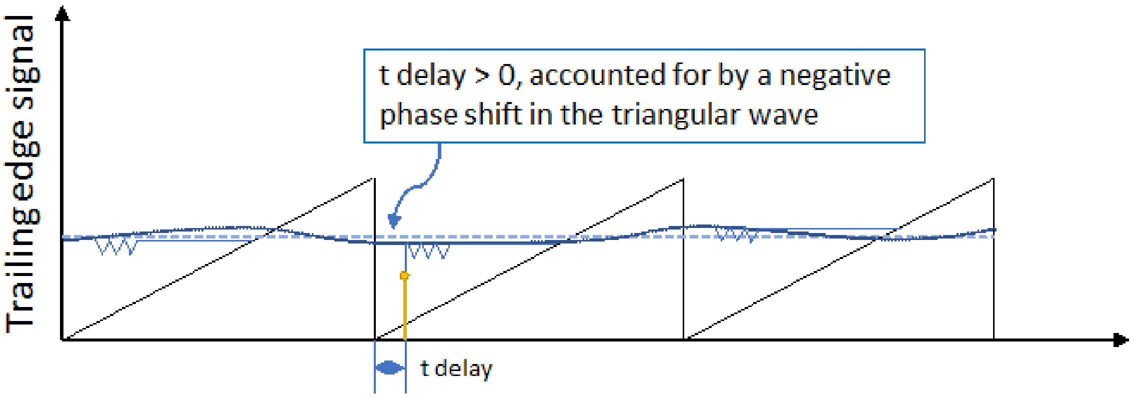
* In the case of an inverter, where the Duty cycle will vary from 0 to 1 along the sine wave, a worst-case scenario should be assumed. In this case, a Maximum Duty cycle would give the highest T_sync, so T_sync should be set to T_switching.

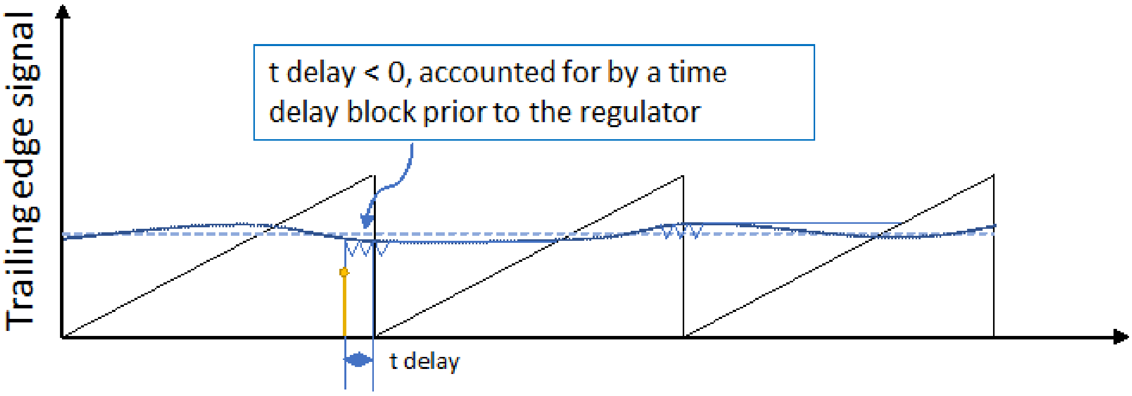
This time delay (t_sync) affects the actual phase margin obtained with the designed digital regulator. The delay is a phase that is subtracted to the phase of the open loop transfer function in the Bode plot. It is recommended to check the effect of the delay in the Bode plot of the open loop transfer function and in the closed loop transfer function.

PSIM implementation

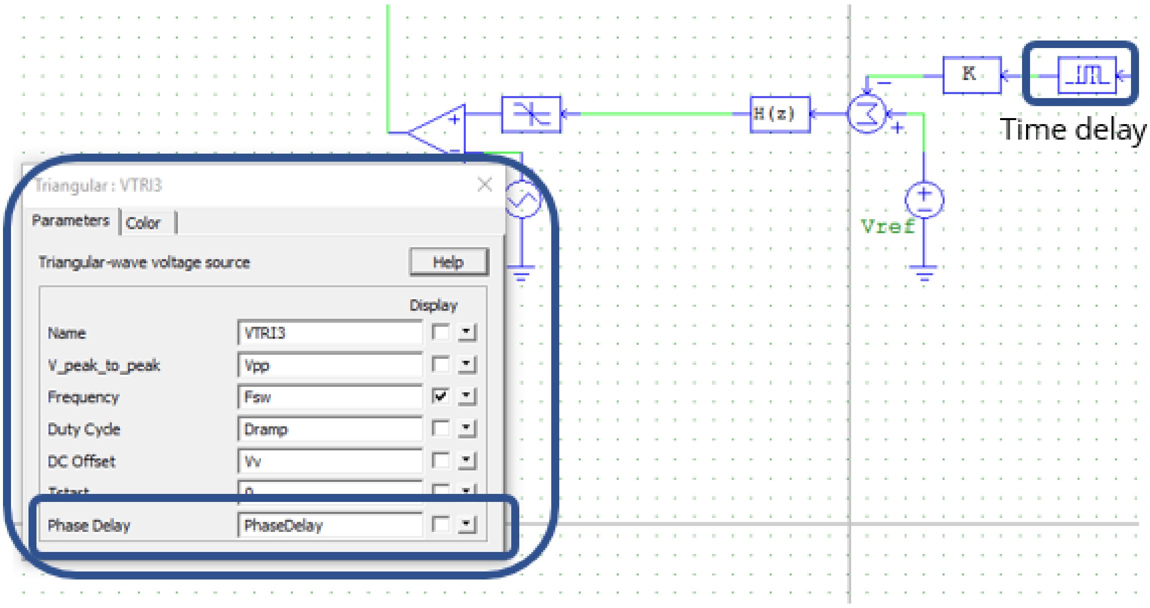
When exporting a design from SmartCtrl to PSIM, the t_delay seen in the figures above is automatically modelled in two ways (explained in the figures below):

- A time delay block is added, which accounts for t_delay when it is less than 0, that means a value is measured prior to the beginning of the ramp.
- A phase shift is added to the ramp, so values are measured when the ramp is already ascending or descending.





When exporting a design from SmartCtrl to PSIM, a time delay block appears in the schematic, to take into account the different time delays of the control loop (shown in the images below). This time delay block represents only the time defined as tdelay, since the modulator delay is included in the behavior of the implemented PWM modulator. User must notice that the parameter to be entered in SmartCtrl is NOT t delay, but tsync, calculated depending on the parameters explained above.



1.18.1 Digital settings

Digital settings

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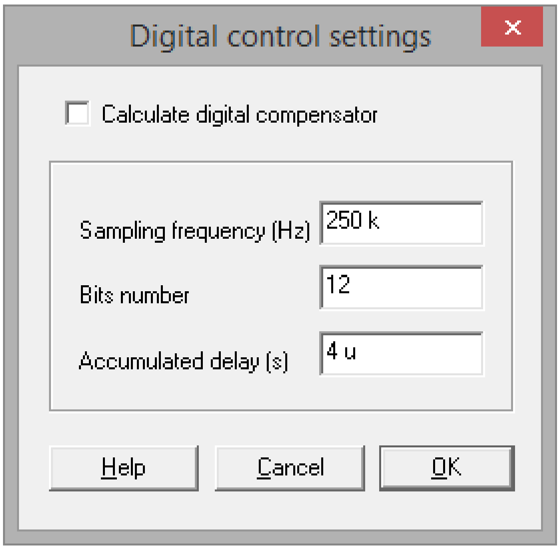
Push in the icon of the main toolbar to start the calculation of the digital regulators. This option is enabled after the calculation of an analog regulator. Digital regulators are calculated in SmartCtrl by discretization of analog regulators using the bilinear or Tustin transformation.



When starting the calculations of digital regulators, three specific parameters are required: sampling frequency, bits number and accumulated delay(s).

Sampling frequency. It is the sampling frequency of the digital regulator. The sampling period Tsamp=1/fsamp is the time between two consecutive samples of the output signal of the regulator.

In many applications, the sampling frequency (fsamp) of the regulator is equal to the switching frequency (fsw) of the power converter. In SmartCtrl the user can select different values for switching and sampling frequency, but **the sampling frequency must be a multiple or submultiple of the switching frequency**. This parameter is used to calculate the digital regulator by means of discretization of the analog regulator.

In current loops, the controlled quantity in the converter has a significant ripple. Therefore, it is recommended to use a Hall Effect sensor that includes a first order low pass filter that can act as an antialiasing filter.

Bits number. It is the number of bits used to represent the coefficients of the digital compensator considering a fixed point representation. The obtained coefficients are rounded to the nearest number that can be represented with the specified number of bits. One bit is used to represent the sign, and the rest to represent the integer part and the decimal part.

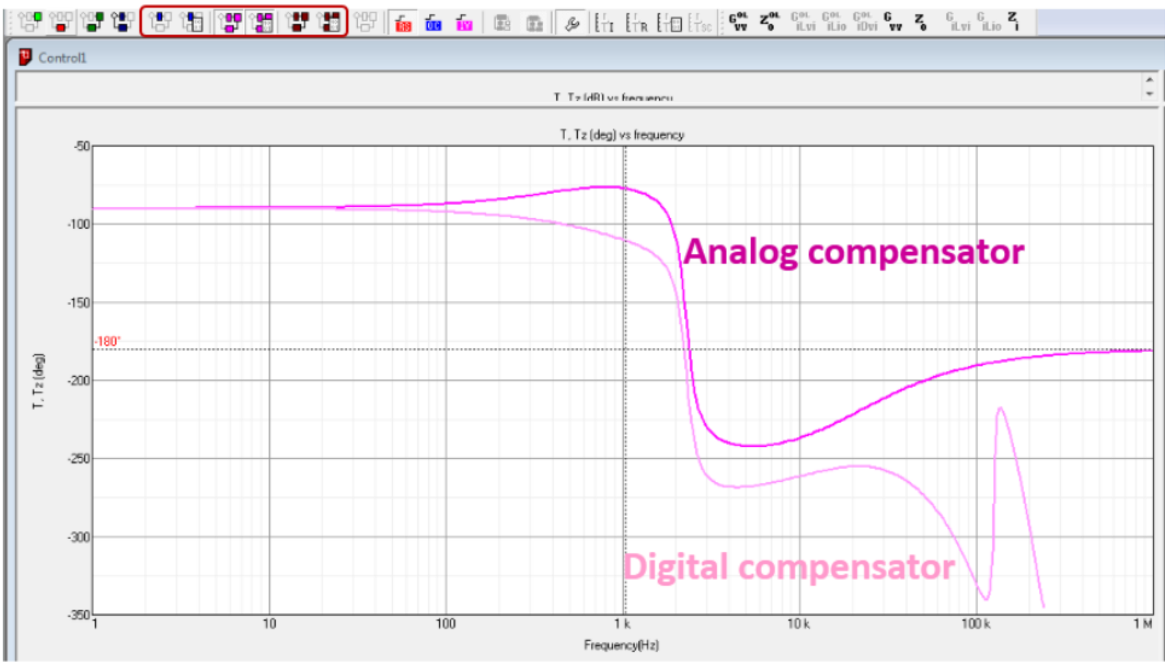
A low number of bits can result in a digital regulator significantly different from the analog regulator. It is recommended to check the similarity between the analog and digital regulator. If analog and digital responses are too much different, especially at low and medium frequencies, it is recommended to increase the Bits number.

Accumulated delay(s). It represents the total time delay in the control loop (modulator delay, calculation delay, ADC delay, etc).

This delay affects the actual phase margin obtained with the designed digital regulator. The delay is a negative phase that is subtracted to the phase of the open loop transfer function in the Bode plot. As the original (analog) regulator is calculated without considering the time delay, the obtained phase margin will be lower than the obtained in the analog regulator. This phase margin loss can be compensated by selecting a higher phase margin in the specification of the analog regulator.

It is recommended to check the effect of the delay in the Bode plot of the open loop transfer function and the closed loop transfer function. The accumulated delay is not represented in the Bode plot of the discretized compensator.

Once discretized, the Bode plots of both compensators can be compared, by activating its representation with the icons that appear in the main toolbar:



1.18.2 Parametric sweep in digital control

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Parametric sweep in digital control

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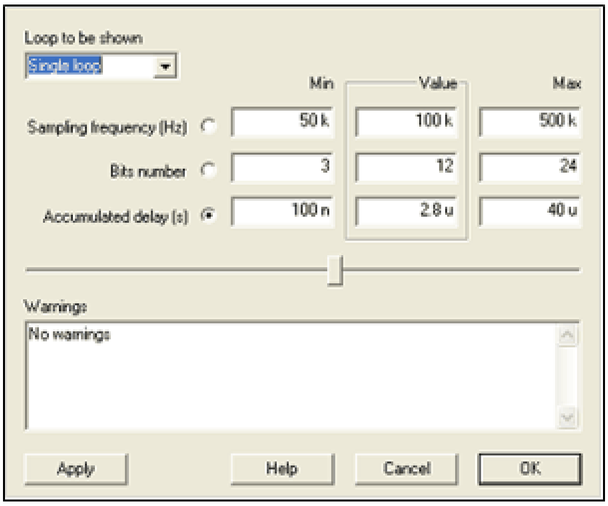
The three specific parameters of digital regulators can be swept: sampling frequency, number of bits and accumulated time delay.

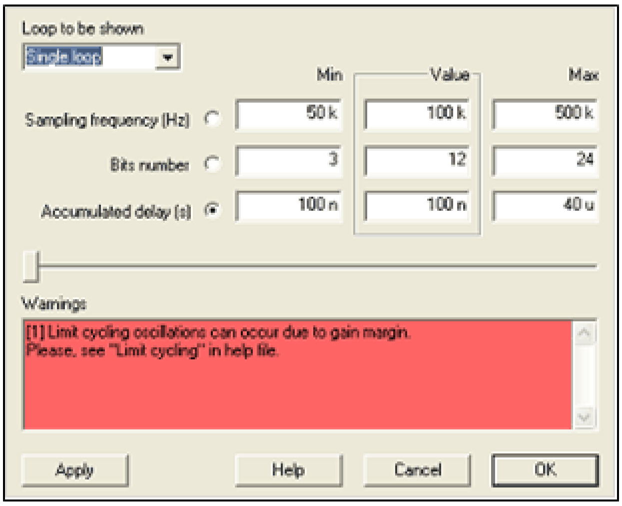
A warning box informs the user about limit cycling. From the four conditions of limit cycling referred in the technical literature [1], [2], the two depending only the regulator calculation are considered.



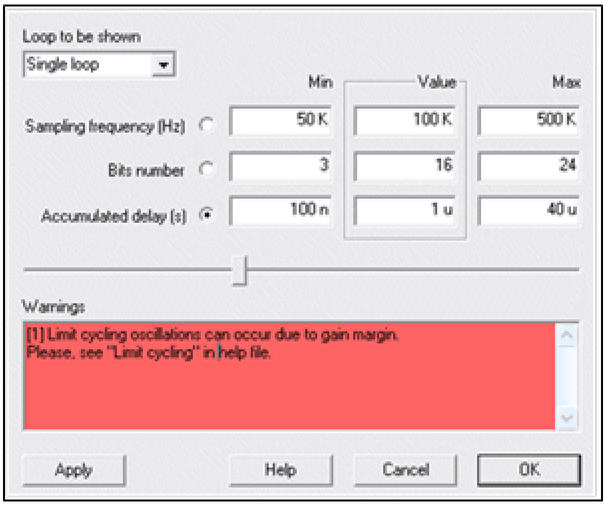
Integral gain and gain margin are evaluated and warning appears in case of non compliance of the limit cycling conditions [1], [2] . When a warning appears, if the limit cycling effect needs to be removed, redesign of the regulator needs to be done.

When limit cycling can occur because a too low gain margin, it must be increased. It is suggested to increase the desired phase margin in order to achieve a higher gain margin.

When limit cycling can occur because a too high integral gain, it is suggested to decrease the desired cross over frequency in order to need a lower integral gain.



[1] A.V.Peterchev, S.R.Sanders, Quantization resolution and limit cycling in digitally controlled PWM converters, IEEE Transactions on Power Electronics, Volume 18, No.1, Jan. 2003, pp.301-308
[2] H.Peng; D.Maksimovic, A.Prodic, E.Alarcon, Modeling of quantization effects in digitally controlled DC-DC converters, IEEE PESC 2004, pp.4312-4318.



1.19 Frequency settings

Navigation: SmartCtrl >

Frequency settings

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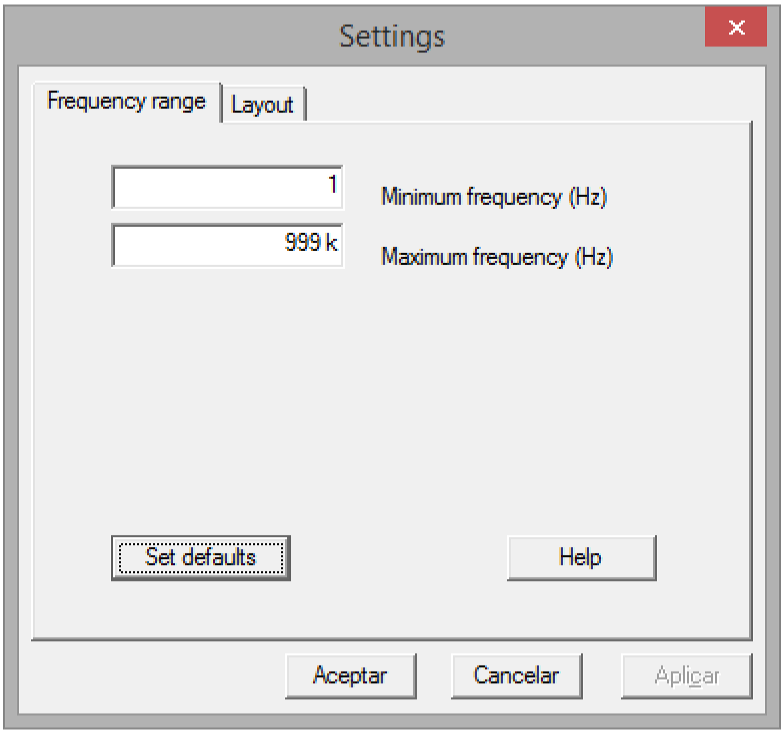
This option is available within the Tools Menu -> Settings.
It allows defining the minimum and maximum frequency of the range to be considered in the calculation of the Bode plots, solutions map, etc.



1.20 Layout settings

Navigation: SmartCtrl >

Layout settings

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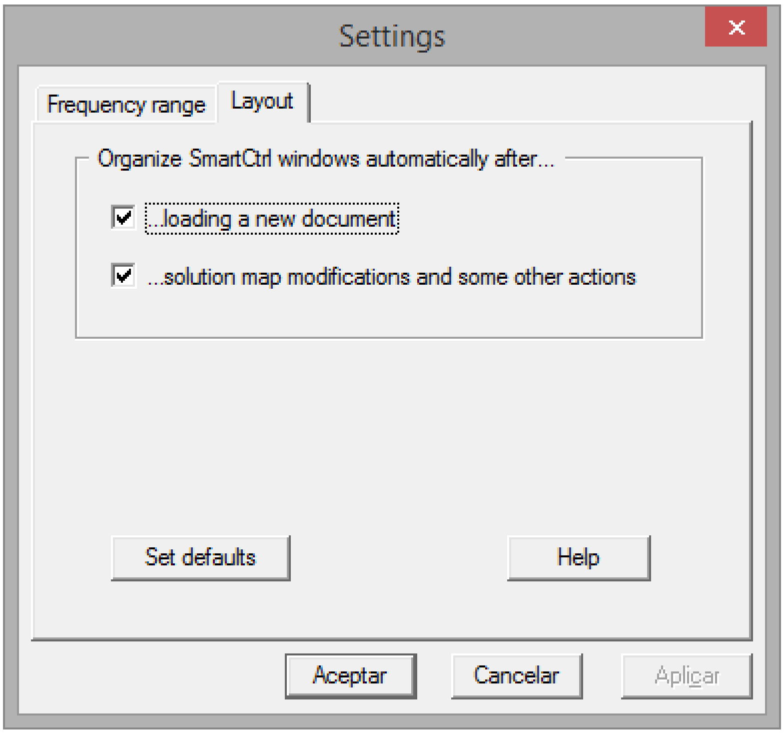
This option is available within the Tools Menu -> Settings.
It allows the user to define whether or not the graphic and text panels will be restored to their default size and appearance after the following two actions:

- After loading a new document
- After any modification on the solutions map



1.21 Warehouse

Navigation: SmartCtrl >

Warehouse

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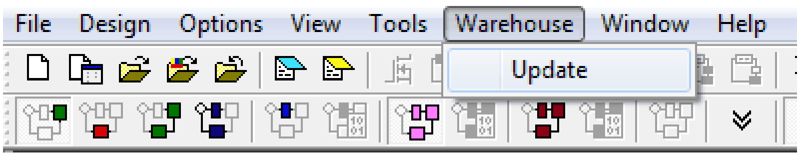
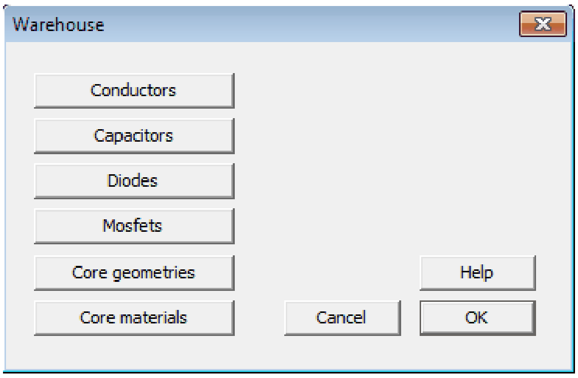
SmartCtrl provides a wide selection of different components used in the design of power circuits, called warehouse. This database is available through the next button:





Warehouse contains information of:

- •Conductors
- •Capacitors
- •Diodes
- •MOSFETs
- •Core geometries
- •Core materials

1.21.1 Warehouse components

Navigation: SmartCtrl > Warehouse >

Warehouse components

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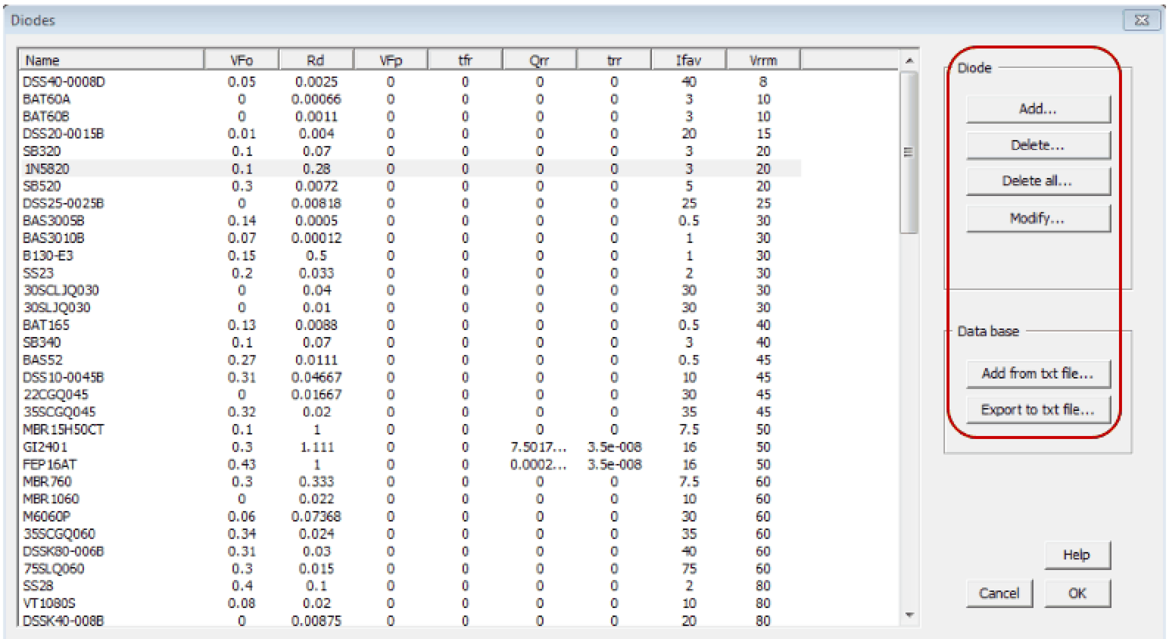
Once one of these components list is selected, the user can modify the database by adding, deleting or modifying a specific component or import a new database from an external txt file. It is also possible to export the current database to a .txt file, with values separated by tabs.



Name	VFo	Rd	VFp	tfr	Qrr	trr	Ifav	Vrrm
DSS40-0008D	0.05	0.0025	0	0	0	0	40	8
BAT60A	0	0.00066	0	0	0	0	3	10
BAT60B	0	0.0011	0	0	0	0	3	10
DSS20-0015B	0.01	0.004	0	0	0	0	20	15
SB320	0.1	0.07	0	0	0	0	3	20
1N5820	0.1	0.28	0	0	0	0	3	20
SB520	0.3	0.0072	0	0	0	0	5	20
DSS25-0025B	0	0.00818	0	0	0	0	25	25
BAS3005B	0.14	0.0005	0	0	0	0	0.5	30
BAS3010B	0.07	0.00012	0	0	0	0	1	30
B130-E3	0.15	0.5	0	0	0	0	1	30
SS23	0.2	0.033	0	0	0	0	2	30
30SCLJQ030	0	0.04	0	0	0	0	30	30
30SLJQ030	0	0.01	0	0	0	0	30	30
BAT165	0.13	0.0088	0	0	0	0	0.5	40
SB340	0.1	0.07	0	0	0	0	3	40
BAS52	0.27	0.0111	0	0	0	0	0.5	45
DSS10-0045B	0.31	0.04667	0	0	0	0	10	45
22CGQ045	0	0.01667	0	0	0	0	30	45
35SCGQ045	0.32	0.02	0	0	0	0	35	45
MBR15H50CT	0.1	1	0	0	0	0	7.5	50
GI2401	0.3	1.111	0	0	7.5017...	3.5e-008	16	50
FEP16AT	0.43	1	0	0	0.0002...	3.5e-008	16	50
MBR760	0.3	0.333	0	0	0	0	7.5	60
MBR1060	0	0.022	0	0	0	0	10	60
M6060P	0.06	0.07368	0	0	0	0	30	60
35SCGQ060	0.34	0.024	0	0	0	0	35	60
DSSK80-006B	0.31	0.03	0	0	0	0	40	60
75SLQ060	0.3	0.015	0	0	0	0	75	60
SS28	0.4	0.1	0	0	0	0	2	80
VT1080S	0.08	0.02	0	0	0	0	10	80
DSSK40-008B	0	0.00875	0	0	0	0	20	80